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# Power and Performance Analysis of Doped SW/DW CNT for On-Chip Interconnect Application

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**Abstract** – In this paper, we investigate the electrical properties of doped single wall (SW) and double wall (DW) carbon nanotube (CNT) for integrated circuits interconnect applications. P-type Iodine charge transferred doping has been studied for modifying electrical properties and models of CNT interconnects. We perform circuit-level simulations on a 5-stage ring oscillator implemented with 45nm CMOS technology node devices for power and performance analysis with doped SWCNT and DWCNT interconnects.

## Introduction

There is a lot of interest and on-going research on carbon nanotubes as a novel material for faster and energy efficient devices, next generation of organic solar cells and fast-charging batteries. In this work, we explore CNT as back-end-of-line interconnect material for integrated circuits. With continuous technology node scaling following Moore's law, the impact of interconnects is becoming dominant due to their significant contribution to delay and power consumption on very large scale integrated (VLSI) circuit. Current copper interconnects are reaching their limit on current density, thermal conductivity performance, thus finding a new interconnect material is imminent and is an on-going quest [1][2].

CNT with its high conductivity, high electro-migration, and the low-temperature effect is a promising candidate for on-chip interconnects applications [3]. Here, we investigate on metallic CNTs as on-chip interconnects material for signal, clock and

power delivery. Uncontrollable chirality of CNTs motivates us to study doped CNTs with the expectation of optimizing semiconducting CNTs and enhancing metallic CNTs' performance. In this paper, we study p-type Iodine intercalate doping. Iodine is known as a good donor. Iodine provides charge transfer towards CNT – this type of doping is chemically and morphologically more stable than CNT surface substitutional doping [4]. We consider an iodine molecule chain located inside the innermost shell of CNTs. The different number of iodine atoms in the chain represent different doping concentration, which shifts Fermi-level differently in a CNT Fermi-Dirac energy band. Density-functional Theory with Generalized Gradient Approximation (DFT-GGA) [5] can calculate the conductivity of this p-type Iodine doping. By dividing the conductivity after doping by intrinsic one electron quantum conductivity  $G_0$  ( $G_0 = 2e^2/h$ ) gives the number of conducting channels of doped CNTs (we consider one electron occupies one conducting channel). We vary the number of conducting channels in simulations to see how doping impacts the electrical performance of metallic CNT interconnects.

## Physical electrical modeling and simulations

Based on Banerjee and Li's work [1][2], We investigate on electrical physical modeling of doped SWCNT and DWCNTs. A SWCNT is modeled as RLC (resistance, inductance, and capacitance) circuit with intrinsic quantum components and diffusive scattering dependences. For DWCNT, mutual interaction effects between two shells are also taken into account. For the doped CNTs, quantum resistance and capacitance are modified accordingly. From quantum physics, it is expected that doping shifts the Fermi-level position, hence provides more available electron states for charge transport [3], which increases the number of

conducting channels as shown in equation (1) below:

$$N_{channels/shell} = \sum_{all\ subband} \frac{1}{\exp\left(\frac{|E_i - E_F|}{k_B}\right) + 1} \quad (1)$$

Where  $E_i - E_F$  is the difference between the possible participating electron energy subband and the Fermi-energy level.

We believe that doping reduces the overall CNT resistance (R) [4]; however, it increases the capacitance (C) effects where the quantum capacitance is  $C_Q = N_{channels} \times 200aF$  (where  $200aF$  is calculated for one electron conducting channel [7]). Therefore, we aim to study the impacts on delay and power consumption for doped CNTs interconnects which depend on both R and C parasitics.

In this paper, we perform circuit-level simulations to analyze delay and power consumption for SWCNT and DWCNT interconnect before and after doping. Ring oscillator (which includes five inverter stages implemented in 45nm CMOS technology node) simulations with electrical models (Figure 1) have been performed on Cadence with Verilog-A models. We study the power and performance (i.e., signal delay) for different SWCNTs (Figure 2) and DWCNTs (Figure 3). SWCNT's diameters are chosen to vary from 3nm to 5nm, which are also the most reliable fabricating range. Based on the calculation of DFT-GGA and methodology described at the end of the previous section, we vary the number of conducting channels from 2 to 8 for SWCNT to represent doping effects corresponding to more available electron transport states after Fermi-level shift. For DWCNT, the inner diameter is chosen as 5nm, and the inter-shell distance is respected to the Van der Waals distance (0.34nm). Based on the study of iodine intercalate doping of CNTs [5] and DFT-GGA calculation, we assume for a DWCNT, the augmentation of conducting channels is directly related to the inner shell; hence, we only vary the inner shell conducting channel numbers from 2 to 12.

## Simulation results and discussions

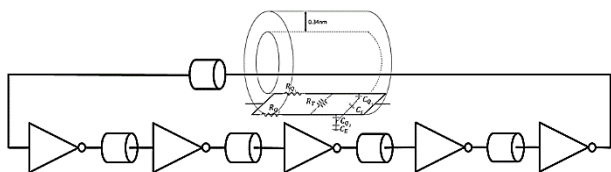
Simulation results show that with increasing of CNT length, signal delay increase and power consumption decrease for both SWCNT and DWCNT. SWCNT used as local interconnect length ( $< 1\mu m$ ), show no evident better performances on delay and power consumption after doping. For semi-global interconnect length (1-100 $\mu m$ ), doping with 8 conducting channels leads up to 4 times higher capacitance effect which gives a 26.9% augmentation of power consumption; however, doping starts to have a decreasing effect on delay when SWCNTs are longer than 10 $\mu m$ . For CNT length of 1mm (global interconnect), doping can reduce 27% of delay but increase 7% of power consumption.

For DWCNT, doping does not improve signal delay on different interconnect lengths. We obtain up to 66.7% of capacitance increase when inner shell conducting channels vary from 2 to 12. However, we observe that overall delay of DWCNT is less than in SWCNT interconnects especially for lengths longer than 100 $\mu m$ . For an interconnect length of 1mm, signal delay can be reduced by 7.6% when using doped DWCNT instead of doped SWCNT, and with a delay reduction of 54.7% when compared to pure SWCNT interconnects.

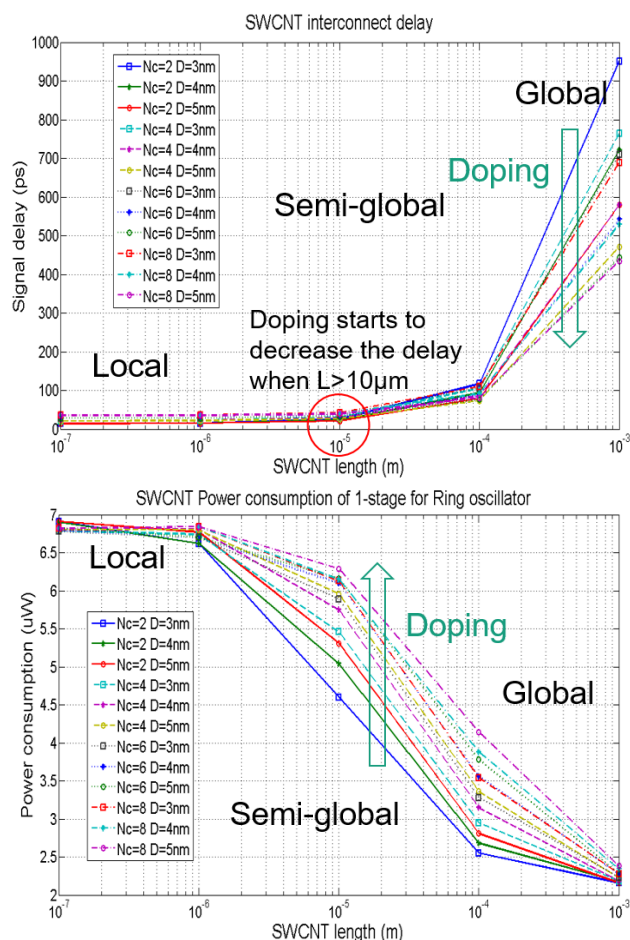
## Conclusion

In this paper, we investigate the electrical modeling of Iodine molecules intercalate charge transfer doping for SWCNTs and DWCNTs as on-chip interconnect material. We also provide signal delay and power consumption simulations for doped SWCNTs and DWCNTs with different aspect ratios. Our simulation results show that for a local interconnect length ( $< 1\mu m$ ), doping does not improve SWCNTs and DWCNTs interconnect performance. In the semi-global interconnect range (1-100 $\mu m$ ), doped SWCNT starts to have better performance as SWCNT get longer than 10 $\mu m$ . Meanwhile, doped global interconnects DWCNTs with the length of 1mm, can reduce up to 54.7% of signal delay compared to pure SWCNT. However, no significant improvement in power consumption is observed mainly due to an increase of quantum capacitance.

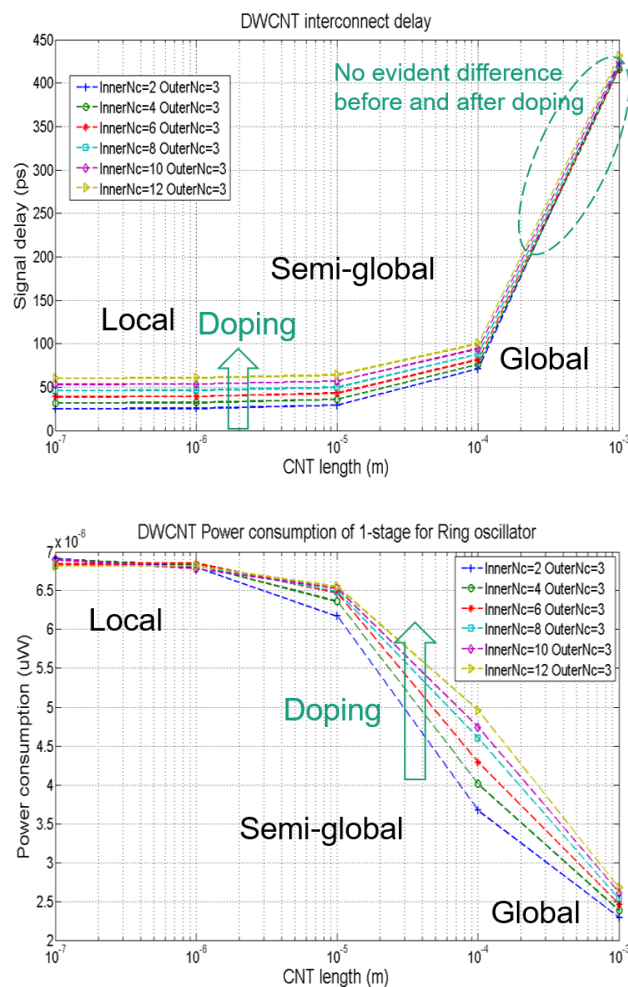
## Figures



**Figure 1:** Ring oscillator simulations of DWCNT with RC circuit model.



**Figure 2:** Signal delay and power consumption for SWCNT interconnect with different conducting channels.



**Figure 3:** Signal delay and power consumption for DWCNT interconnect with different conducting channels.

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