Power Supply Noise Aware Task Scheduling on Homogeneous 3D MPSoCs Considering the Thermal Constraint

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Abstract Thanks to the emerging 3D integration technology, The multiprocessor system-on-chips (MPSoCs) can now integrate more IP cores on chip with improved energy efficiency. However, several severe challenges also rise up for 3D ICs due to the die-stacking architecture. Among them, power supply noise becomes a big concern. In the paper, we investigate power supply noise (PSN) interactions among different cores and tiers and show that PSN variations largely depend on task assignments. On the other hand, high integration density incurs severe thermal issue on 3D ICs. In the paper, we propose a novel

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task scheduling framework considering both the PSN and the thermal issue. It mainly consists of three parts. First, we extract current stimuli of running tasks by analyzing their power traces derived from architecture level simulations. Second, we develop an efficient PDN solver to evaluate PSN magnitudes efficiently. Third, we propose a heuristic algorithm to solve the formulated task scheduling problem. Compared with the state-of-the-art task assignment algorithm, the proposed method can reduce PSN by 12% on a $2 \times 2 \times 2$ 3D MPSoCs and by 14% on a $3 \times 3 \times 3$ 3D MPSoCs. The end-to-end task execution time also improves as much as 5.5% and 7.8% respectively due to the suppressed PSN.

Keywords power supply noise (PSN), power delivery network (PDN), task scheduling algorithm, temperature, 3D MPSoCs

1 Introduction

With the exponential increase of transistor count on-chip and insatiable demand of high performance, the power density on-chip increases dramatically. “Power Wall” issue becomes a serious concern for modern VLSI designers [1]. The stringent power constraint makes it extremely difficult to squeeze extra performance by simply scaling the clock frequency. As a result, MPSoCs (Multi-Processor System on Chips) emerge as an effective technique to continue Moore’s law, especially in the embedded system domain [2] because of their better energy efficiency. Moreover, MPSoC design methodology facilitates integration of various IP cores from different vendors, which reduces the design complexity and accelerates time-to-market greatly.

Recently, the emerging 3D integration technology is adopted in the MPSoC design (i.e., 3D MPSoCs) to approach higher integration density and more functionalities than the 2D counterpart [3]. By stacking several thinned tiers vertically, data communication bandwidth and power consumption can be improved greatly with the aid of through-silicon-vias (TSVs). However, the 3D MPSoC architecture also presents several challenges due to the die-stacking structure. Among them, signal integrity is a critical issue for chip reliability. Since IP cores residing on different tiers commonly share a power delivery network [4], the activities on one core may propagate to cores in its vicinity by the shared power delivery network. The shrinking power supply voltage and increasing magnitudes of current transients make the power supply noise (PSN) more significant on 3D MPSoCs compared with their 2D counterparts. To constrain the PSN magnitude, many effective methods are proposed from different optimization perspectives. Todri *et al.* investigated the PSN interactions on a multi-processor platform, and derived several guidelines for workload assignments to suppress the PSN [5]. Wang *et al.* optimized the task mapping and scheduling to minimize the PSN induced by power gating [6]. Although their work provides insights of the PSN effect in traditional MPSoCs, the proposed method can not be simply extended to 3D MPSoCs due to the following reasons. First, each tier manifests different characteristic impedance and may experience different voltage drop [7]. Second, the PSN can propagate from one tier to other tiers through TSVs, which introduces non-negligible PSN couplings. As a result, the heterogeneity of die-stacking structure and complicated PSN interactions require a novel hardware-software co-design methodology for 3D MPSoCs to suppress PSN effectively.

On the other hand, the reliability of 3D MPSoCs is also threatened by the thermal issue [8]. Stacking several tiers together presents a severe challenge on thermal dissipation. High temperature can aggravate the NBTI (Negative Bias Temperature Instability) and the hot carrier injection effect [9]. Since upper tiers are thinned before integration to facilitate die stacking, the vertical thermal correlation dominates the heat dissipation in 3D MPSoCs, which makes the thermal modeling of 3D MPSoCs different from those of 2D counterparts.

In the paper, we explore to deal with the above two reliability concerns from the task assignment perspective for hard real-time applications on homogeneous 3D MPSoCs. In the hard read-time application, the task graph extracted is predetermined and the deadline must be guaranteed [10]. With an illustrative example, we show that different task mapping and scheduling schemes may result in significantly different PSN distributions, which implies the large optimization potential by PSN aware task scheduling. However, we observe that the conventional thermal aware task assignment scheme may cause severe PSN, which motivates our work. In order to optimize task scheduling with both thermal and PSN concerns, we propose a framework to evaluate the PSN and thermal distributions effectively. First, we extract representative power traces from real applications, and convert them to current stimuli traces instead of the traditional triangular or trapezoidal current stimuli to make the PSN calculation more accurate and realistic. Second, we construct a power delivery network (PDN) model of 3D MPSoCs for PSN calculations, and develop a fast power grid solver to facilitate PSN analyses. Based on these modeling techniques, we formulate the task scheduling optimization as an linear programming problem, which minimizes the PSN with the peak temperature constraint. Then, a list-scheduling based heuristic algorithm is proposed to obtain the optimal task scheduling solution. Extensive simulation results show that the proposed algorithm can reduce PSN by 12% on a $2 \times 2 \times 2$ MPSoC and 14% on a $3 \times 3 \times 3$ MPSoC platform compared with the state-of-the-art thermal aware task scheduling scheme [11]. Additionally, task execution time can be improved by 5.5% and 7.8% respectively due to the reduced PSN.

Our main contributions are listed as follows.

- We proposed an efficient architecture-level PSN simulation framework to fill the gap between circuit-level PSN simulation and architecture-level task scheduling for 3D MPSoCs.
- Our another contribution is considering both power supply noise and temperature to effectively avoid hotspot during the PSN optimization for 3D MPSoCs.
- We propose a novel list-scheduling based heuristic algorithm for the task scheduling problem on homogeneous 3D MPSoCs with both thermal and PSN considerations. Extensive simulation results show that the proposed algorithm can reduce PSN by 12% on a $2 \times 2 \times 2$ MPSoC and 14% on a $3 \times 3 \times 3$ MPSoC compared with the state-of-the-art thermal aware task scheduling scheme [11]. Additionally, task execution time can be improved by 5.5% and 7.8% respectively due to the reduced PSN

The rest of the paper is organized as follows. Section 2 presents the preliminaries of 3D MPSoC PDN and thermal modeling techniques. Task graph is also introduced in this section. An illustrative example is presented in Section 3 to motivate our work. Section 4 formulates the PSN aware task scheduling problem with the thermal constraint and proposes a framework to solve it. The computing complexity analysis of the proposed algorithm is given in this section as well. Section 5 shows the experimental results by running our task scheduling algorithm extensively on different scales of 3D MPSoCs. Section 6 presents the related work and Section 7 concludes the paper.

2 Preliminaries on Power Delivery Network and Thermal Modeling Techniques of 3D MPSoCs

For the ease of understanding, some necessary background knowledge is introduced as follows.

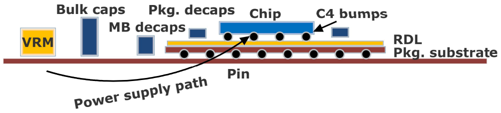


Fig. 1: The power delivery system including both off-chip and on-chip components.

2.1 Power Delivery Network Modeling and PSN Evaluation for 3D MPSoCs

In general, a chip power delivery network consists of off-chip and on-chip power delivery interconnects as shown in Fig. 1. A VRM (voltage regulator module) converts the high voltage (e.g., 2.5V) to the chip operating voltage (e.g., 1V). Then the supply voltage goes through the motherboard, P/G pins and on-chip interconnects to drive transistors on-chip. The PDN design needs to be determined at the early stage of chip design as any PDN change in the later phase of design flow may introduce expensive design iterations. Therefore, it is imperative to predict the supply voltage variations accurately to evaluate its impact on-chip performance and reliability as early as possible. As suggested in [12], it is necessary to consider both package and on-chip power delivery network for accurate PSN prediction. Traditionally, the package is modeled considering its inductive effect while on-chip interconnects are modeled considering their resistive and capacitive effects. However, as the working frequency increases, on-chip inductance can no longer be ignored [13]. In the paper, we model both the package and on-chip PDNs to capture PSN accurately.

We assume the on-chip PDN is in the mesh topology and shared by all cores on-chip as similar to [14]. The power and grid lines interleave with each other in one metal layer and are orthogonally aligned on different layers for PSN reduction. P/G interconnects on different layers are connected by vias and deliver the power from global metal layers to local metal layers. A simplified model of a typical mesh PDN for 3D homogeneous MPSoC is shown in Fig. 2. As shown in the figure, current is delivered from the package to the on-chip PDN through P/G C4 bumps, and the power supplies of upper tiers are provided from the bottom tier through P/G TSVs similar to the structure mentioned in [15].

Then, the PSN can be calculated as follows [16]:

$$
\begin{aligned}
V_{pnoise} &= \int_{\mathrm{t_s}}^{\mathrm{t_e}} \max\{V_{dd} - V_p, 0\}\mathrm{d}t/(t_e - t_s),\\
V_{gnoise} &= \int_{\mathrm{t_s}}^{\mathrm{t_e}} max\{V_{ss}, 0\}\mathrm{d}t/(t_e - t_s),\\
V_{noise} &= V_{pnoise} + V_{gnoise}.
\end{aligned}
$$

where $\mathrm{t_s}$ is the start of the timing window for the PSN calculation, and $\mathrm{t_e}$ is the end of the timing window. V_{dd} is the normal power supply voltage. V_p is the real voltage of the power grid node under investigation, and V_{ss} is the ground bounce of the corresponding ground grid node. Using the above equations, we can calculate the PSN magnitude of each P/G grid node considering both voltage drop (V_{pnoise}) and ground bounce (V_{gnoise}).

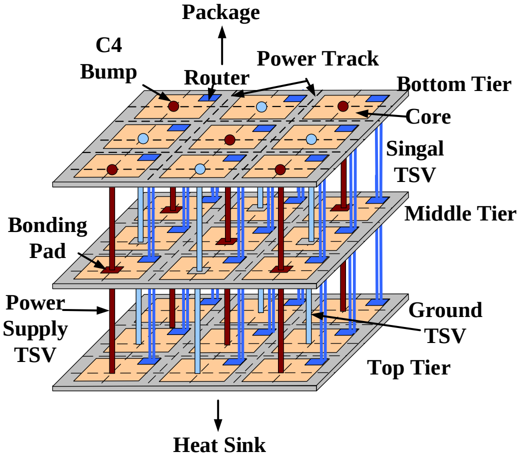


Fig. 2: On chip mesh grid power delivery network of homogeneous 3D MPSoCs.

2.2 Thermal Modeling Techniques for 3D MPSoCs

Since the thermal issue is another important concern for 3D ICs, it is imperative to consider the thermal constraint during workload assignment optimization for 3D MPSoCs. In order to capture on-chip thermal distribution, an accurate thermal model is required. Thermal modeling techniques for 3D ICs can be classified into several categories.

- Solve the heat flow equation directly to get the temperature distribution on-chip by the finite element method or finite differential method [17, 18].

- Utilize duality between the thermal and the electrical properties. The thermal conductivity can be modeled as the resistance in the equivalent electrical circuit. The temperature difference corresponds to the voltage difference. The power consumption can be modeled as the current source. Then, the temperature of each node can be solved by circuit analyses [19].

- Utilize on-chip power information such as the power gradient, to roughly estimate the temperature variations among functional blocks or cores [20].

The first method can obtain the accurate solution, but the computing complexity is too high to be adopted for the large scale of MPSoCs. The last one is the fastest method but it can only be used for qualitative analyses lacking of enough accuracy. The second method listed above makes a good trade-off between the accuracy and the efficiency. The widespread used thermal simulation tool Hotspot [21] is based on the second method and we will use it to evaluate the thermal distribution in this paper.

2.3 Introduction to Task Graph

In the paper, we assume that the running application can be split into a number of tasks with specified timing dependencies and constraints. Then, the application can be represented by a directed acyclic task graph, which is widely used for task scheduling research [11]. A task graph example is shown in Fig. 3. In the figure, a node in the task graph denotes a task of the running application, and an edge denotes the task running priority and the running dependency. For example, task S_2 can only execute after S_1 finishes. The weight of the node (i.e., t_i) denotes the execution time of the task. For real-time applications, each task node has the deadline constraint and the task execution can not violate it.

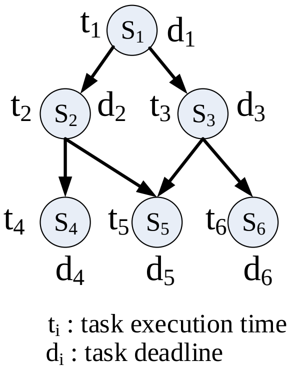


Fig. 3: An illustrative task graph example.

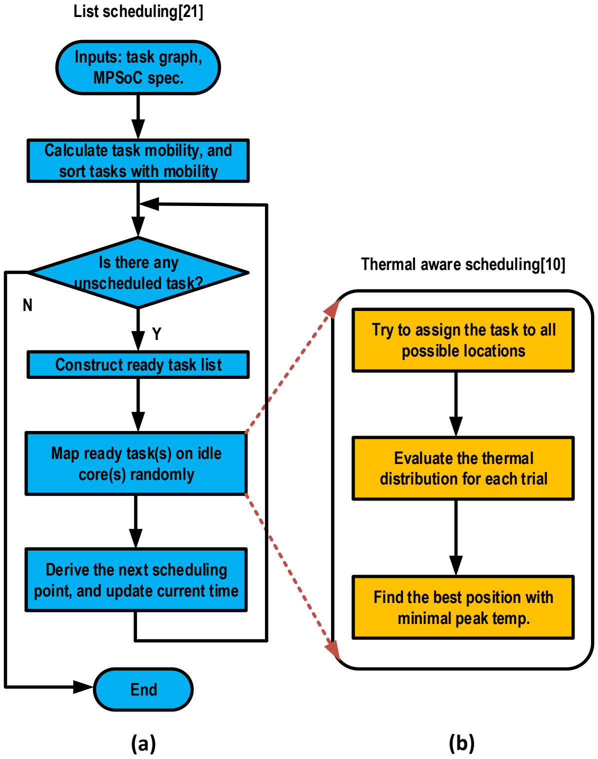

List scheduling[21]
Inputs: task graph, MPSoC spec.
Calculate task mobility, and sort tasks with mobility
Is there any unscheduled task?
N
Y
Construct ready task list
Map ready task(s) on idle core(s) randomly
Derive the next scheduling point, and update current time
End
Thermal aware scheduling[10]
Try to assign the task to all possible locations
Evaluate the thermal distribution for each trial
Find the best position with minimal peak temp.
(a)
(b)

Fig. 4: (a) The flow chart of the list scheduling scheme [10]. (b) The thermal aware scheduling algorithm [11].

3 Motivation

In this section, we investigate PSN distributions caused by different task allocation schemes. For the completeness of the paper, we briefly introduce the task allocation schemes used in our investigation. The first scheme is based on the conventional list scheduling algorithm [10] as shown Fig. 4(a). According to the task execution deadline, it calculates the earliest start time (i.e., EST) and the latest start time (i.e., LST) of each task. Then, all tasks are sorted with their mobilities (i.e., the difference of LST and EST). At each schedule point, the scheduler assigns a ready task to an idle core randomly. When all ready tasks are allocated, the time will advance to the next scheduling point. If all cores are busy such that no ready task can be allocated at current scheduling point, the time will advance to the next one when at least one core becomes idle. The second scheme is the state-of-the-art thermal aware task scheduling algorithm proposed by [11] as shown in Fig. 4(b). The scheduler evaluates the thermal distribution on-chip at each scheduling point for each possible task assignment, and the scheduler chooses the best candidate position approaching the lowest peak temperature. The third scheme is similar to the thermal aware scheduling but evaluates PSN instead. At each schedule point, the scheduler will assign the ready task to the available position approaching minimal PSN (the PSN evaluation procedure will be detailed in the next section).

To illustrate scheduling results using the three task assignment schemes, we use TGFF [22] to generate a task graph and schedule it on a $2 \times 2 \times 2$ 3D MPSoC using these schemes. The task graph has 20 nodes and 30 edges. The task characterizations, detailed simulation setup, PDN and thermal model parameters are presented in Section 4 and Section 5 respectively. Table 1 indicates the comparisons among three algorithms (conventional list scheduling algorithm, i.e., the "Random" algorithm in the table, thermal aware scheduling algorithm and PSN-aware scheduling algorithm wihtout thermal consideration) in terms of temperature and PSN.

Table 1: PSN and Temperature Comparisons of Three Task Assignment Schemes[a]

	Random	T-aware	PSN-aware
PSN (mV)	147.6	174.7	143.2
Temp. (K)	310.3	307.5	309.3

[a] T-aware denotes the thermal aware task scheduling scheme and PSN-aware denotes the PSN aware task scheduling scheme. Both PSN and temperature values are the peak values among all cores.

Table 2: Psn and Temperature Comparisons of Three Task Running Scenarios

	Case 1			Case 2			Case 3		
	Bottom	Middle	Top	Bottom	Middle	Top	Bottom	Middle	Top
PSN(mV)[a]	**54.8**	46.6	46.5	42.4	**59.8**	49.3	41.1	48.2	**63.4**
Temperature(K)[b]	**304.8**	303.5	302.77	**303.67**	303.51	302.78	**303.26**	303.1	302.79

[a,b] Both PSN and temperature values are the peak values among all cores on the same tier.

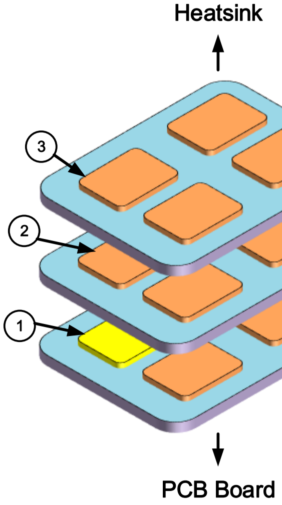


Fig. 5: Running a single task on different tiers for thermal and PSN comparisons: (1) running the task on the bottom tier; (2) running the task on the middle tier; (3) running the task on the top tier.

As shown in Table 1, the random task assignment scheme can be neither thermal nor PSN friendly. Moreover, we can observe that the thermal aware scheduling scheme may generate severe peak PSN (increasing 18% compared with that of the PSN-aware case). In contrast, PSN aware task scheduling scheme may incur higher peak temperature than that of thermal aware scheduling algorithm.

To examine the conflict between the thermal aware scheduling scheme and the PSN aware scheduling scheme, we investigate the thermal and PSN distributions of each tier when running a single task on different tiers as shown in Fig. 5. In case 1, the task is assigned to the bottom tier. In case 2, it is assigned to the middle tier. In case 3, it is assigned to the top layer. In Fig. 5, we assume that the bottom tier is attached to the PCB board and provides power supply for upper tiers while the top tier is attached to the heatsink for thermal dissipation. Both the peak temperature and the PSN magnitude of each tier are shown in Table 2.

As shown in Table 2, the peak PSN magnitude is the largest when the task is assigned to the top tier (63.4mV). The peak PSN magnitude is the smallest when the task is assigned to the bottom tier (54.8mV). From the power supply noise suppression perspective, it is preferable to schedule the task near the bottom tier as much as possible. Since the power supply has to go through the bottom and the middle tier to reach PDN on the top tier, the top tier suffers from more severe PSN than other tiers [23]. On the other hand, when the task is allocated on the bottom tier, the peak temperature is the highest (304.8K) among all three cases. Therefore, from the heat dissipation perspective, it is better to assign the task in upper tiers which are closer to the heat sink. As a result, there is conflict between the PSN-aware task scheduling and the thermal-aware task scheduling, which is coincide with [19]. The above analyses imply that it is necessary to consider both thermal and PSN issues during the task scheduling to ensure the reliability and availability of 3D MPSoCs.

4 Proposed Framework for Task Scheduling on 3D MPSoCs Considering Both Thermal and PSN Issues

In order to evaluate the temperature and PSN distributions, we need to build the thermal and electrical PDN models of 3D MPSoCs. Traditionally, considering the large scale of on-chip power grid, stimuli of the PDN are usually simplified as current sources with some regular waveforms such as the triangular or trapezoidal waveforms. Although this assumption reduces the complexity of solving PDN equations, it sacrifices simulation accuracy and can not reflect the real activities and different characteristics of various running tasks. To illustrate this point, we perform the power supply noise simulations with two different methods. In the first one, we extract the power traces by the architecture level simulation, and convert them to the stimuli to the PDN for PSN simulations. In the second method, the PDN stimuli waveforms are simplified as triangular waveforms, and the average power consumption is set as the same with that of the first method. The experimental results on a single core show that the PSN error of the first method can be as large as 51.35% (please refer to Section 5 for the experimental setup). Therefore, it is imperative to consider application running characteristics derived from the power traces for the accurate PSN evaluation.

In this paper, we propose a power trace based architecture level PSN evaluation framework. The advantages of this framework are as follows. First, the architecture level simulation can improve the PSN calculation efficiency and save significant computing overhead. Second, various characteristics of tasks can be captured by power traces extracted. Therefore, interactions of tasks running simultaneously can be captured by feeding power traces to the PDN

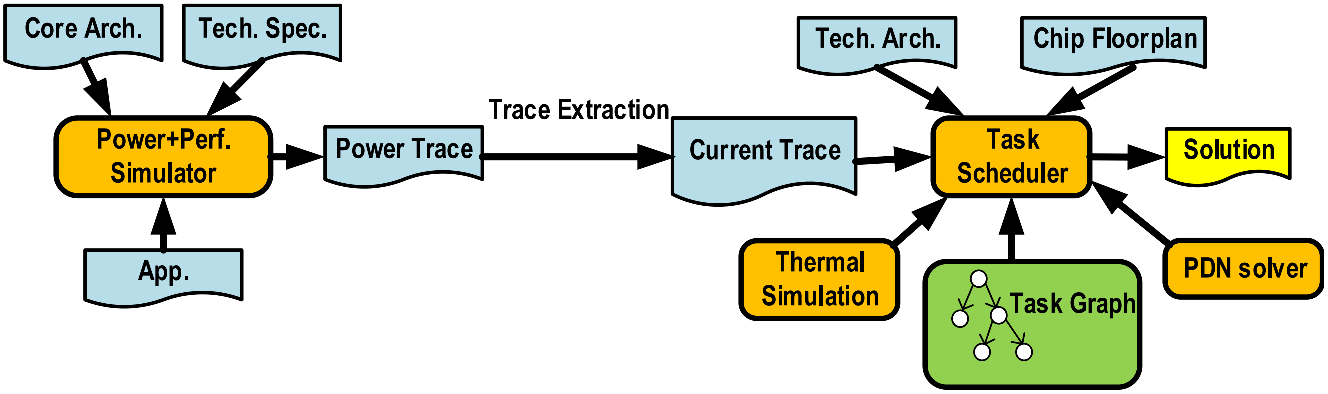


Fig. 6: Proposed task scheduling framework considering both thermal and PSN issues.

model.

Our proposed framework can be divided into three steps as shown in Fig. 6.

- First, we input the core architecture, technology parameters to set up the architecture-level simulator. Then, power traces of different tasks are extracted with simulations.

- Second, power traces are converted into current traces and fed into the 3D MPSoC PDN model for PSN calculations. We develop an efficient PDN solver to accelerate the PSN evaluations instead of the time-consuming HSPICE simulations.

- At last, we formulate the task scheduling problem and propose a heuristic algorithm to solve it. The task graph and 3D MPSoC architecture specifications are inputs to the task scheduler. During the task scheduling, thermal simulations and PSN calculations are performed to find the optimal solution.

In the following, we will detail each step of the framework.

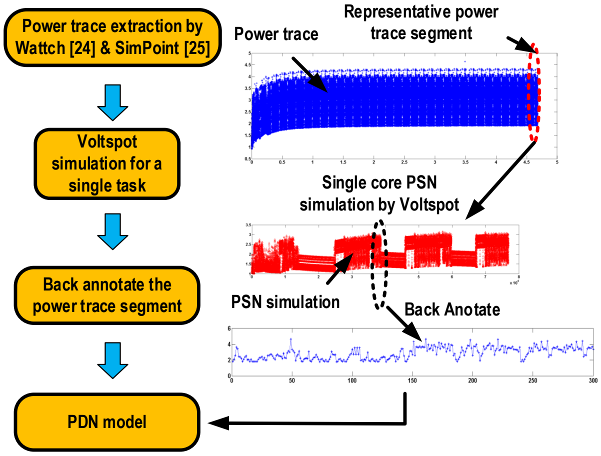

Power trace extraction by Wattch [24] & SimPoint [25]
Voltspot simulation for a single task
Back annotate the power trace segment
PDN model
Power trace
Representative power trace segment
Single core PSN simulation by Voltspot
PSN simulation
Back Anotate

Fig. 7: Illustration of the workload characterization process.

4.1 Power Trace Based Task Characterization

Tasks running simultaneously on the 3D MPSoC have different characteristics, such as peak current magnitudes, running frequencies, power consumptions. Furthermore, their behaviors may affect one another when running at the same time. Individual workload or workload combinations may cause different PDN responses due to PSN propagation and intercoupling. In the paper, we use the architecture level simulation to get the power consumption information and then derive waveforms of current stimuli, which can be integrated with the PDN model conveniently for PSN analysis. Although there is another simulation tool Voltspot available for power trace driven PSN simulation [24], it could not scale very well for large scale 3D MPSoCs and incurs unacceptable running time overhead. Therefore, we propose the " single core power trace extraction + custom PDN solver" for the PSN evaluation. We choose Wattch [25] for power trace extraction since it can get a satisfied trade-off between the running speed and the accuracy for a single core simulation. Note that our proposed framework does not depend on the specific simulator.

Then, the generated power trace can be converted to current traces and integrated with the PDN model. Here, we will take a SPEC2000 application "ammp" as an example to illustrate the workload characterization process as shown in Fig. 7.

Considering the large scale of power grid, it cannot afford to apply the entire power trace for PSN calculations, which will incur unacceptable running time overhead. Therefore, it is necessary to capture the representative segment of the extracted power trace. We use SimPoint [26] to identify several different running phases of "ammp". For each identified running phase, we fast forward 1 million instructions for the cache warm-up and perform detailed timing simulation for another 1 million instructions (refer to Section 5 for our architecture simulation setup). Then, we extract 10000 cycle long segment from the generated power trace, which can capture the peak power consumption. Although the power consumption has close relationship with power supply noise, we observe that the maximum PSN may not exactly happen at the same time when the peak power appears due to the propagation delay of PDN. To capture the worst PSN exactly, we take the generated power trace segment as input and use Voltspot [24] to identify the interval including the worst PSN. Then, we back-annotate the interval to the original power trace segment for the PDN stimuli extraction. Consequently, the

In the paper, we use workload and task interchangeably

Since the Voltspot-based PSN simulation is only performed on a single task in this paper, the run time overhead of Voltspot is acceptable.

extracted stimuli are inserted at current source insertion points of the PDN model for PSN calculations, which will be detailed in the next subsection.

4.2 Development of the PDN Model and the PDN Solver

Since we focus on the PSN at the core-level and emphasize the power supply interactions between different cores, it is enough to only consider the global power grid, which takes each core as one block as in [5]. Considering the on-chip PDN, each interconnect segment is modeled with its distributed RLC parasitics. Decoupling capacitance, including intrinsic and external decoupling capacitance, is assumed to be distributed evenly across the core, and connected in parallel with the current source derived from the power trace generated above to the switching activity of the task running on it. Note that both power and ground grids are considered for PSN calculations. Power/ground grids on each layer are interconnected by TSVs, which are modeled as resistors and inductors. C4 bumps distribute on the bottom layer to connect the on-chip PDN to the off-chip PDN. Fig. 8 illustrates the on-chip PDN model [27] while the off-chip model is derived from [28].

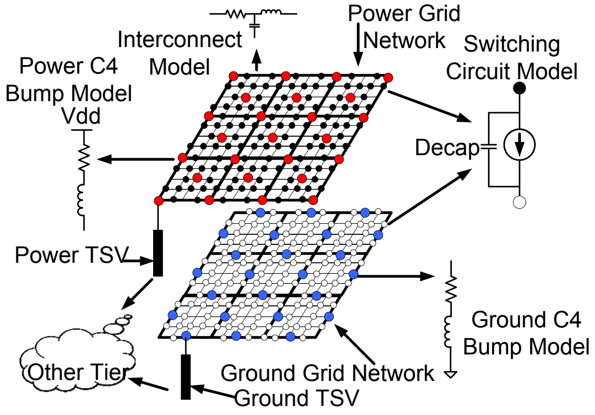
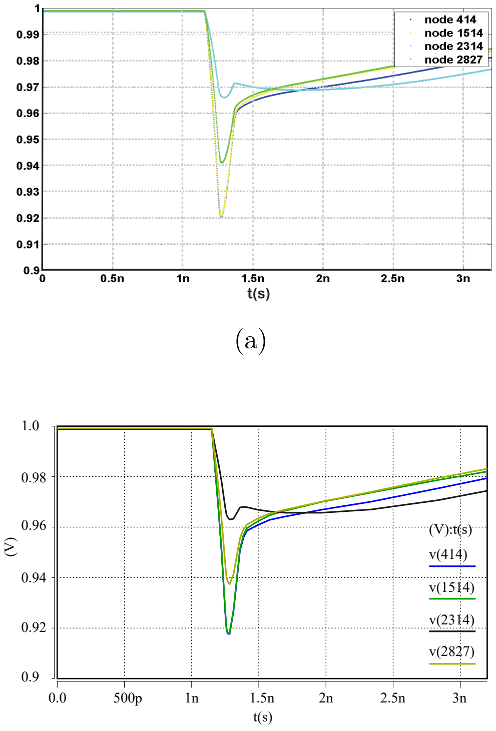


Fig. 8: Illustration of the on-chip PDN model [27].



(a)

(b)

Fig. 9: Simulation result comparisons between our PDN solver and HSPICE simulations on four sample power grid nodes. (a) Simulation results of the PDN solver. (b) HSPICE simulation results.

In contemporary VLSI design, the power grid mesh can easily contain millions of nodes for the PSN calculation. It imposes a great challenge on power grid analysis. As the traditional simulation using HSPICE can no longer be applied for such a very large scale problem, many efficient numerical solving methods have been proposed considering the regularity of the power grid structure, such as multi-grid method [29, 30], preconditioned conjugated gradient method [31].

In order to reduce the simulation complexity, we construct a power grid hierarchy, i.e., the power grid in one core consists of several base grids while each base grid is composed of several base cells as in [5]. Although the PDN model is largely simplified by the hierarchical structure, it would be still very time-consuming for PSN computations in task allocation and scheduling as the scheduling algorithm usually involves many trial-and-fail iterations to obtain the final solution. Therefore, we develop an efficient PDN solver to accelerate PSN analysis based on the modified nodal analysis (MNA).

To verify the effectiveness of the PDN solver, we generate the netlist of a $2 \times 2 \times 2$ 3D MPSoC and feed it into the PDN solver to calculate its pulse response. The simulation results on some selected power grid nodes are shown in Fig. 9. The simulation error of the PDN solver is negligible compared with the HSPICE simulation.

4.3 Problem Formulation

As stated in Section 3, to ensure reliable operations of 3D MPSoCs, we need to consider both thermal and PSN issues during the task scheduling. To clearly formulate the problem, we firstly give 3D MPSoC architecture and task graph definitions as follows,

3D MPSoC Architecture The 3D MPSoC architecture can be described as $AR(m, n, l)$, where l is the layer count, and each layer has $m \times n$ cores. All processing elements (PEs for short) within a layer are interconnected by a 2D mesh Network-on-chip (NoC) structure. PEs on different layers are connected through TSVs, as proposed in [32]. All PEs within the 3D MPSoC share a global power grid, and the power supply is delivered from the bottom layer to upper layers through power supply TSVs, as shown in Fig. 2.

Task Graph Definition The application running on the MPSoC can be split by a set of tasks executing concurrently or in a specified order. As shown in Fig. 3, **S** is the vertex set of task graph $G(S, E)$. S_i denotes task i. Its weight t_i denotes the execution time. If task i is

In the paper, we use tier and layer interchangeably.

a predecessor of task j, then they should satisfy the following constraints, $t_s(j) \geq t_e(i)$, where $t_s(j)$ is task j's start time and $t_e(i)$ is task i's finish time. Additionally, all tasks should meet the deadline constraints, i.e., $t_e(i) \leq d(i)$ where $d(i)$ is the deadline of task i.

Then, the task scheduling problem can be formulated as follows,

$$\begin{aligned}
\text{min.} \quad & \sum_{S_i \in S, p \in P} x_{ip} PSN(p, S_i). \\
\text{s. t.} \quad & \forall S_i \ \sum_{p} x_{ip} = 1, && (1) \\
& t_e(S_i) = t_s(S_i) + t_i), && (2) \\
& t_s(S_i) \geq max_{e_{ji} \in E} \{t_e(S_j)\}, && (3) \\
& t_e(S_i) \leq d_{S_i}, && (4) \\
& t_s(S_i) \geq t_e(S_j), && (5) \\
& p_{ij} + p_{ji} = 1, && (6) \\
& \max_{p \in P} T_p(t) \leq T_0, && (7) \\
& t \leq SL, \\
& \mathbf{G}\mathbf{V}(x) + \mathbf{C}\frac{d\mathbf{V}(x)}{dt} = \mathbf{MAI}, && (8) \\
& x \in \text{power grid nodes}, \\
& PSN(p, S_i) = max|V(x_k, S_i) - V_{dd}|, && (9) \\
& x_k \in \text{core } p.
\end{aligned}$$

where,

$$x_{ip} = \begin{cases} 1 & \text{if task } S_i \text{ is allocated to core } p \\ 0 & \text{otherwise} \end{cases}$$

$$p_{ij} = \begin{cases} 1 & \text{if task } S_i \text{ is scheduled before } S_j \\ & \text{and both of them are allocated} \\ & \text{to the same core} \\ 0 & \text{otherwise} \end{cases}$$

As shown above, our optimization target is to minimize the PSN magnitudes of running cores by task scheduling. (1) means that every task S_i can only be allocated to a single core. S is the task set and P is the core set. (2) derives the finish time of task S_i, where t_i denotes the task i's execution time. (3) is used to guarantee the task precedence during the task scheduling, i.e., a task can only be scheduled after all its predecessors finish execution. (4) guarantees that the deadline constraint can not be violated. (5) and (6) maintain the execution order when two tasks are allocated on the same core. (7) makes sure that the peak temperature of the 3D MPSoC must be lower than the temperature constraint T_0. SL is the task schedule time length. At each schedule point, power supply noise can be calculated by (8) and (9).

In the next subsection, we will propose a

Algorithm 1 PSN and thermal aware task scheduling algorithm

```
procedure pt_schedule(G, spec, PDN_param, thermal_param, PSN_profiles_table)
    // G: task graph, spec: 3D MPSoC specification, PDN_param: PDN parameters
    // thermal_param: thermal parameters, PSN_profiles_table: PSN profiles of each task
    construct_ready_list(&ready_list, G, &task_map); cur_time ← 0
    while ready_list! = NULL do
        ready_list_sort(&ready_list, G);  task ← task_select(ready_list, cur_time)
        for i ← 0, spec.core_count do
            if spec.core[i] = free then
                update_task_map(task.id, i, &task_map)
                if task.finish_time > deadline[task.id] then
                    restore(task.id, i, &task_map);  continue
                else
                    thermal_sim_time ← finish_time(task_map)
                    peak_temp ← thermal_sim(task.id, i, spec.power_table, thermal_param, sim_time)
                    if peak_temp > max_temp then
                        restore(task.id, i, &task_map);  continue
                    else
                        PSN_value ← PSN_eval(task.id, i, PSN_profiles_table, PDN_param)
                        if PSN_value < optimal_value then
                            optimal_value ← PSN_value;  spec.core[i] ← busy;
                            find_solution ← true
                            update_solution(&PSN_schedule_solution, task.id, i, cur_time)
                        else
                            restore(task.id, i, &task_map);  continue
        if find_solution = false && slack = −1 then
            return NULL
        else
            update_ready_list(task.id, i, &G, &task_map, &scheduling_point)
            update_core_status(spec.core, scheduling_point);  cur_time ← scheduling_point
    return PSN_schedule_solution
```

heuristic algorithm to solve the problem effectively.

4.4 Our Proposed Task Scheduling Algorithm

As shown in Algorithm 1, the inputs to the algorithm include the 3D MPSoC specification, current stimuli derived from the power trace extraction, and the task graph. The output is the optimal task schedule. The algorithm is constructed based on the widely-used list scheduling algorithm [33]. First of all, the earliest start time of each task is calculated by ASAP (i.e., as soon as possible) algorithm. The latest start time is calculated by ALAP (i.e., as late as possible) algorithm. Then, all tasks are sorted by their mobilities (i.e., the difference of the latest start time and the earliest start time of the task) in the ascending order such that the task with the least mobility can be scheduled firstly to avoid the violation of the deadline requirement.

At the beginning of the schedule, the first task is put into the ready list. During the schedule, all tasks whose parents finish executions are put into the ready list for scheduling. At each schedule point, ready tasks are assigned to idle cores in an iterative manner. For each assignment trial, the PSNs of all running cores are calculated by the PDN solver mentioned above. At the same time, the peak temperature of each trial is evaluated using Hotspot [21]. As a result, the core incurring the minimum PSN value while meeting the peak temperature constraint is chosen for the task assignment. Since the thermal constant is in the range of milliseconds [34], we use the average power consumption of each task instead of the transient power for the thermal simulation to accelerate the simulation speed. Additionally, as mentioned in [35], significant thermal/PSN fluctuation occurs when there is a new task beginning to run or an old one finishing execution. Therefore, we define the schedule point as the time point when there is any task ending execution or beginning to run, and we only perform the PSN and thermal evaluations at each scheduling point, which reduces the computing overhead further. When the ready list becomes empty, it means all tasks have been scheduled and the optimal schedule can be obtained.

The timing complexity of the proposed algorithm is analyzed as follows. Assume the task graph has S tasks and the 3D MPSoC has $C = l \times m \times n$ cores, where l is the number of tiers, and each tier has $m \times n$ cores. The worst case is that every task has only one parent and only one child. In this case, at each schedule point, the core candidate for assignment is C. For each candidate, we need to perform one thermal simulation and one PSN calculation, whose running time mainly depends on the thermal and power grid sizes. Assume that the base grid size is a constant. Then, the number of thermal and PDN grids depends on the number of tiers and the number of cores on each tier. Therefore, the time complexity of the thermal simulation or the PSN calculation is $O(Cp_0q_0)$. p_0 is the time of one thermal simulation for a single core, and q_0 is the time of one PSN calculation for a single core. In the worst case, we need totally $S \times C$ thermal simulations and PSN calculations to obtain the optimal schedule. As a result, the time complexity of the algorithm is $O(SC^2p_0q_0)$ or $O(SC^2)$ since p_0 and q_0 are constants.

Note that we assume that the task graph to be run on the 3D MPSoC is determined in advance similar to [11, 20]. Therefore, our proposed algorithm can run off-line to derive the optimal task scheduling. Although the iterative optimization procedure involves power supply noise and temperature evaluations, the running time overhead is acceptable due to the linear increase of the time complexity with the number of tasks. Moreover, since the algorithm is off-line, it does not need to make the task assignment decision during the run time, and can guarantee quick scheduling response during the run time.

5 Experimental Results

In this section, we describe the experimental setup firstly and then present the experimental results of the proposed task scheduling algorithm.

Table 3: Task Graphs Used in the Experiments

Benchmark	Task count	Edge Count
auto-indust	24	21
consumer	13	14
networking	15	11
office-automation	5	5
telecomm	34	28
tgff1	23	35
tgff2	16	21
tgff3	18	25
tgff4	21	28
tgff5	17	24
tgff6	26	30
tgff7	22	33
tgff8	18	27

5.1 Experimental Setup

Our proposed task scheduling algorithm is implemented by C++. E3S benchmark suite is adopted in our experiments. E3S benchmarks are extracted from EEMBC benchmark suite and widely used in the task scheduling research [11, 36]. The E3S benchmarks can be classified into five application categories, i.e., automotive, consumer, networking, office automation and telecommunications.

In addition to E3S benchmarks, we also use TGFF [22] to generate eight different hypothetical task graphs suitable for evaluations on the large-scale 3D MPSoC. The specifications of E3S and synthesized benchmarks are shown in Table 3. The first column is the name of the benchmark. The second and the third column denote the task number and the edge count between tasks respectively. Since task power traces used for PSN evaluations are not available from task graph specifications, we take power trace extracted from SPEC2000 benchmarks instead, and different SPEC2000 benchmarks correspond to different tasks. In practice, task power traces could be obtained with the technique described in Section 4.

Table 4: Architecture Parameters of a Single Core of the 3D MPSoCs

CPU	Alpha 21264 2GHz
Predictor	Bimodal predictor, BTB with 2-bit counter
IFQ Size/LSQ Size	4/8
L1 D$/I$	32KB/32KB 64B block size 4-way/1-way associative LRU replacement
Unified L2$	1MB, 64B block size 4-way associative LRU replacement

Table 5: PDN Model Parameters in Our Experiments

Interconnect		TSV	
segment length	200μm	diameter	10μm
segment resistance	48mΩ	aspect ratio	1 : 8
segment capacitance	6.8pF	resistance	20mΩ
segment inductance	196pH	inductance	25pH
C4 Bump		Core	
resistance	9.52mΩ	size(mm)	3.2 × 3.2
inductance	12.65pH	mesh grid	16 × 16

Table 6: Thermal Model Parameters Used for Temperature Evaluations

Bulk Si thickness of bottom die (next to heat sink)	150μm
Bulk Si thickness of other dies	50μm
Cu metal layer thickness	0.42μm
Si thermal conductivity	100.0W/(mK)
Heat sink thermal conductivity	400.0W/(mK)
HotSpot grid resolution	64 × 64
Ambient temperature	27°C

Architecture parameters of the core used for the power trace extraction are listed in Table 4. The extracted power traces are converted to current stimuli corresponding to the running tasks and fed into the PDN solver for PSN calculations. The PDN and TSV parameters used in our PDN model are listed in Table 5. Core size used in our experiments is derived from a 45nm 48-core IA-32 processor [37]. The inter-

PTM interconnect model. http://ptm.asu.edu.

connect parasitics are derived based on 45nm PTM interconnect model. TSV parasitics are obtained from [38]. To evaluate the temperature using Hotspot, it requires to obtain the power trace of the running task. As mentioned in Subsection 4.1, we firstly use the architecture level simulation to get the power trace when a specific task runs on a core. Because the thermal constant lies within the range of several milliseconds which is much larger than the clock cycle time (within nanosecond range), we pick the average power for the thermal simulation. The leakage power of idle cores is also taken into account during the thermal simulation. With these power information and the Hotspot configuration listed in Table 6, we can get the temperature distributions on-chip in each scheduling step.

Two kinds of MPSoCs are used in our evaluation. The first one has two tiers and each tier has 2×2 homogeneous cores. The power consumption of the core is assumed to be 4.6W according to measurements from a prototype of many-core processor [37]. Another one has 3 tiers and each tier has 3×3 homogeneous cores. To verify the effectiveness of our proposed algorithm, we implement a thermal-aware task scheduling algorithm proposed by [11] for comparisons.

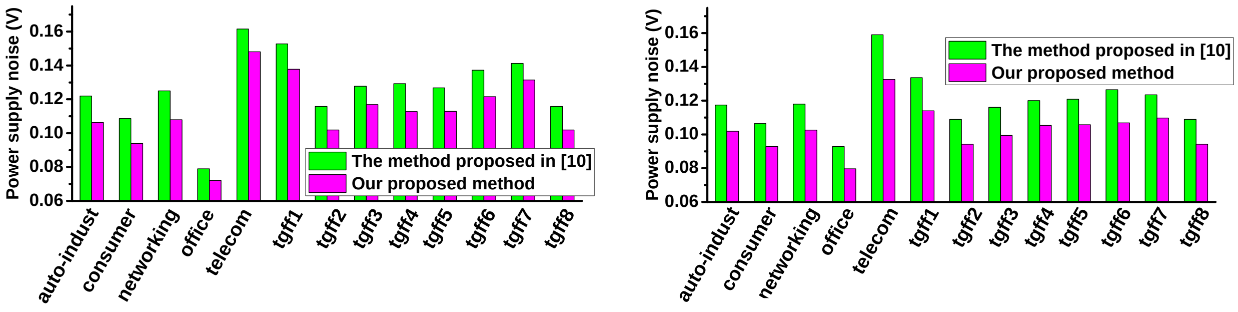
5.2 PSN Reductions of Our Proposed Scheme Compared with the State-of-the-art 3D MPSoC Task Scheduling Algorithm

First, the $2 \times 2 \times 2$ homogeneous MPSoC is considered. During the PSN calculations, the worst case voltage drop during the whole task scheduling procedure among all power grid nodes is chosen for comparison. The temperature constraint is set to 320K. The comparison results are shown in Fig. 10(a).

As shown in Fig. 10(a), different benchmarks have significantly different PSN distributions due to their various switching activities. Our proposed task scheduling algorithm can reduce PSN by 12% on average compared with the task scheduling scheme proposed in [11].

Then, we schedule tasks on the $3 \times 3 \times 3$ MPSoC and the comparison results are shown in Fig. 10(b). The power supply noise magnitudes on the $3 \times 3 \times 3$ MPSoC are generally smaller than those of the $2 \times 2 \times 2$ MPSoC case. It is because more cores are idle during the scheduling procedure and can provide more capacitance to suppress the transient PSN. Our proposed algorithm can reduce as much as 17% power supply noise compared with the work in [11] with the same thermal constraint. It indicates the good scalability of our algorithm.

In the above experiments, we observe that



(a)

(b)

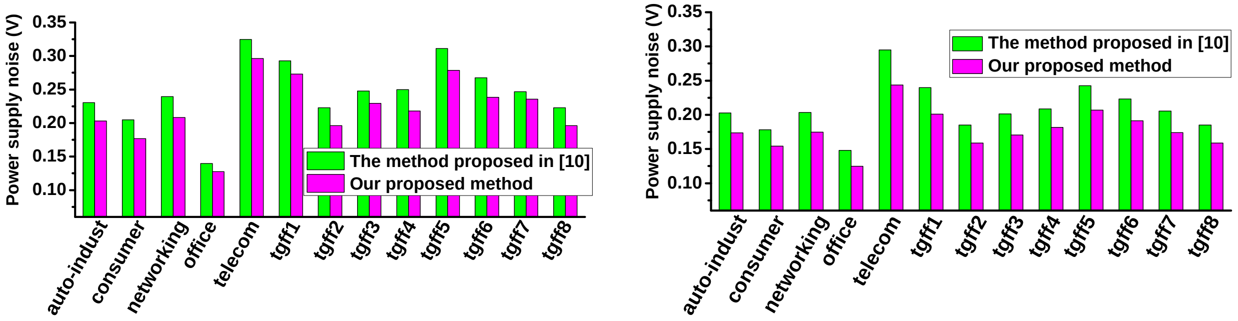
Fig. 10: PSN comparisons of our proposed task scheduling algorithm and the thermal aware task scheduling algorithm [11] given the same thermal constraint. (a) Running tasks on the 2 × 2 × 2 MPSoC. (b) Running tasks on the 3 × 3 × 3 MPSoC.

there are at most four tasks running simultaneously during the task schedule. Considering the peak power of each core is 4.6W in our assumption, the total power consumption is at most 18.4W. To explore the PSN reducing potential of the proposed task scheduling algorithm, we scale the core power by 2X to evaluate the scalability of our proposed technique in terms of the power consumption. Fig. 11(a) and Fig. 11(b) plot PSN comparisons for $2\times2\times2$ and $3\times3\times3$ MPSoC cases respectively. The thermal constraint is still set to 320K. As shown in Fig. 11, increasing core power induces more severe PSN. Compared with [11], our proposed method can reduce PSN by 10.2% for the $2 \times 2 \times 2$ MPSoC case and by 14.8% for the $3 \times 3 \times 3$ MPSoC case.

5.3 Running Performance & Temperature Comparisons

PSN may not only be detrimental to the system reliability but also increase critical path delay variations, which may severely degrade the task running performance. For example, Saint-Laurent and Swaminathan ana-lyzed the relationship between the power supply noise and the clock frequency, and claimed that 63mV PSN variation can slow down clock frequency by 6.7% at 130nm technology node [39]. Therefore, the PSN-aware task scheduling algorithm is beneficial for the task running performance as well. We use the formula proposed by [39] to model the relationship between the average PSN and the critical path delay, i.e.,

$$\frac{D}{D_0} = 1 - k_1 \frac{\Delta V}{V_{dd} - V_t} + k_2 (\frac{\Delta V}{V_{dd} - V_t})^2. \quad (10)$$



(a)

(b)

Fig. 11: PSN comparisons of our proposed task scheduling algorithm and the thermal aware task scheduling algorithm given the same thermal constraint when the core power is doubled. (a) Running tasks on the $2 \times 2 \times 2$ MPSoC. (b) Running tasks on the $3 \times 3 \times 3$ MPSoC.

where V_{dd} is the nominal supply voltage. V_t is the transistor threshold voltage. k_1 and k_2 are process dependent constants. D_0 is the ideal critical path delay.

The critical path delay variations may degrade the processor running frequency and the task execution time. For example, when the critical path delay increases by 20% due to the PSN, the clock frequency would have to be decreased accordingly to prevent logic errors. Therefore, the task execution time will increase. In the experiment, according to the PSN distributions during the task scheduling procedure, the clock frequency when running different tasks can be obtained by Eq. (10). Then, the updated clock frequency is used to derive the task execution time. Fig. 12 illustrates the final completion time when running different task graphs with the thermal-constrained algorithm proposed in [11] and our proposed algorithm assuming the core power is 9.2W.

As shown in Fig. 12, due to the reduced PSN, the task completion time also improves by the proposed task scheduling algorithm. For the $2 \times 2 \times 2$ MPSoC case, the task completion time can be improved by 3.2% on average and 5.5% in maximum. For the $3 \times 3 \times 3$ MPSoC case, the task completion time can be improved by 4.4% on average and 7.8% in maximum. The task completion time of task graphs with 4.6W core power also shows the similar trend and is not plotted due to the lack of space. The above experimental results validate the effectiveness of our proposed algorithm in terms of the PSN reduction and the running task performance improvement.

The peak temperature comparisons caused

Table 7: Peak Temperature Comparisons of the Thermal-Aware Task Scheduling Algorithm and Our Proposed Algorithm (Unit: K)

	$2 \times 2 \times 2$		$3 \times 3 \times 3$	
	Thermal-aware [11]	Our method	Thermal-aware [11]	Our method
auto-indust	309.88	311.36	312.03	316.99
consumer	308.33	310.79	311.2	315.82
networking	309.34	311.58	312.19	316.96
office-automation	306.59	308.71	309.87	314.04
telecomm	313.79	315.08	317.15	320.44
tgff1	313.43	313.87	313.44	318.17
tgff2	310.3	313.87	311.59	315.78
tgff3	311.39	312.68	312.15	316.6
tgff4	309.76	311.75	312.36	317.33
tgff5	312.88	314.31	313.6	318.54
tgff6	311.73	312.39	312.9	317.9
tgff7	311.93	312.13	312.11	316.37
tgff8	310.3	310.56	311.59	315.63

by different task scheduling techniques are shown in Table 7. As shown in the table, both task scheduling methods can meet the 320K peak tempearture constraint. The thermal-aware task scheduling can obtain lower peak temperature while the task scheduling solution derived by our proposed method can achieve an optimal trade-off between temperature and power supply noise.

5.4 Discussion of the Extension to the Hetergeneous 3D MPSoCs

Although we focus on the homogeneous 3D MPSoCs in this work, our proposed method can be easily extended to the heterogeneous case. For the homogeneous case, the task execution time is the same even that it runs on different cores if we do not take PSN effect into account. Therefore, we set the PSN magnitude as the optimization target for homogeneous 3D MPSoCs. Whereas, for the heterogeneous case, the same task can have different power consumptions and execution time on different cores, and the optimization target should be set as the final execution time considering the PSN effect. In each task scheduling step, we need to evaluate the new execution time with the power supply noise consideration. Due to the lack of the space, we take this extension as our future work.

6 Related Work

With the scaling down of power supply voltage, the noise margin reduces remarkably. The signal integrity issue is of a great concern for modern VLSI circuit design. Arabi *et al.* investigated the power supply noise (PSN) impact on performance and reliability of SoCs [40]. The authors observed that the PSN can affect the timing of critical path and the chip reliability. Chen *et al.* proposed a systematic technique to predict the PSN distributions across the chip in the early stage of chip design, and used it to guide the decoupling capacitor insertion [12]. Firouzi *et al.* formulated the PSN estimation as a linear programming problem, and proposed an efficient method to solve it [41]. All the work above explored the PSN calculation from the circuit level. Gupta *et al.* constructed the power delivery network from the architecture level, and obtained voltage variations within CMP when running different applications, and several hazardous activity sequences are identified based on the PSN simulation [28]. Joseph *et al.* proposed a voltage simulation method which used the power trace as stimuli to the PDN model for voltage simulation [42]. Grochowski *et al.* proposed a hardware implementation to accelerate the simulating [43]. Due to TSV parasitics, 3D ICs have some different properties, such as PSN distribu-

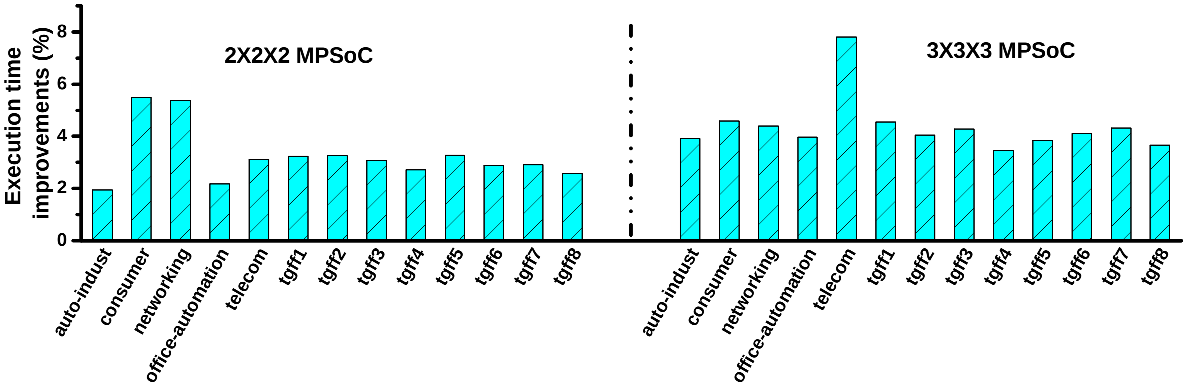


Fig. 12: Task graph completion time improvements of the proposed task scheduling algorithm compared with that of the algorithm proposed in [11] under the same thermal constraint (assume the core power is 9.2W).

tion heterogeneities among layers, vertical PSN coupling, compared with 2D ICs. Huang *et al.* proposed a compact model for 3D power delivery networks analysis [44]. The model has only less than 4% errors compared with HSPICE simulations but with much higher simulation speed. Healy *et al.* explored the TSV topology impact on the power supply noise for 3D ICs [45]. Zhang *et al.* investigated efficient IR drop calculation for 3D ICs [46]. Their proposed method can speed up simulation by 10× to 20× compared with the preconditioned conjugated gradients method. Todri-Sanial *et al.* studied the PDN modeling of 3D ICs with multiple clock domains [47].

As power density increases, chip temperature becomes another important issue affecting the chip reliability. High temperature not only degrades the chip performance, but also makes the material fragile under repeated thermal cyclings [48]. Thermal evaluation and optimization gets much attention recently, especially for 3D IC whose heat removal is more difficult than the 2D counterpart. Huang *et al.* explored thermal modeling for micro-architecture blocks, and developed Hotspot tool for architecture level thermal simulation [21]. Shang *et al.* claimed that on-chip networks heat dissipation can not be ignored either. They proposed a NoC thermal model and the ThermalHerd technique for online thermal management[49]. Coskun *et al.* investigated the thermal scheduling policy for MPSoCs [48]. By combining current temperature profile with past thermal history, the authors proposed a novel OS-level dynamic thermal management heuristic algorithm to reduce performance overhead induced by traditional power/thermal management techniques. Jung *et al.* held the view point that due to thermal measurement errors and varying application characteristics, stochastic-based method can model thermal dissipation more efficiently and effectively compared with previous work [50]. They proposed the dynamic thermal management for multicore system based on Markov decision process to maximize performance under the given temperature constraint. With the emerging of 3D integration technology, heat dissipation becomes a great concern for chip designers and requires more efficient and effective thermal modeling methods. Qian *et al.* proposed an analytical three-dimensional thermal model for 3D ICs considering the TSV effect[51]. Hameed *et al.* adjusted the core activities at different layers according to their distances from the heatsink such that the hotspot will not occur [52]. This method is combined with DVFS to improve the chip performance by run-time adaption with the thermal consideration.

For MPSoCs, task mapping and/or scheduling is another important research topic. Some work focuses on improving the performance under some constraints such as [53, 54, 55] (thermal constraint), [56] (power aware task scheduling). On the other hand, increasing power density inspires the research for energy minimization, such as [57, 58]. Since task mapping/scheduling gets rid of changing the low level hardware design, it can improve the system adaptability for different types of applications with relative low overheads, and will become more important with the prevalence of 3D MPSoCs.

7 Conclusions

As transistor integration density increases continuously, more cores can be fabricated on a single chip to implement more functionalities and approach higher energy efficiency. Moreover, with the emergence of 3D integration technology, many core MPSoCs can be packaged in smaller footprints and achieve higher performance. Although 3D MPSoCs bring huge opportunities for high performance system design, they also have some challenging problems. Among them, power supply noise interactions among different cores and tiers become an imminent issue for consideration during the software-hardware co-design. In the paper, we investigated the PSN optimization of 3D MPSoCs from the task scheduling perspective. To capture PSN accurately and efficiently, we proposed a framework including PDN stimuli extraction based on the architecture level simulation, an efficient PDN solver for PSN calculations and a heuristic algorithm for task scheduling taking both PSN and thermal issues into account. Compared with the state-of-the-art task scheduling algorithm for 3D MPSoCs, our proposed algorithm could reduce PSN by 12% on the $2 \times 2 \times 2$ 3D MPSoC and by 14% on the $3 \times 3 \times 3$ 3D MPSoC. The execution time can also be improved by 5.5% and 7.8% respectively due to the reduced PSN magnitudes. Moreover, the experimental results also showed the good scalability of our proposed algorithm as power consumptions of 3D MPSoCs increase.

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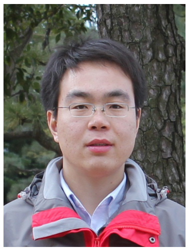

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