Addressing the Thermal Issues of STT-MRAM from Compact Modeling to Design Techniques

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***Abstract*—STT-MRAM (Spin Transfer Torque Magnetic Random Access Memory) possesses many desirable properties such as non-volatility, fast access speed, unlimited endurance and good compatibility with CMOS fabrication process. ITRS has highlighted the potential of STT-MRAM as one of the candidates for the next-generation universal memory technology. However, both the behaviors of the MTJ (Magnetic Tunnel Junction) and the CMOS access transistor, which are two basic elements of STT-MRAM, are generally temperature dependent, threatening the reliability and performance of STT-MRAM under thermal fluctuations. To investigate the reliability and performance of STT-MRAM under the temperature variation, we developed a thermal model for the PMA (Perpendicular Magnetic Anisotropy) MTJ device. With the developed model, thermal behaviors and performance of the hybrid MTJ/CMOS circuits can be characterized and thermal optimization techniques can then be studied. Afterward, a thermal-aware sensing circuit is proposed as a case study to exploit the thermal characteristics for improving STT-MRAM read reliability under the temperature variations. Our experimental results show that the proposed sensing circuit can markedly reduce the read error rate under thermal fluctuations compared with the state-of-the-art designs.**

***Index Terms*—Magnetic tunnel junction (MTJ), read reliability, sensing circuit, STT-MRAM, thermal fluctuations.**

I. Introduction

As process technology continuously shrinks, the power wall issue has become one of the most significant bottlenecks for integrated circuits [1, 2]. Especially, the leakage power consumption occupies as much as half of the total power budget in a contemporary computing system [3]. To address this problem, spintronics emerges and its related nonvolatile memory has achieved a success in the past few years, e.g., toggle MRAM in 2006 and STT-MRAM in 2012 [4-6]. Recently, STT-MRAM has even been suggested as one of the most promising candidates for the next-generation universal memory technologies by ITRS [7].

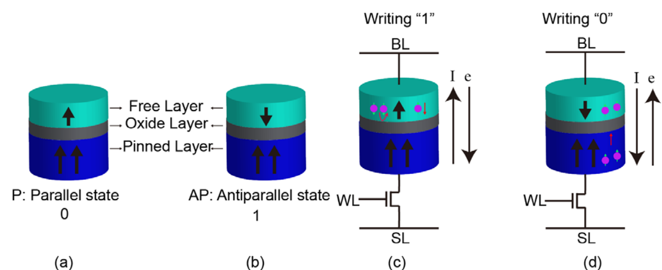

Fig. 1. The basic cell structure of STT-MRAM. (a) MTJ in parallel (low resistance) state; and (b) in antiparallel (high resistance) state, respectively; (c) writing "1" operation: from the parallel state to antiparallel state, and (d) writing "0" operation: from the antiparallel state to parallel state.

Although promising, process, voltage and temperature (PVT) variations severely affect the reliability and performance of STT-MRAM as technology downscales [8]. Until now, lots of attempts have been done to address the process and voltage variations on STT-MRAM [9-12], the impact of the temperature variation or thermal fluctuation, however, has not yet been comprehensively studied. Based on our investigations, when the temperature varies, the switching current and the TMR (Tunnel magneto-resistance) ratio of the MTJ device as well as the driving capability of the CMOS access transistor fluctuate accordingly, resulting in performance and reliability degradations of STT-MRAM. To investigate the thermal reliability and performance of STT-MRAM under the temperature variation, this paper developed a thermal model of the MTJ device. With the proposed MTJ thermal model, the behaviors of the hybrid MTJ/CMOS circuit under the temperature variations can then be characterized and the corresponding thermal optimization techniques can be studied. Afterward, a thermal-aware sensing circuit is proposed as a case study to exploit the thermal characteristics for improving STT-MRAM read reliability under the temperature variations.

The rest of this paper is organized as follows. Section II introduces the thermal issues of STT-MRAM, and Section III models the thermal behaviors of MTJ. A thermal-aware sensing circuit is proposed and discussed in Section IV. Finally, Section V concludes this paper.

II. Thermal Issues of STT-MRAM

The typical cell structure of STT-MRAM consists of one transistor and one MTJ (1T1MTJ) connected in series as

This work was supported part by the Innovation Foundation of BUAA for PhD Graduates, National Natural Science Foundation of China (NSFC) under grant No. 61501013 and No. 61401008, Beijing Natural Science Foundation under grant No. 4154076 and EU H2020 CONNECT grant agreement No. 688612. (Liuyang Zhang and Yuanqing Cheng contributed equally to this work. Corresponding author: Weisheng Zhao and Aida Todri-Sanial)

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TABLE I
PHYSICAL PARAMETERS OF THE MTJ DEVICE

Parameters	Description	Value
E	energy barrier	1.54 eV
Δ	thermal stability factor	~60 k_BT @300 K
t_{ox}	the thickness of the oxide layer	0.85 nm
t_{sl}	the thickness of the free layer	1.3 nm
k_B	Boltzmann constant	$8.625 \cdot 10^{-5}$ eV/K
M_S	saturation magnetization	2200 Oe
H_K	magnetic anisotropy field	17200 Oe
area	cross section area of MTJ	$40 \cdot 40 \cdot \pi/4$ nm^2
V_{sl}	the volume of the free layer	area$\cdot t_{sl}$
$TMR(0)$	tunnel magnetoresistance ratio of MTJ	300%
T_0	ambient temperature	300 K
P_0	spin polarization percentage	0.52

shown in Fig. 1. The MTJ in the cell is considered as the storage element, while the transistor works as a switch to control the access condition of the cell. It also provides the bi-directional driving current to write data into or read data out from the memory cell. Due to the temperature fluctuations, failures may occur in STT-MRAM. These failures can be classified into three types: writing operation error, reading operation error and retention error.

Writing operation error. When writing data "1" or "0" into the cell, a negative or a positive voltage is applied to the cell as shown in Fig. 1(c) and (d) respectively. Writing errors may occur if the writing current amplitude is insufficient or (and) the pulse width is not long enough [13]. Generally, the writing pulse width for a memory chip is fixed, writing errors mostly result from the declined driving ability of the transistor under the temperature fluctuations [14].

Reading operation error. Reading error commonly has two categories, including sensing error and read disturbance. In general, a relatively larger sensing current is preferred to improve sensing margin [15]. On the other hand, the sensing current should be much lower than the switching current of MTJ to avoid the read disturbance during the reading "1" operation. Particularly, both the sensing current and switching current of MTJ varies under the temperature fluctuations, increasing the read reliability challenges. In practice, writing operation error can be robustly tackled by providing a sufficient writing current with high amplitude or (and) long pulse width. Reading operation error, however, cannot be effectively resolved in a similar way, owing to the intrinsic trade-off between sensing error and read disturbance [16]. Therefore, this paper focuses on the read reliability under the temperature fluctuations.

Retention error. Retention error, which depends mainly on the thermal stability factor, refers to the accidental MTJ flipping during the idle state. Unfortunately, the thermal stability factor decreases with respect to the temperature, adding challenges on STT-MRAM reliability under the temperature fluctuations.

Both MTJ and transistor are temperature dependent devices. The writing, reading and retention conditions of STT-MRAM change due to the temperature variations. Until now, the thermal property of a transistor has been investigated thoroughly. This paper focuses on the thermal behaviors of the MTJ device. There are many works on studying the switching behaviors of MTJ device under the temperature variations, but an electrical model capturing the thermal properties of the MTJ device is still missing for circuit design and evaluation [17, 18]. In this paper, we first present a compact MTJ model that includes the thermal properties. Then, a thermal-aware sensing circuit is proposed to tackle the reading operation issues in STT-MRAM.

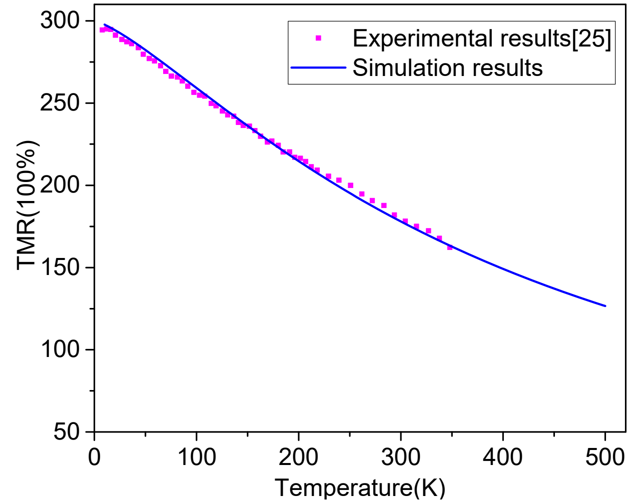

Fig. 2. TMR under the temperature variations, which is drew with (5). The magenta points are experimental results, and the blue line is the simulation results derived by the proposed model. It fits well with the experimental results in the specified temperature range.

III. THERMAL MODELING OF MTJ

Both the critical switching current and TMR are temperature dependent [19, 20]. A compact model that describes the thermal behaviors of the critical switching current and TMR of a PMA (Perpendicular Magnetic Anisotropy) MTJ device is developed. Physical parameters of the MTJ used in this work are shown in Table I.

A. TMR Temperature Dependency

The TMR, defined as $TMR = (R_H - R_L)/R_L$, indicates the resistance difference between the antiparallel and the parallel states of an MTJ. Many experimental results have shown that the high resistance R_H depends on the temperature; however, the low resistance R_L almost keeps constant under the temperature fluctuations [21]. According to Shang's model [21], the conductance of an MTJ is expressed as follows,

$$G(\theta) = G_T[1 + \cos\theta \cdot P_1 P_2] + G_{SI} \quad (1)$$

The first term represents the spin dependent part, and G_{SI} is the spin independent part ($\sim T^{1.35\pm0.15}$) of the conductance. θ is the angle between the magnetization directions of the free layer and that of the pinned layer (θ=0° or 180° for parallel or antiparallel state respectively). $G_T = G_0 \omega T / \sin(\omega T)$ is the

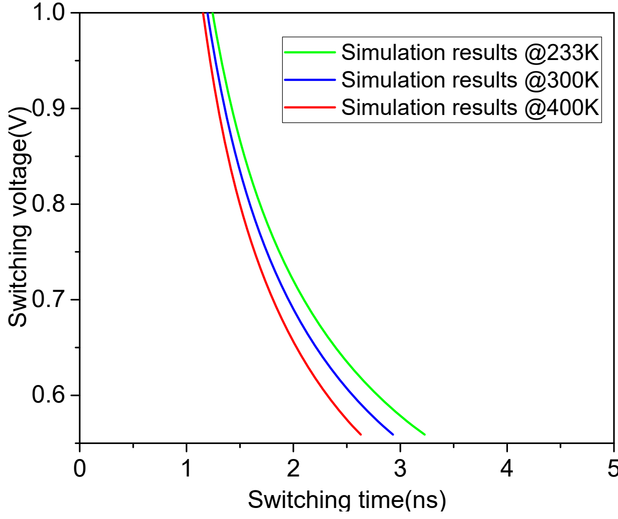

Fig. 3. The switching time of MTJ in the precessional regime under different switching voltage and temperatures. It shows that large voltage and high temperature help MTJ switch.

prefactor for direct elastic tunneling. G_0 is a constant, and $\omega = 1.387\times10^{-4} t_{ox}/\sqrt{E}$. t_{ox} is the thickness of the oxide layer and E is the energy barrier of MTJ, P_1 and P_2 (P_1 usually equals to P_2) are the spin polarization percentages of the free layer and the pinned layer respectively.

According to [22], the temperature dependence of the spin polarization percentage P dominates the variation of the high resistance R_H of an MTJ. With the temperature increasing, the spin polarization percentage P of an MTJs' ferromagnetic layers (both the free layer and pinned layer) decreases. It can be described by (2) [22, 23].

$$P(T) = P_0(1-\beta T^{\alpha}) \tag{2}$$

In (2), P_0 is the spin polarization percentage of an MTJ at room temperature. α and β are parameters, which are related to the material and magnetic anisotropy of an MTJ, equal to 1.04 and 2.07×10^{-5} respectively in this model. Spin-flip scattering was proposed to explain the temperature dependence of the spin polarization percentage [24].

The TMR ratio of an MTJ without biasing voltage could be described by the following equation.

$$TMR(T) = \frac{2P_1P_2(1-\beta T^{\alpha})^2}{1-P_1P_2(1-\beta T^{\alpha})^2 + G_{SI}/G_T} \tag{3}$$

Then under a biasing voltage, it can be expressed by [22],

$$TMR(V) = \frac{TMR(0)}{1+V^2/V_h^2} = \frac{2P_1P_2/(1-P_1P_2)}{1+V^2/V_h^2} \tag{4}$$

where $TMR(0)$ is the TMR without biasing voltage at room temperature, V is the bias voltage on MTJ, V_h equals to 0. 5V. The product of P_1 and P_2 can be expressed by $TMR(0)$ as, $P_1P_2 = TMR(0)/[TMR(0)+2]$. Therefore, combining the (3) and (4), the TMR ratio under the temperature variations and biasing voltage can be expressed by (5),

$$TMR(T,V) = \frac{\dfrac{2(1-\beta T^{\alpha})^2 TMR(0)}{TMR(0)\left[1-(1-\beta T^{\alpha})^2\right]+[1+TMR(0)]G_{SI}/G_T+2}}{1+V^2/V_h^2} \tag{5}$$

Fig. 2 shows the temperature-dependent TMR ratio of an MTJ derived from the above equation, which is consistent with the experimental results [25].

B. Switching Current and Switching Time

According to the switching time, the magnetization dynamics of an MTJ can be classified into two regimes: precessional switching regime and thermal activated switching regime [26-28]. In the follows, we will study the switching behaviors of MTJ under the temperature variations and model them in the precessional regime.

The magnetization switching dynamics of an MTJ is dominated by the spin polarized current flowing through it, and also impacted by the temperature. The critical current I_C, which is defined as the smallest current to switch the MTJ state. In the precessional switching regime, the amplitude of the required switching current is generally larger than that of the critical current, and the switching time is then less than 10 ns. Because the spin polarization efficiency factor g and TMR ratio depend on the temperature, (6) can be obtained by replacing g with $g(T)$ in Sun model [29], which depends on the temperature and is calculated with (8). In the precessional regime, the switching current and the switching time under the temperature variations can be calculated with (6) and (7) respectively [26].

$$I_C = \alpha\frac{\gamma e}{\mu_B g(T)}\mu_0 M_S H_K V_{sl} = 2\alpha\frac{\gamma e E}{\mu_B g(T)} \tag{6}$$

$$\tau^{-1} = \frac{1}{\tau_0 \ln(\pi/2\theta_0)}\cdot\left(\frac{I}{\lambda I_C}-1\right) \tag{7}$$

$$g(T) = \frac{\sqrt{TMR(T,V)(TMR(T,V)+2)}}{[2(TMR(T,V)+1)]} \tag{8}$$

Here, α is the Gilbert damping coefficient, γ is the gyromagnetic ratio, e is the electron charge, μ_B is Bohr magneton. μ_0 is the permeability of free space, M_S is the saturation magnetization of MTJs' ferromagnetic layers, H_K is the magnetic anisotropy field, V_{sl} is the volume of free layer and E is the energy barrier. θ_0 is the initial angle of the magnetization direction of the free layer, which is thermally distributed and can be calculated by $\sqrt{k_BT/2E}$ [30]. τ_0~1.0 ns is the relaxation time, and λ is a coefficient λ=0.2333 , I is the writing current. As can be seen, when the temperature elevates, θ_0 increases, providing a larger spin torque to help MTJ

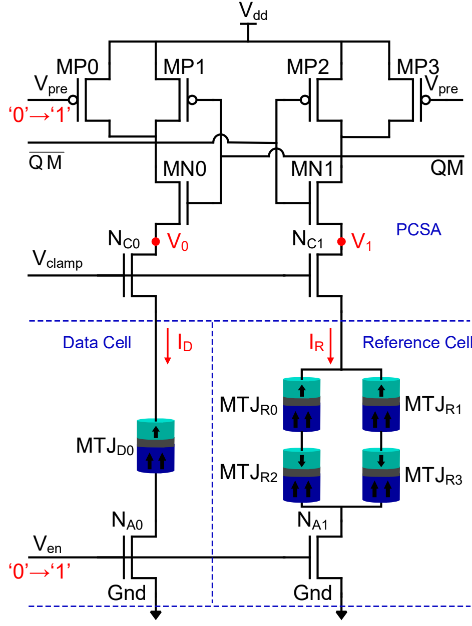

Fig. 4. The circuit of pre-charge sensing amplifier, data cell and reference cell. The resistance of the data cell branch is less than that of the reference cell. When V_{pre} and V_{en} are set to '1' from '0', and V_{clamp} is enabled, the discharge current I_D is larger than I_R. $\overline{QM}$ will decline faster than QM. As $\overline{QM}$ reaches the threshold voltage of inverter, $\overline{QM}$ will discharge to '0', and QM increases to '1'.

magnetization switching [29]. In this case, MTJ switching time reduces under a high temperature, which has been experimentally verified [28, 31]. Fig. 3 shows the simulation results with the thermal model in the precessional regime.

IV. STT-MRAM Sensing Circuit Design Under the Temperature Fluctuations

As discussed above, the read reliability is heavily affected by thermal variations. In this section, we present a thermal-aware sensing circuit to effectively tackle this problem.

A. PCSA and Its Temperature Dependences

Fig. 4 shows the schematic of a typical sensing circuit of STT-MRAM, named pre-charge-sensing amplifier (PCSA) [32], which is composed of two inverters (MP1, MN0 and MP2, MN1), two PMOS transistors (MP0, MP3) in parallel with MP1 and MP2 respectively. N_{C0} and N_{C1} work as the clamp transistors, N_{A0} and N_{A1} are the accessing transistors of the data cell and the reference cell respectively. The sensing procedure is as follows: V_{pre} and V_{en} are first set to "0", and V_{clamp} is set to "0", the drain terminals of N_{C0} and N_{C1} are pre-charged to V_0 and V_1 respectively without any standby currents in the circuit as N_{C0} and N_{C1} are closed. As V_{pre} and V_{en} are set to "1" from "0", and V_{clamp} is enabled, the pre-charged voltages start to discharge. The discharge speeds are different between the data cell branch and the reference cell branch due to their different resistances. In Fig. 4, the resistance of MTJ_{D0} in the parallel state is less than that of the reference cell. Therefore, the current flowing through the data cell branch is larger than that of the reference cell (I_D > I_R),

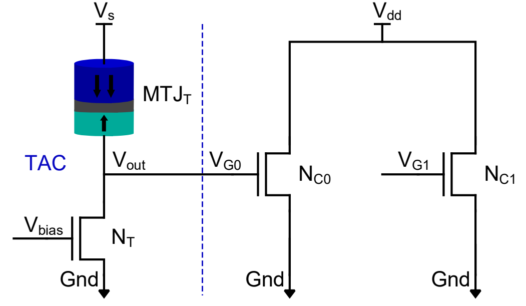

Fig. 5. The schematic of TAC. The left part is TAC, and the right part is designed for comparative experiments. The MTJ MTJ_T in TAC is configured as antiparallel state in case of being switched, while the NMOS N_T works in the saturation region. Thus, a thermal-aware output voltage V_{out} is obtained. The amplitude of V_{out} can be tuned by adjusting V_s and V_{bias}. When the temperature increases, the current of NMOS declines. However, the current of N_{C0} can be compensated by V_{out}, which increases with the temperature, while the current of N_{C1} reduces due to the fixed gate voltage V_{G1}. Experiment results are shown in Fig. 6, Fig. 7 and Fig. 8.

$\overline{QM}$ will decline faster than QM. When $\overline{QM}$ is lower than the threshold voltage of inverter, the two inverters will reach at a stable state ($\overline{QM}$ = '0', QM = '1'). Thus, the sense amplifier can amplify the difference to a full-swing voltage output, and data stored in the data cell is sensed out.

In PCSA, sensing margin is computed by the resistance difference of the data cell and the reference cell, and can be reflected by the amplitude of currents I_D and I_R. Therefore, the sensing margin of the PCSA circuit can be calculated by (9).

$$I_{SM}(T) = \left| I_D(T) - I_R(T) \right| \tag{9}$$

$$I_D(T) = \frac{V_{clamp}}{R_{MTJ}(T) + R_{N_{A0}}} \tag{10}$$

$$I_R(T) = \frac{V_{clamp}}{0.5 \times (R_{P_MTJ} + R_{AP_MTJ}(T)) + R_{N_{A1}}} \tag{11}$$

It is found that the sensing margins are inversely proportional to the temperature by calculating them. The reading operation error rate is determined by the amplitude of the sensing margin. Larger sensing margin is preferred to obtain lower reading operation error rate. In order to increase the sensing margin when the temperature increases, one practicable way is to increase the sensing current. Increasing transistor channel width can increase sensing current, but its amplitude cannot be tuned automatically under the temperature fluctuation, and will seriously result in read disturbance when sensing "1" if sensing current is too large. Therefore, it is critical and beneficial to compensate sensing current automatically in high temperature without aggravating read disturbance. In the follows, it provides a thermal-aware circuit to control the gate voltage of NMOS transistor, and then automatically compensate the sensing current loss.

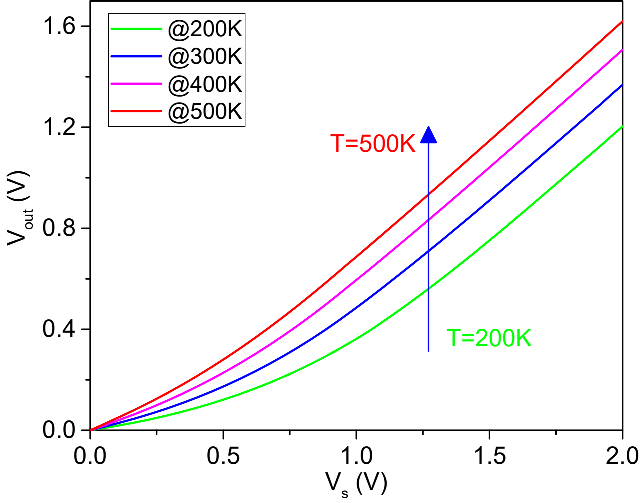

Fig. 6. The output voltages of TAC circuit under different voltage supplies and temperatures. The voltage elevates with the temperature, which is used to tune the gate voltage of N_{C0} automatically.

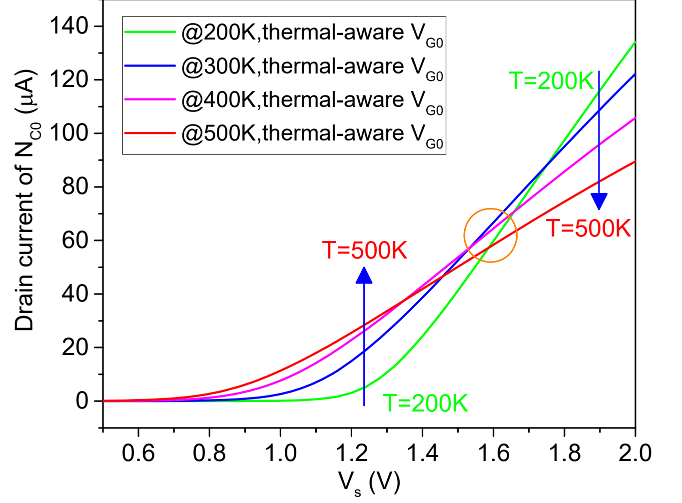

Fig. 7. The drain current of N_{C0} under different V_s and the temperature variations. The drain current increases with the temperature before the brown circle, but decreases after it.

TABLE II
CONFIGURATION OF THE TAC CIRCUIT

Parameters	Description	Value
MTJ_T	the MTJ used in TAC	Antiparallel
TMR	tunnel magnetoresistance ratio of MTJ_T	200%
V_{bias}	voltage bias of N_T	1.2V
V_{dd}	drain potential of both N_{C0} and N_{C1}	1.0V
W_{NMOS}	the channel width of NMOS used in TAC	240nm
L_{NMOS}	the channel length of NMOS used in TAC	45nm

B. Proposed Thermal-aware Circuit (TAC)

Fig. 5 shows the schematic of the proposed thermal-aware circuit, which comprises an MTJ (MTJ_T) in the antiparallel state and an NMOS transistor (N_T), V_{out} is the output of this TAC. The circuit is configured with the parameters listed in Table II. As indicated in the last section, the resistance of MTJ_T in the antiparallel state reduces with the temperature, while that of N_T has the contrary thermal property. Therefore, the output V_{out} is thermal-aware and increases with the temperature, it can be calculated with (12). The corresponding simulation results are shown in Fig. 6.

$$V_{out}(T) = V_s \times \frac{R_{N_T}(T)}{R_{MTJ_T}(T) + R_{N_T}(T)} \tag{12}$$

The right part in Fig. 5 is used to carry out the comparative experiments. The simulation results are shown in Fig. 7 and Fig. 8. The gate of N_{C0} is controlled by V_{out}, while that of N_{C1} connects to the fixed voltage V_{G1}. As indicated in Fig. 8, the drain current of N_{C1} declines with the temperature as expected. In Fig. 7, the drain current of N_{C0} has few variations around Vs=1.6V. This region can be used to compensate for the current loss of NMOS resulted from the temperature variations, which is specified by a brown circle. Before the region, N_{C0} is overcompensated, its drain current increases as the

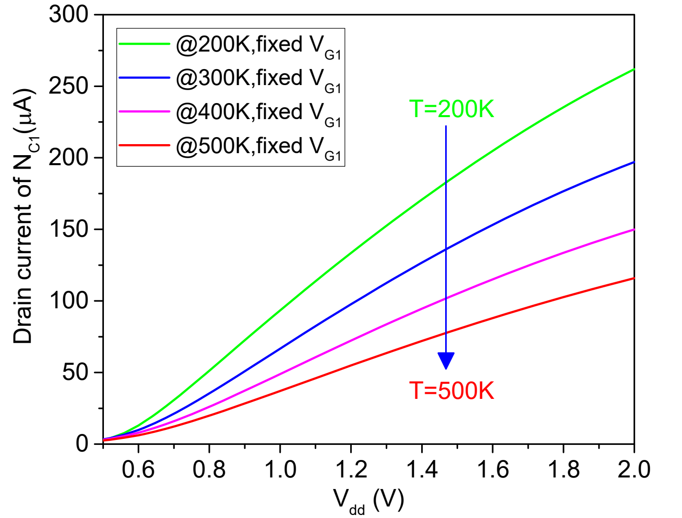

Fig. 8. The drain current of N_{C1} under different V_{dd} and the temperature variations. The drain current declines with the temperature.

temperature; while the current of N_{C0} is undercompensated after the region. The amplitude of the output current meets the requirement for reading the MTJ. The lower or higher drain current of N_{C0} can be reached by tuning V_s and V_{bias} in the circuit. With this knowledge, the sensing amplifier shown in subsection A will be adapted to work better under the temperature fluctuation as illustrated in the next subsection.

C. Proposed Thermal-aware Sensing Amplifier (TASA)

Based on the proposed TAC, the PCSA in subsection A will be adopted to enhance its reliability under the temperature variations in this subsection.

In PCSA, the reading error rate increases due to insufficient sensing current in the high temperature. The

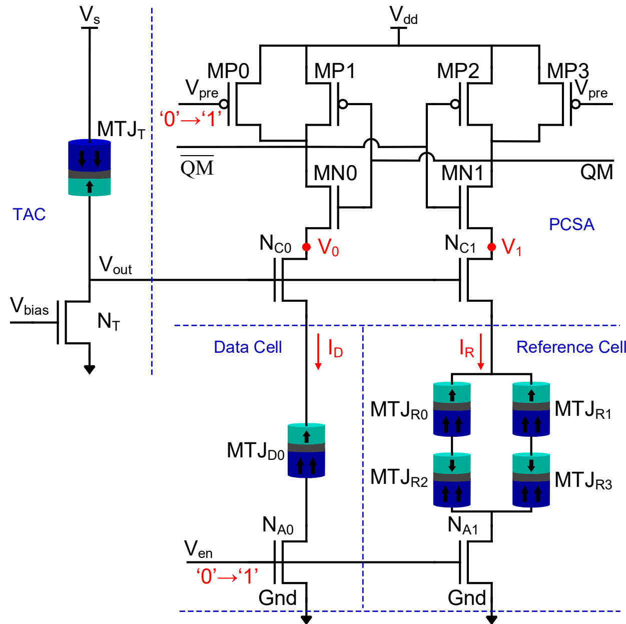

Fig. 9. The schematic of TASA, data cell and reference cell. The upper part is TASA, which comprises TAC and the adopted PCSA; the left side is the data cell, and the reference cell is in the other side of bottom parts. While sensing, the discharge current will be compensated by the thermal-aware V_{out} of TAC, which helps to enhance the reading reliability.

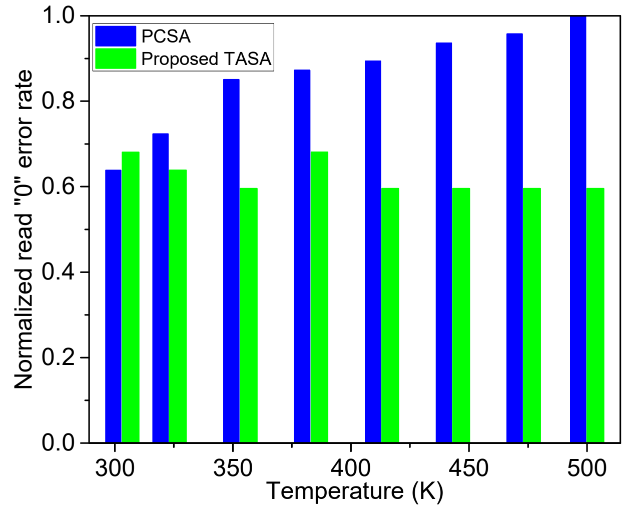

Fig. 10. Reading "0" error rates of STT-MRAM under the temperature variations. The error rates increases with PCSA, but it almost keeps constant with TASA when the temperature elevated, which has the biggest error rate reduction (almost 40%) in 500K.

currents cannot be however increased simply by enlarging the channel width of transistors, which may result in read disturbance when reading "1". Note that N_{C0} and N_{C1} in Fig. 4 are transistors to clamp the voltage for reading data cell, this voltage can be changed by adjusting the gate voltage of N_{C0} and N_{C1}. With this idea, PCSA is adopted with the gate voltage of N_{C0} and N_{C1}, which are tuned by V_{out} of TAC. Thus, the TASA is proposed to harden the reading reliability.

TABLE III
THE CONFIGURATION OF TASA

Parameters	Description	Value
MTJ_{D0}	the MTJ in data cell	Parallel
MTJ_T	the MTJ in TAC	Antiparallel
TMR	tunnel magnetoresistance ratio of MTJ	200%
V_{bias}	voltage bias of N_T	1.2V
V_s	voltage source applied to thermal-aware circuit	1.5V
V_{dd}	voltage source applied to TASA	1.2V
V_{pre}	gate voltage of P1 and P4	1.2V
W_{NMOS}	the channel width of the transistor used in TASA	240nm
L_{NMOS}	the channel length of the transistor used in TASA	45nm

The schematic of TASA is shown in Fig. 9, which comprises two parts. In the upside, the left part is TAC, and the right part is different from PCSA. It has two clamp transistors with their gate voltage controlled by V_{out} of TAC. The data cell connects to the left branch of PCSA, while the reference cell connects to the right branch in the bottom of the circuit. As the sensing procedure indicated in subsection A, the resistance difference between the data cell and the reference cell is distinguished by measuring the amplitude of discharge currents with PCSA. The currents that decrease with the temperature in PCSA, however, can be compensated automatically in TASA. Therefore, the sensing amplifier has almost the same sensing margin as that at room temperature even under high temperatures. Reading "0" operation will be taken out as a case to exploit the thermal characteristics for improving STT-MRAM read reliability under the temperature variations in follows.

With the configuration in Table III, we use Cadence environment to study reading error rate of STT-MRAM with TASA and PCSA. The Monte Carlo simulation results are shown in Fig. 10.

As can be seen, the reading operation error rates with PCSA increase with the temperature varying from 300K to 500K. However, the reading operation error rates with TASA almost keep a constant under the temperature variations. The largest reduction of reading operation error rates is about 40% when the temperature rises to 500K. These results validate the thermal variation tolerance capability of the proposed TASA. Afterward, a suitable ECC (Error Correction Code) solution can be adopted to further reduce the BER (Bit Error Rate)[33].

V. CONCLUSION

In this paper, we look into the thermal behaviors of STT-MRAM and model them into a 40nm Verilog-A based PMA MTJ SPICE model. Afterward, by analyzing the reading operation failure mechanism of STT-MRAM under the temperature variations, we propose further a thermal-aware sensing amplifier (TASA) design to deal with this problem. At last, the effectiveness of TASA is evaluated by Monte-Carlo simulations in comparison with conventional sensing circuit.

REFERENCES

[1] Y. Huai, "Spin-transfer torque MRAM (STT-MRAM): Challenges and prospects," *AAPPS Bulletin,* vol. 18, no. 6, pp. 33-40, Dec. 2008.

[2] N. S. Kim, T. Austin, D. Baauw *et al.*, “Leakage current: Moore's law meets static power,” *Computer,* vol. 36, no. 12, pp. 68-75, Dec. 2003.

[3] W. Zhao, and G. Prenat, *Spintronics-based computing*, Switzerland: Springer, 2015.

[4] S. A. Wolf, D. D. Awschalom, R. A. Buhrman *et al.*, “Spintronics: a spin-based electronics vision for the future,” *Science,* vol. 294, no. 5546, pp. 1488-1495, Nov. 2001.

[5] H.-S. P. Wong, and S. Salahuddin, “Memory leads the way to better computing,” *Nature nanotechnology,* vol. 10, no. 3, pp. 191-194, Mar. 2015.

[6] W. Kang, Y. Zhang, Z. Wang *et al.*, “Spintronics: emerging ultra-low-power circuits and systems beyond MOS technology,” *ACM Journal on Emerging Technologies in Computing Systems (JETC),* vol. 12, no. 2, pp. 16, Aug. 2015.

[7] L. Wilson, “International technology roadmap for semiconductors (ITRS),” *Semiconductor Industry Association*, 2013.

[8] H. Cai, H. Petit, and J. F. Naviner, “Reliability aware design of low power continuous-time sigma–delta modulator,” *Microelectronics Reliability,* vol. 51, no. 9–11, pp. 1449-1453, Sep. 2011.

[9] W. Kang, L. Zhang, J.-O. Klein *et al.*, “Reconfigurable codesign of STT-MRAM under process variations in deeply scaled technology,” *IEEE Transactions on Electron Devices,* vol. 62, no. 6, pp. 1769-1777, Jun. 2015.

[10] Y. Zhang, X. Wang, H. Li *et al.*, “STT-RAM cell optimization considering MTJ and CMOS variations,” *IEEE Transactions on Magnetics,* vol. 47, no. 10, pp. 2962-2965, Sep. 2011.

[11] H. Cai, Y. Wang, W. Zhao *et al.*, “Multiplexing sense-amplifier-based magnetic flip-flop in a 28-nm FDSOI technology,” *IEEE Transactions on Nanotechnology,* vol. 14, no. 4, pp. 761-767, Jul. 2015.

[12] A. Aziz, and S. K. Gupta, “Hybrid multiplexing (HYM) for read- and area-optimized MRAMs with separate read-write paths,” *IEEE Transactions on Nanotechnology,* vol. 15, no. 3, pp. 473-483, May 2016.

[13] L. Zhang, A. Todri-Sanial, W. Kang *et al.*, “Quantitative evaluation of reliability and performance for STT-MRAM,” in *IEEE International Symposium on Circuits and Systems 2016*, 2016, pp. 1150-1153.

[14] D. Lee, and K. Roy, “Energy-delay optimization of the STT MRAM write operation under process variations,” *IEEE Transactions on Nanotechnology,* vol. 13, no. 4, pp. 714-723, Jul. 2014.

[15] X. Fong, S. H. Choday, and K. Roy, “Bit-cell level optimization for non-volatile memories using magnetic tunnel junctions and spin-transfer torque switching,” *IEEE Transactions on Nanotechnology,* vol. 11, no. 1, pp. 172-181, Jan. 2012.

[16] W. Kang, Z. Li, J. O. Klein *et al.*, “Variation-tolerant and disturbance-free sensing circuit for deep nanometer STT-MRAM,” *IEEE Transactions on Nanotechnology,* vol. 13, no. 6, pp. 1088-1092, Nov. 2014.

[17] C. J. Lin, S. H. Kang, Y. J. Wang *et al.*, “45nm low power CMOS logic compatible embedded STT MRAM utilizing a reverse-connection 1T/1MTJ cell,” in *2009 IEEE International Electron Devices Meeting (IEDM)*, 2009, pp. 1-4.

[18] B. Wu, Y. Q. Cheng, J. L. Yang *et al.*, “Temperature impact analysis and access reliability enhancement for 1T1MTJ STT-RAM,” *IEEE Transactions on Reliability*, vol. 65, no. 4, pp. 1755-1768, Dec. 2016.

[19] L. Zhang, Y. Cheng, W. Kang *et al.*, “Reliability and performance evaluation for STT-MRAM under temperature variation,” in *2016 17th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, 2016, pp. 1-4.

[20] X. Y. Bi, H. Li, and X. B. Wang, “STT-RAM cell design considering CMOS and MTJ temperature dependence,” *IEEE Transactions on Magnetics*, vol. 48, no. 11, pp. 3821-3824, Nov. 2012.

[21] X. Liu, D. Mazumdar, W. Shen *et al.*, “Thermal stability of magnetic tunneling junctions with MgO barriers for high temperature spintronics,” *Applied Physics Letters*, vol. 89, no. 2, pp. 023504, Jul. 2006.

[22] C. H. Shang, J. Nowak, R. Jansen *et al.*, “Temperature dependence of magnetoresistance and surface magnetization in ferromagnetic tunnel junctions,” *Physical Review B*, vol. 58, no. 6, pp. R2917, Aug. 1998.

[23] X. Kou, J. Schmalhorst, A. Thomas *et al.*, “Temperature dependence of the resistance of magnetic tunnel junctions with MgO barrier,” *Applied Physics Letters*, vol. 88, no. 21, pp. 212115, May 2006.

[24] F. Guinea, “Spin-flip scattering in magnetic junctions,” *Physical Review B*, vol. 58, no. 14, pp. 9212, Oct. 1998.

[25] V. Drewello, J. Schmalhorst, A. Thomas *et al.*, “Evidence for strong magnon contribution to the TMR temperature dependence in MgO based tunnel junctions,” *Physical Review B*, vol. 77, no. 1, pp. 014440, Jan. 2008.

[26] T. Aoki, Y. Ando, D. Watanabe *et al.*, “Spin transfer switching in the nanosecond regime for CoFeB/MgO/CoFeB ferromagnetic tunnel junctions,” *Journal of Applied Physics*, vol. 103, no. 10, pp. 103911, Mar. 2008.

[27] D. Apalkov, M. Pakala, and Y. Huai, “Micromagnetic simulation of spin transfer torque switching by nanosecond current pulses,” *Journal of Applied Physics*, vol. 99, no. 8, pp. 08B907, Apr. 2006.

[28] H. Zhao, P. K. Amiri, Y. Zhang *et al.*, “Spin-transfer torque switching above ambient temperature,” *IEEE Magnetics Letters*, vol. 3, pp. 3000304-3000304, May 2012.

[29] J. Z. Sun, “Spin angular momentum transfer in current-perpendicular nanomagnetic junctions,” *IBM Journal of Research and Development*, vol. 50, no. 1, pp. 81-100, Jan. 2006.

[30] W. Kang, Y. Ran, Y. Zhang *et al.*, “Modeling and exploration of the voltage-controlled magnetic anisotropy effect for the next-generation low-power and high-speed MRAM applications,” *IEEE Transactions on Nanotechnology,* vol. 16, no. 3, pp. 387-395, May 2017.

[31] Y. Wang, H. Cai, L. Naviner *et al.*, “Compact thermal modeling of spin transfer torque magnetic tunnel junction,” *Microelectronics Reliability,* vol. 55, no. 9, pp. 1649-1653, Aug. 2015.

[32] W. Zhao, C. Chappert, V. Javerliac *et al.*, “High speed, high stability and low power sensing amplifier for MTJ/CMOS hybrid logic circuits,” *IEEE Transactions on Magnetics*, vol. 45, no. 10, pp. 3784-3787, Oct. 2009.

[33] W. Kang, W. Zhao, Z. Wang *et al.*, “A low-cost built-in error correction circuit design for STT-MRAM reliability improvement,” *Microelectronics Reliability,* vol. 53, no. 9–11, pp. 1224-1229, Sep. 2013.