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Progress on Carbon Nanotube BEOL Interconnects

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***Abstract*—This article is a review of the current progress and results obtained in the European H2020 CONNECT project. Amongst all the research on carbon nanotube interconnects, those discussed here cover 1) process & growth of carbon nanotube interconnects compatible with back-end-of-line integration, 2) modeling and simulation from atomistic to circuit-level benchmarking and performance prediction, and 3) characterization and electrical measurements. We provide an overview of the current advancements on carbon nanotube interconnects and also regarding the prospects for designing energy efficient integrated circuits. Each selected category is presented in an accessible manner aiming to serve as a review and informative cornerstone on carbon nanotube interconnects.**

***Index Terms*—carbon nanotubes, interconnects**

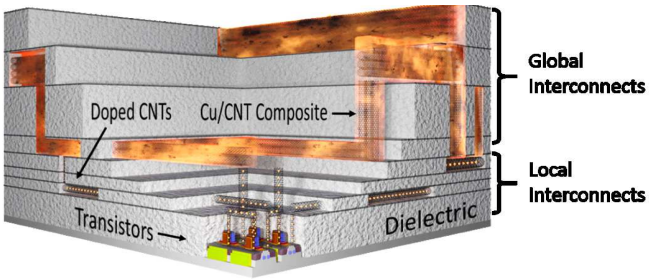

Fig. 1. Schematic of using doped CNTs for local interconnects and CNT-Cu-composite material for global interconnects.

I. Introduction

Carbon nanotubes (CNTs) have sparked a lot of interest in their applicability as future VLSI interconnects because of their extremely desirable properties of high mechanical and thermal stability, high thermal conductivity and large current carrying capacity [1]–[4]. Due to strong sp^2 bonding between carbon atoms, CNTs are much less susceptible to electromigration (EM) problems than copper interconnects and can carry high current densities [1]. Ballistic electronic transport can go over long nanotube lengths, 1 μm, enabling CNTs to carry very high currents with virtually no heating due to nearly 1D electronic structure. Metallic single-walled CNT bundles have been shown to be able to carry extremely high current densities of the order of 10^9 A/cm^2 [5]. In contrast, EM limits the current carrying capacity of Cu interconnects to 10^6 A/cm^2 [6]. Copper interconnect with cross-section 100 nm x 50 nm can carry currents up to 50 μA, whereas a 1 nm diameter CNT can carry up to 20-25 μA current [7]. Hence, from a reliability perspective, a few CNTs are enough to match the current carrying capacity of a typical Cu interconnect. Although it should be noted, that the need to reduce interconnect resistance (and hence delay) makes it necessary to have CNTs with a minimum density of 0.096 per nm^2 [8], if pure CNT interconnects are used. Additionally, estimations based on measured thermal conductivity (K_{th}) on films of single-wall CNTs (SWCNT) bundles, combined with observations from electrical conductivity experiments, predict K_{th} in the range 3000-10000 W/mK [9] at room temperature, while K_{th}, Cu = 385 W/mK. Hence, heat diffuses more efficiently through CNT vias than Cu vias and can reduce the on-chip temperature. Such properties also make CNTs desirable as vertical through-silicon via for three-dimensional (3D) integration.

In this paper, we highlight the recent advancements of carbon nanotubes as interconnect material based on the current progress and results achieved on H2020 CONNECT project. The rest of the paper is organized as follows. Section II presents carbon nanotube growth process and integration approaches. CNT transport properties and circuit-level modeling are described in Section III. Section IV provides an overview of the CNT characterization and electrical measurements. Section V concludes the paper.

II. CNT Process & Growth

Using CNTs as interconnect material in semiconductor manufacturing is a huge paradigm shift, even higher than the change from aluminum (Al) to copper (Cu) in Back-End-of-Line metallization. For this to be a realistic alternative for high volume manufacturing a lot of challenges, have to be addressed. We need reliable and reproducible integration approaches for manufacturing, more importantly, CMOS compatibility has to be targeted, both in terms of materials and process temperature. Additionally, defectivity of CNTs has to be under control for performance and variability reasons and contacting the CNTs reliably is an issue as well.

To target different requirements two approaches have been subject of research and are presented in this paper. First, local interconnects are to be replaced by single CNTs modified by doping to tackle variability and increase conductivity.

Second, global interconnects of composite Cu-CNT material is studied to improve ampacity and help with integration. Fig. 1 illustrates the vision of H2020 CONNECT project.

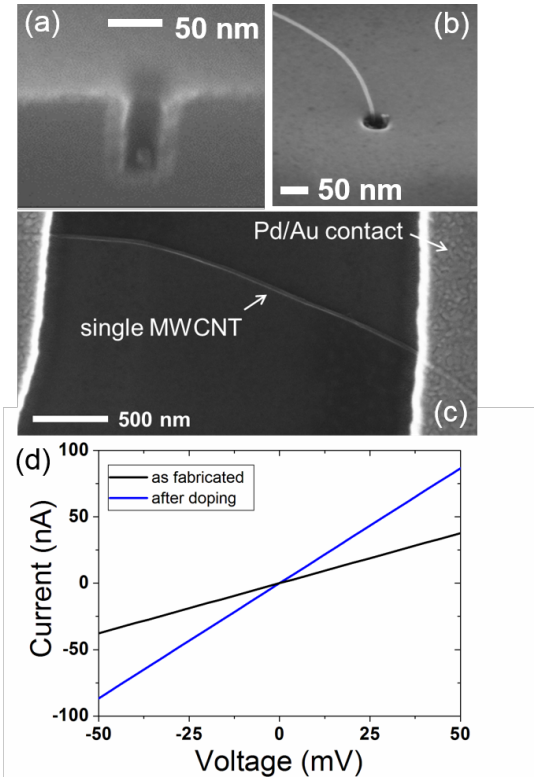

Fig. 2. 30 nm via hole with catalyst at the bottom before (a) and after (b) CVD growth of single CNT. (c) Side-contacted single MWCNT horizontal interconnect and (d) its electrical characterization before and after doping by $PtCl_4$.

A. Doped CNTs as local interconnects

The parallel fabrication of single CNT horizontal interconnects with controlled placement is achieved by catalytic chemical vapor deposition (CVD) of CNT on catalyst nanoparticle localized in pre-patterned nanometric via holes. Single MWCNTs with 4 or 5 walls and diameter around 7.5 nm are typically synthesized from a 1 nm thick catalyst film deposited at the bottom of a 30 nm via hole (Fe catalyst on aluminosilicate support). CNTs are then aligned on the sample surface before patterning of Pd/Au electrodes to electrically contact the CNTs. This unique technological platform is used to address the most critical points related to the integration of CNTs as local interconnects, namely the variability in electrical performances, the electrical contacting and transport mechanism in MWCNT, and the charge transfer doping of CNTs and its stability. As an illustration, Fig. 2 showcases a side-contacted MWCNT and the impact of (external) doping by $PtCl_4$ solution on its electrical resistance. Alternate processes for the internal doping of end-contacted CNTs are also being developed.

CNTs grown by CVD method have inherent challenges mainly 2/3rd of CNTs are semi-conducting. Secondly, the presence of defects due to low-temperature growth compared to the Arc-discharged method. These problems lead to the variation of resistance in the CNT interconnect device. One way to overcome the variability of resistance is by doping. As shown from the simulations, internal doping of CNT is more stable than external doping. Therefore we have developed a protocol to insert dopants in the CNTs. The ends of the CNTs are opened using optimized plasma process. This allows the dopants to move into the CNTs in a liquid medium. The result of doping process can be seen in the STEM image in Fig. 3. In this High Angle Annular Dark Field (HAADF) image, the bright dots are individual Pt atoms. The wall of the CNTs are less bright but are visible. EDX analysis proved the dopants are composed of an amorphous network of Pt and Cl atoms.

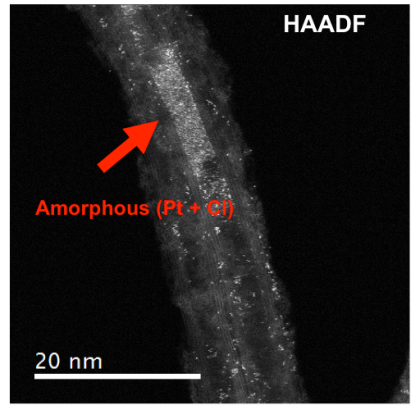

Fig. 3. STEM image of PtCl doping inside of CNT.

B. CMOS compatible CNT growth

To ensure compatibility with state of the art semiconductor manufacturing process flows the growth of CNTs has to be adapted in terms of catalyst material and process temperature. For this, we developed a catalyst based on cobalt (Co), which is a material commonly used in CMOS BEOL flows. Additionally, the CNT growth temperature has to be lowered to $< 400^oC$. Several experiments have been done at Aixtron, and the resulting CNT layers were characterized by SEM and Raman spectroscopy. First results indicate that good CNT growth on Co catalyst at lower temperatures is possible, enabling future integration paths (see Fig. 4).

To be a real alternative for leading-edge semiconductor manufacturing, CNT integration has to be scaled up from a lab to a fab scale. This means reliable processes on 300 mm wafer size have to be demonstrated. This could be shown together with Aixtron with a good starting uniformity and full 300 mm wafer CNT-growth (see Fig. 5).

C. Cu-CNT composite formation

Embedding CNTs in a copper matrix presents several advantages. Integration such as void-free filling, CMP or patterning becomes possible, variability can be decreased, and an efficient trade-off between resistivity and ampacity can be realized. Using galvanic electrodeposition, several

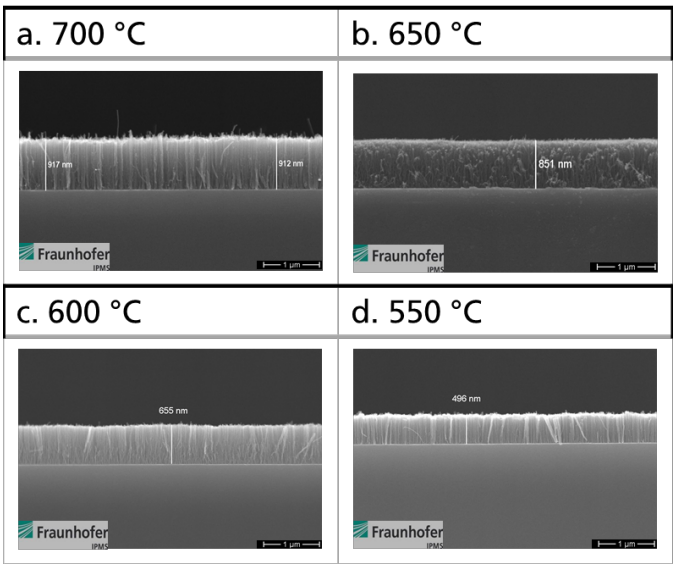

Fig. 4. SEM Results of CNTs grown with Co catalyst at different temperatures so that the growth process can be shifted into the CMOS compatible temperature range.

approaches of impregnating bundles of CNTs with copper have been investigated. In principle there are two ways, electroless deposition (ELD) [10] [11] [12] [13] and electrochemical deposition (ECD) [14]. The former needs lower technical effort, but often involves a multitude of different chemicals, which again raises the question of CMOS compatibility. While the latter, ECD, is more common, has a lot of control knobs but needs a conductive substrate. Both methods were extensively investigated for both, vertically (VA) and horizontally aligned (HA) MWCNTs. While the VA-CNTs could be used directly after growth, the HA-CNTs needed to be prepared using a specially developed technique from CEA. With this, properly aligned HA-CNT carpets could be realized.

Fig. 6 shows a cross-section and a top-view SEM of a sample of VA-CNT after Cu impregnation via an ELD step. After filling of the CNTs, an additional Cu overburden can be seen which results in additional Cu crystal growth on top. The small inset photo confirms copper plating on a silicon coupon. For the HA-CNTs a successful ECD process was developed. Fig. 7 shows the void-free filling of HA-CNT bundles.

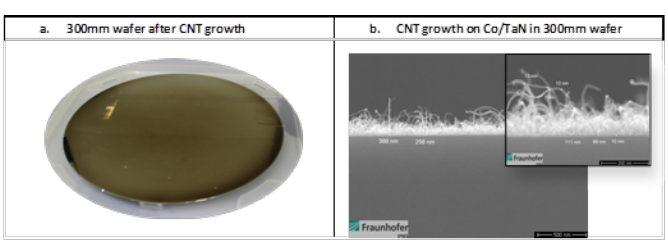

Fig. 5. CNT growth with Co catalyst on a 300 mm wafer.

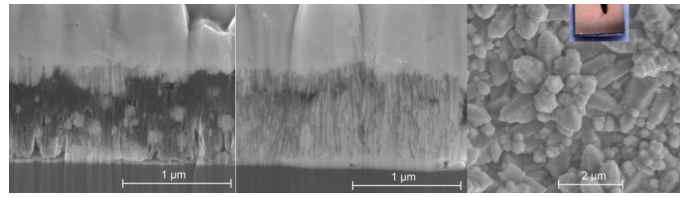

Fig. 6. SEM cross-section and top-view of Cu-impregnated VA-CNTs. Inset shows the Cu layer.

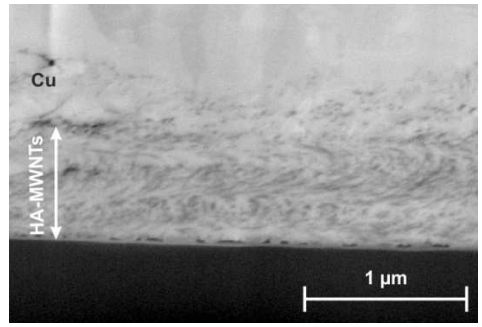

Fig. 7. SEM cross-section and Cu-impregnated HA-CNTs.

III. Atomistic to Circuit-level Modeling

A. First principle calculations

To understand the physical properties of CNTs, we have performed Density Functional Theory (DFT)-based simulations, implemented in Atomistix ToolKit [15] [16] [17]. All atoms are fully relaxed until the forces of any atom become less than 0.01 eV/$\AA$. The generalized gradient approximation (GGA) was applied as the exchange-correlation functional. For the transport simulation, we have used the Non-Equilibrium Greens Function (NEGF) framework with the ballistic approximation. Fig. 8a shows the dependence of the ballistic conductance G_{bal} on the diameter of SWCNTs. From G_{bal}, we can extract the number of conducting channel (N_c) as follow:

$$N_c = G_{bal}/G_0 \tag{1}$$

where G_0 is the quantum conductance (0.077 mS). It is important to note that although there is a variation due to the quantum confinement effects with a small diameter of SWCNTs, the value of N_c is close to 2 regardless of the diameter and chirality. In other words, the conductance of CNTs per unit area decreases as the diameter increases.

We also investigate the impact of doping CNTs on conductance. Fig. 8b shows the optimized atomic structures of armchair SWCNT(7,7) with and without iodine dopant, respectively. The diameter of SWCNT(7,7) is about 1 nm. Fig. 8c describes their band structure and transmission coefficient obtained from DFT calculations. We found that iodine atom acts as a p-type dopant well in CNTs because the Fermi-level shifted down by about 0.6 eV. Simultaneously, the ballistic conductance increases from 0.155 mS to 0.387 mS after doping process.

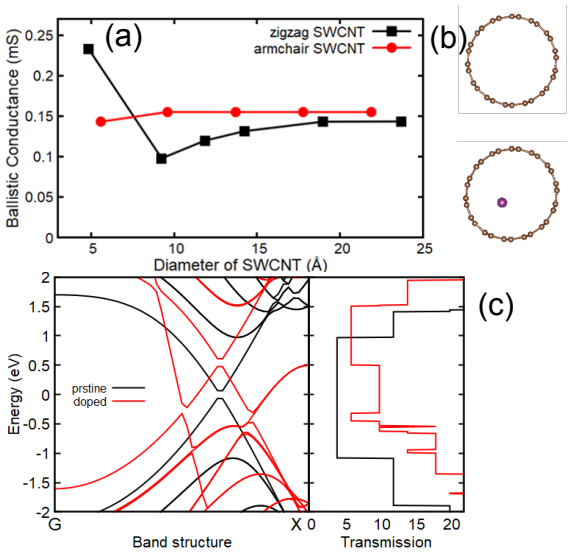

Fig. 8. (a) Ballistic conductance vs. diameter of zigzag and armchair SWCNTs at 300K, and (b) atomic structures of CNT(7,7) with and without iodine dopant. Brown and purple spheres indicate the carbon and iodine atoms, respectively. (c) Band structure and transmission coefficient of pristine and doped SWCNT(7,7) are shown, respectively. The Fermi-level is set to 0.0 eV.

B. TCAD simulations

We compute the material parasitics based on the results obtained by first principle calculations. For example, Fig. 9 shows the electrical conductivity of SWCNT and MWCNT lines with different lengths and diameters, as compared to Cu lines. The conductivities are calculated using analytical models [18] [19], where the fitting parameters are calibrated against the ab-initio simulations described in Section III.A. A finite-difference approach is adopted to solve the Laplace equations for macroscopic resistance and capacitance (RC) extraction in complex interconnect structures:

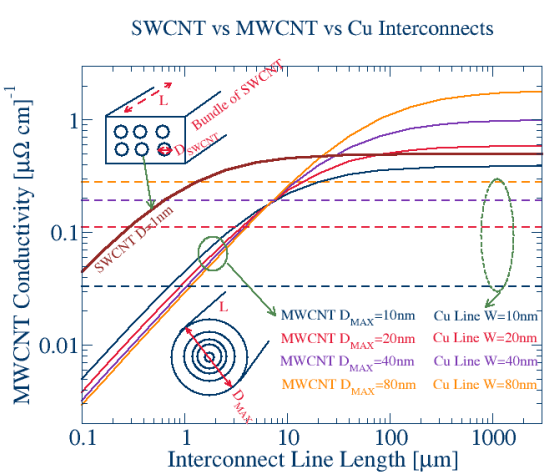

Fig. 9. Conductivity of SWCNT and MWCNT lines with different lengths and diameters, as compared Cu lines.

$$\nabla \varepsilon \nabla \psi = 0 \quad for\ an\ insulator \tag{2}$$

$$\nabla \kappa \nabla \psi = 0 \quad for\ an\ metal \tag{3}$$

where ε, κ, and ψ are permittivity, conductivity, and potential, respectively. Fig. 10 shows the 3D TCAD simulation output for a 14nm CMOS inverter highlighting the cross-talk between lines up to the M2 interconnect level. Advanced models for conductivity and capacitance of both Cu and CNT are implemented using ab-initio results. Extracted RC netlists are provided in a SPICE-like format for circuit-level simulation.

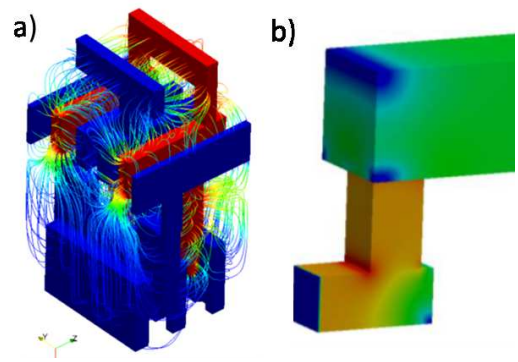

Fig. 10. (a) 3D TCAD capacitance, where the electric field streamlines highlight the cross-talk between interconnects. (b) Resistance simulation detail, where the current density flow highlights the interconnects hot-spots.

C. Electrical compact models and simulation

CNT electrical compact models have been established several years ago by [20] [21]. We developed RC compact models for doped CNTs. Doping is considered as an effective way to counteract to the challenges associated with CNT chirality control, defective growth, and resistive metal-CNT contacts. Inner and outer Iodine charge transfer doping has been investigated and compact models are developed for circuit-level simulation. Based on the understandings from atomistic simulations, we introduce the doping enhancement factor N_c (i.e. conducting channels per shell), as doping can shift the Fermi-level and increase the DOS for pristine CNTs, hence, we generate more conducting channels and ultimately reduce resistance [22]. Doped MWCNT resistance and capacitance are derived as:

$$R_{MW} = 1/(N_C N_S G_{1-channel}) \tag{4}$$

$$C_{MW} = \frac{N_C N_S C_{Q,1-channel} \cdot C_E}{N_C N_S C_{Q,1-channel} + C_E} \approx C_E \tag{5}$$

One-channel conductivity is given by $G_{1-channel}$ = G_0 / (1 + L/L_{MFP}). G_0 is quantum conductance ($\sim$1/12.9 k$Omega$)). L_{MFP} is used for metallic CNT [19]. Quantum capacitance per channel $C_{Q-1channel}$ is given as 96.5aF/μm [20], C_E is electrostatic capacitance and is geometry dependent, C_E does not depend on doping. Number of shells (N_s) is derived as $diameter - 1$.

Fig. 11 shows the circuit benchmark with CMOS 45nm technology node inverters connected with doped MWCNT interconnects. We perform simulations with pristine and doped MWCNTs with the outermost shell diameter of 10, 14, and

$22nm$, respectively. We derive the delay ratio between doped and pristine MWCNT over different interconnect lengths and number of conducting channels (N_c) as shown in Fig. 12. We select N_c per shell to vary from 2 to 10 for different doping concentrations.

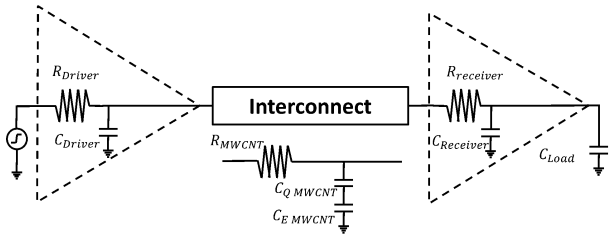

Fig. 11. Circuit benchmark with 45nm technology node inverters connected with MWCNT interconnects.

Delay ratio is calculated by the ratio of propagation delay with respect to pristine MWCNT ($N_c = 2$). In this study, we assumed that MWCNT is filled with shells until its diameter is smaller than D_{CNT}^{max} / 2 and each shell has the same N_c. We also have investigated the doping effects by changing N_c. As shown in these figures, dopants in MWCNT interconnects with D_{CNT}^{max} of 10, 14, and $22nm$ reduce the propagation delay by 10, 5 and 2 %, respectively, when $L = 500\mu m$. By increasing D_{CNT}^{max} also increases the number of shells (N_{sh}) and number of the conducting channels ($N_C^{tot} = N_{sh} \times N_c$), doping effects diminishes. Additionally, we observe that as L increases, doping becomes more effective in reducing delay.

IV. Characterization & Electrical Measurements

A. Test layout for EM studies

For a detailed electrical characterization, a special test layout was designed as shown in Fig. 13a. Apart from single line structures varying width, length and angle also multi-line structures, comb structures, extrusion monitors and via test patterns are included. To emulate advanced nodes, part of the layout is designed for E-beam lithography to generate lines with 50 nm widths.

The aim is to do a full wafer electrical characterization to enable the transfer from lab to manufacturing. Fig. 13b shows the first 300 mm wafer patterned with the Cu reference test structure. In the end, the new Cu-CNT composite material has to be benchmarked against state-of-the-art Cu BEOL metallization with the focus on reliability improvement for small dimensions regarding ampacity and electromigration resistance.

B. Thermal studies

The resistance of a CNT line always consists of two parts, the contact resistance and the resistance of the CNT itself. For obtaining the contact resistance and CNT resistance per unit length, the transmission line measurement technique can be used [23]. MWCNTs of different lengths are contacted, and the resistance of the resulting structure is measured. By correlating line length with total resistance, contact resistance and CNT resistance per unit length can be extracted.

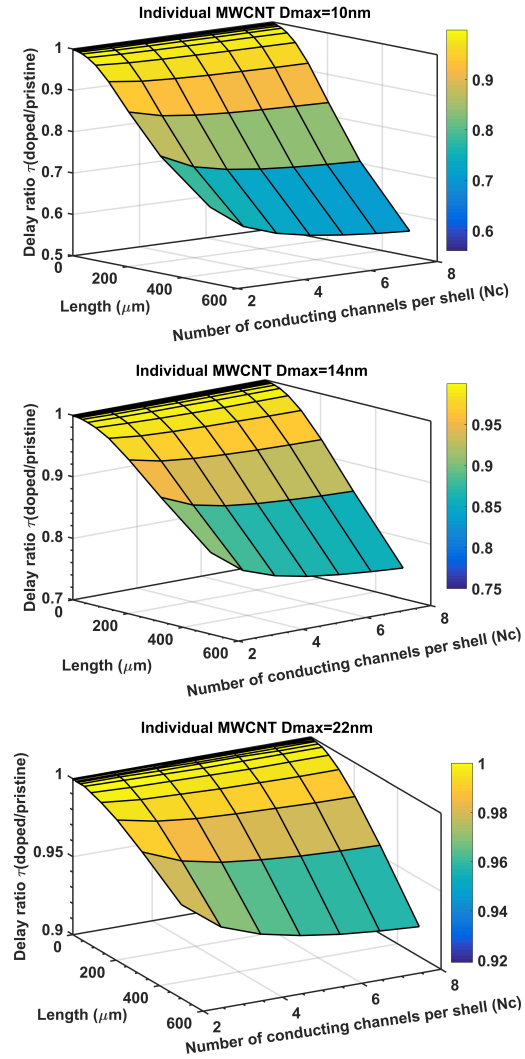

Fig. 12. The dependence of the delay ratio of MWCNT interconnects with D_{CNT}^{max} = 10 nm, 14 nm, and 22 nm on the interconnect length and the number of conducting channel per shell.

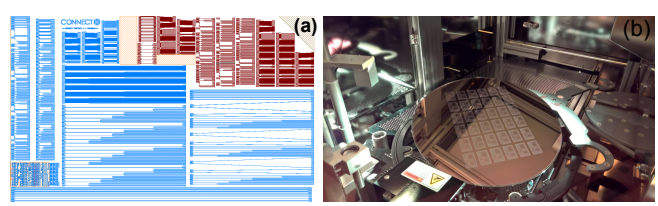

Fig. 13. (a) Test layout for electrical data and electromigration characterization, and (b) full 300 mm wafer patterned with Cu reference test layout.

A significant advantage of CNT interconnects is their high thermal conductivity, which holds the potential to alleviate thermal design constraints in advanced integrated circuits. To fully benefit from this advantage, a good understanding of their thermal properties is needed. Because MWCNTs have diameters on the order of 10nm, only a few techniques for thermal conductivity and self-heating studies can be consid-

ered [24]. Scanning thermal microscopy with resistively heated probes holds the potential to perform temperature mapping of MWCNT interconnects under operation. Hence we can study their self-heating and extract thermal conductivity data [25].

Knowledge of the positioning of dopant particles is crucial for improving doping recipes. In the extreme case, the dopants are individual atoms. Therefore, they need to be studied with atomic resolution. For this purpose, TEM can be used. It is planned for the project to perform TEM measurements of operating CNT interconnects *in situ*, to study dopant migration and CNT degradation at high current densities.

V. Conclusion

Carbon nanotubes present viable solutions to overcome the current challenges with copper interconnect technology. Nevertheless many challenges remain. On the processing side, continued efforts are needed on the CVD growth of CNTs both to produce high-quality CNTs at a reasonable temperature, but also to reduce the CNT tortuosity and increase their packing density in interconnects. For back-end-of-line fabrication process, issues arise from high planarity CMP processes, temperature budget (i.e., 400^oC) and contamination management. Stable doping of CNTs at the operating temperature of circuits still needs to be developed and integrated into BEOL processing. The fabrication of aligned CNT-Cu composite material requires specific developments, and the corresponding electrical conduction mechanism needs to be carefully studied. On characterization, there is a need for structural and morphological CNT-level electrical and thermal characterization. Research efforts related to physical modeling, physical design, design space exploration, CNT processing and characterization are gaining momentum and will provide a clearer picture of the costs and benefits of integrating CNTs as on-chip interconnects. Concerning modeling, electro-thermal modeling and simulation tools are needed to evaluate the performance, reliability, and variability of CNTs, and composite Cu-CNT interconnects. It can also help to assess the impact of CNT-metal contacts. In this context, a multi-scale physics-based simulation platform (from ab-initio material simulation to circuit-level) that considers all aspects of VLSI interconnects (i.e., performance, power, and reliability) is desirable to explore and evaluate the potential of CNT technology. In summary, there are a lot of research efforts ongoing on CONNECT project and also required from the community into enabling CNTs for BEOL interconnects.

Acknowledgment

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