

Atomistic to circuit level modeling of defective doped SWCNTs with contacts for on-chip interconnect application

Jie Liang, Lee Jaehyun, Salim Berrada, Vihar P. Georgiev, Asenov Asen,
Nadine Azemard, Aida Todri-Sanial

► To cite this version:

Jie Liang, Lee Jaehyun, Salim Berrada, Vihar P. Georgiev, Asenov Asen, et al.. Atomistic to circuit level modeling of defective doped SWCNTs with contacts for on-chip interconnect application. NMDC: Nanotechnology Materials and Devices Conference, Oct 2017, Singapore, Singapore. pp.66-67, 10.1109/NMDC.2017.8350506 . lirmm-01880220

HAL Id: lirmm-01880220

<https://hal-lirmm.ccsd.cnrs.fr/lirmm-01880220>

Submitted on 16 Jul 2019

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



University
of Glasgow

Liang, J., Lee, J., Berrada, S., Georgiev, V., Asenov, A., Azemard-Crestani, A. and Todri-Sanial, A. (2018) Atomistic to Circuit Level Modeling of Defective Doped SWCNTs with Contacts for On-Chip Interconnect Application. In: 12th IEEE Nanotechnology Materials and Devices Conference (NMDC 2017), Singapore, 2-4 Oct 2017, pp. 66-67. ISBN 9781538627723.

There may be differences between this version and the published version. You are advised to consult the publisher's version if you wish to cite from it.

<http://eprints.gla.ac.uk/151261/>

Deposited on: 30 November 2018

Enlighten – Research publications by members of the University of Glasgow
<http://eprints.gla.ac.uk>

Atomistic to Circuit Level Modeling of Defective Doped SWCNTs with Contacts for On-Chip Interconnect Application

J. Liang¹, J. Lee², S. Berrada², V. Georgiev², A. Asenov², N. Azemard-Crestani¹, A. Todri-Saniai¹

CNRS-LIRMM/University of Montpellier, France¹
School of Engineering, University of Glasgow, UK²

I. INTRODUCTION

Carbon nanotubes (CNTs) due to their high electrical/thermal conductivity, high ampacity, high tolerance to electromigration [1] and small dimensions make them an ideal candidate for future on-chip interconnects [2]. Fabricating the CNTs, random chirality and some defects are introduced which can degrade the CNT electrical properties [3]. Additionally, the contact resistance between metal and CNT presents additional parasitics that impose restraints on the electron transport. Electrical models of CNT for interconnect application were developed several years ago [4-5]. In this paper, we explored on doped and defective single-wall CNTs (SWCNT (24,0)) including contact resistance as important physical parameters to assess the performance of fabricated SWCNTs realistically for back-end-of-line (BEOL) on-chip interconnects on VLSI circuit application.

II. HIERARCHICAL MODEL

Fig. 1 shows the atomistic structure of SWCNT (24,0). In order to extract the defective resistance with this structure, we have performed tight-binding (TB) - Non-Equilibrium Green's Function (NEGF) simulations implemented in the Atomistic ToolKit (ATK) [6-7]. The length of central region is set to about 42.6nm having 9600 carbon atoms. We distributed vacancy defects in central region randomly from 1 to 6, and have calculated the defective resistance by $R_{defect} = R - R_{perfect}$. The dependence of R_{defect} on the number of defects is shown in **Fig. 2**. For statistical analysis, 80 samples were used. We have found that the median value of R_{defect} varies from 4 to 40 k Ω with 1 to 6 defects, respectively.

We have calculated the number of conducting channels N_C of doped SWCNT (24,0) using Density Functional theory (DFT) with generalized gradient approximation (GGA). It was assumed that the dopant only changed the Fermi level of the CNT without affecting its band structure. The number of conducting channel is derived by G/G_0 , where G_0 is the quantum conductance $2e^2/h$ ($G_0 = 7.748 \cdot 10^{-5}$ S). Thanks to the DFT-GGA calculation, we have found that N_C can vary from 2 to 8 when the Fermi level is changed from -1.0 to 1.0 eV (0.0 eV is set to the Fermi level of pristine CNT.).

Based on previous works, SWCNT interconnect can be represented by an RC-model. By taking into the account the impact of doping, defects and contact resistance, we compute the SWCNT resistance as follows:

$$R_{SWCNT} = \frac{h}{2e^2 N_C} \left(1 + \frac{L}{L_{mfp}} \right) + R_{defect} + R_{contact}, \quad \text{where}$$

L_{mfp} and L are the electron mean free path and the interconnect length, respectively [8]. Moreover, the parasitic capacitance can be written by $C_{SWCNT} = \frac{C_Q C_E}{C_Q + C_E}$, where C_Q and C_E are quantum and electrostatic capacitances, respectively [4]. We use a circuit benchmark as shown in **Fig. 3** to investigate SWCNT's performance. R_{driver} , C_{driver} and C_{load} are assumed to be 24 k Ω , 450aF and 10fF, respectively, which are values extracted from the logic gates implemented in CMOS 45nm technology node using Cadence environment with Verilog-A models.

III. SIMULATION RESULTS

Fig. 4 shows the delay ratio of the doped and defective SWCNT(24,0) to the perfect SWCNT. SWCNT interconnect length sets to be 1 μ m. As shown in the figure, the propagation delay (t_d) decreases as N_C increases by dopants. This is because the interconnect resistance decreases due to larger N_C . In this analysis, the change of C_Q due to the Fermi level shift had no significant effect. However, additional defective resistance increases the propagation delay. We observed that t_d increases by about 6% due to 6 defects, and increasing N_C to 8 reduces it to 5%. Moreover, the delay ratio of doped SWCNT ($N_C = 3$) with 1 defect decreases to 1, which means that it has the same t_d as the perfect SWCNT. Such results indicate that doped CNTs can mitigate the increase in t_d caused by defects. However, if there are two or more defects, it is not possible to return the delay ratio to 1.0 even with high doping concentration. Thus, it is more important to not create too much defects during the fabrication process.

Fig. 5 (a) describes the dependence of the delay ratio of the doped SWCNT on the contact resistance when $L = 1 \mu$ m. In order to keep the delay ratio less than 1, the contact resistance should be less than 4 k Ω (8 k Ω), and N_C should be greater than 3 (8). However, if $L = 10 \mu$ m, the delay ratio is less than 1 even though the contact resistance and N_C are 10 k Ω and 3, respectively as shown in **Fig. 5** (b). Given the time delay dependence on L , we found that doping process has a greater impact to enhance the conductance when the interconnect length is longer. Therefore, for the efficient circuit, one should focus on reducing the contact resistance as the interconnect length is shorter.

IV. CONCLUSION

A hierarchical model, from atomistic to electrical compact model is presented and investigated. We calculate the defective resistance and number of conducting channels of doped SWCNT using TB and DFT-GGA approaches. Through the circuit-level electrical compact modeling and simulations, we investigate the impact of defects and doping on the SWCNT interconnect in terms of the propagation delay. We believe that our study provides the guidelines for the optimal design of CNT interconnects.

ACKNOWLEDGMENT

Authors would like to thank H2020 CONNECT European project. This project has received funding from the European Union's Horizon 2020 research and innovation program under grant agreement No 688612. (<http://www.connect-h2020.eu/>)

REFERENCES

- [1] C. Subramaniam et al. Nat. Commun. 4, 2202 (2013).
- [2] A. Todri-Sanial et al., Carbon Nanotube Interconnects: Process, Design and Applications, Springer 2016, ISBN#: 978-3-319-29744-6.
- [3] M. Bockrath et al. Science, 291, 283-285 (2001).
- [4] Srivastava et al. ICCAD-2005. IEEE/ACM (2005).
- [5] L. Hong et al. IEEE Transactions on electron devices 55.6 (2008) : 1328-1337.
- [6] Atomistix Tool Kit (2016.3), QuantumWise A/S.
- [7] Y. Hancock et al. J Low Temp Phys, 153, 393-398 (2008).
- [8] J. Jiang et al. Physical Review Letter, vol. 64, no. 4, 2 July 2001.

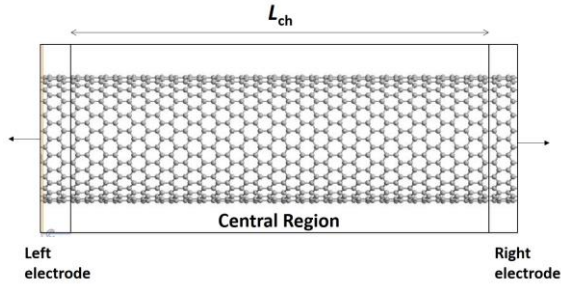


Figure 1. Atomistic structure of SWCNT (24,0) interconnect.

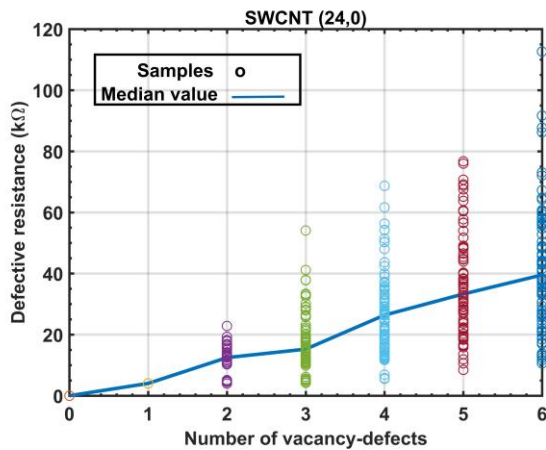


Figure 2. Dependence of defective resistance on number of vacancy defects for SWCNTs (24,0). We used 80 samples for the statistical analysis.

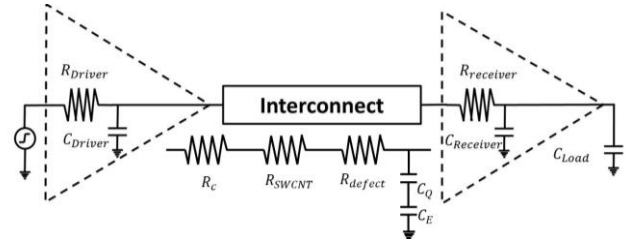


Figure 3. Schematic diagram for the circuit-level simulation.

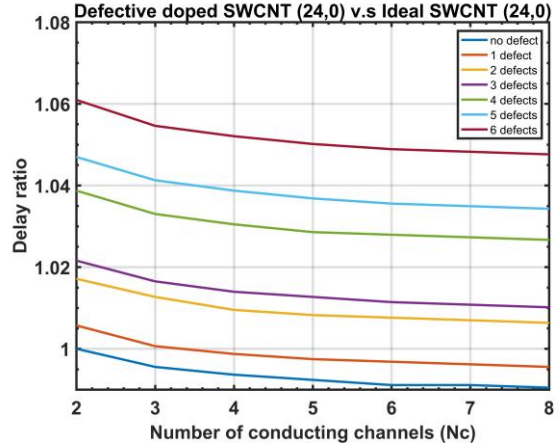


Figure 4. Dependence of the delay ratio of defective SWCNT(24,0) to perfect SWCNT(24,0) on the number of conducting channels.

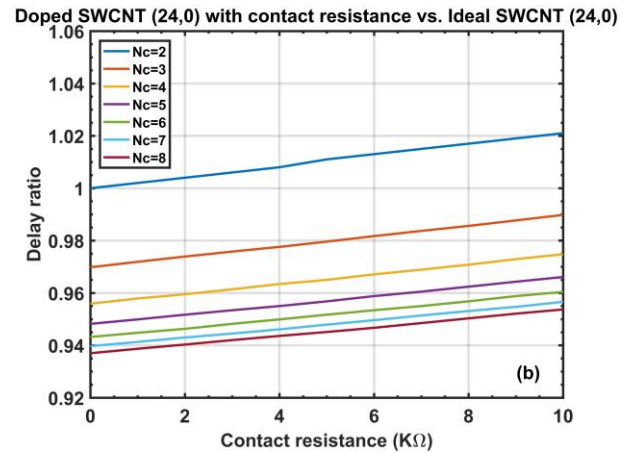
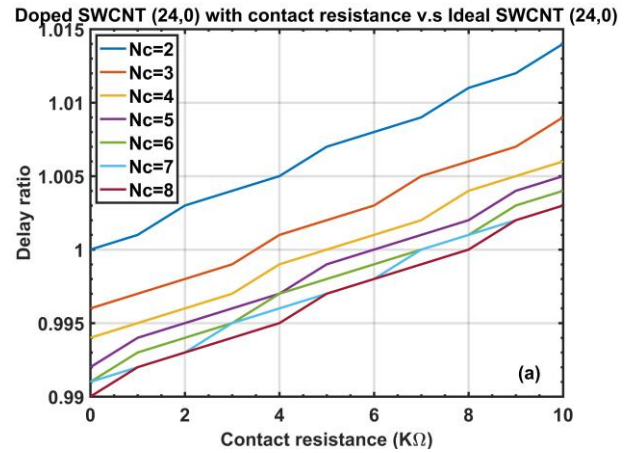


Figure 5. Dependence of the delay ratio of doped SWCNT to perfect SWCNT on the contact resistance. Interconnect lengths are (a) 1 μm and (b) 10 μm , respectively.