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Power Distribution Studies for CMS Forward Tracker

A.Todri, M.Turqueti, R.Rivera and S.Kwan

***Abstract* — The Electronic Systems Engineering Department of the Computing Division at the Fermi National Accelerator Laboratory is carrying out R&D investigations for the upgrade of the power distribution system of the Compact Muon Solenoid (CMS) Pixel Tracker at the Large Hadron Collider (LHC). Among the goals of this effort is that of analyzing the feasibility of alternative powering schemes for the forward tracker, including DC to DC voltage conversion techniques using commercially available and custom switching regulator circuits. Tests of these approaches are performed using the PSI46 pixel readout chip currently in use at the CMS Tracker. Performance measures of the detector electronics will include pixel noise and threshold dispersion results. Issues related to susceptibility to switching noise will be studied and presented.**

In this paper, we describe the current power distribution network of the CMS Tracker, study the implications of the proposed upgrade with DC-DC converters powering scheme and perform noise susceptibility analysis.

***Index Terms* — Power distribution network, power supply noise.**

I. Introduction

The inner detectors of the Large Hadron Collider (LHC) are pixel and strip silicon detectors. Compact Muon Solenoid (CMS) is one of the detectors capable of studying various aspects of proton collisions at 14 TeV. CMS contains thousands of pixel and silicon strip modules with millions of channels in a small space volume. Delivering power reliably to all modules in a high radiation environment is a challenging task.

The Large Hadron Collider (LHC) is expected to be upgraded to the Super-LHC in order to deliver 10-fold increased luminosity [1]. Such upgrade brings additional challenges to the power delivery network. The detectors will face high particle densities and radiation levels. Detector granularity and electronics channels will increase 2-10 times depending on radius angular region and sensor technology [1]. Thus, distribution of power in an efficient and reliable fashion with minimum volume of cables is a key challenge for the CMS upgrades.

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In this work, we perform a detailed power network analysis for the CMS upgrade and investigate its implications on the system. This paper focuses on the powering scheme with DC-DC converters which utilizes the existing power distributions and cables with minor modifications. We further study the impact of power supply noise to pixel performance.

The remainder of this paper is organized as follows. In Section II, we introduce the design and architecture of the power network for CMS Forward Tracker. In Section III, we analyze the noise sensitivity and threshold of the pixel modules. In Section IV, we analyze the power network for FPIX with DC-DC converter insertion. Section V brings the conclusions and future work.

II. CMS Tracker Power Distribution

The current CMS Forward Tracker [2] has 4320 hybrid modules consisting of pixel sensors with readout chips or ROCs. A plaquette is a cluster of several ROCs. Several plaquettes constitute a panel, and two panels assembled together make a blade. Forward tracker disks are populated with blades. Each detector module has three blades (or 6 panels that equals 135 ROCs) which are powered in parallel through several cables from the main power supply unit. The power lines pass through several boards and 45 meters of cable till reach the pixel modules. Figure 1, illustrates the global power distribution from the power supply to the blades.

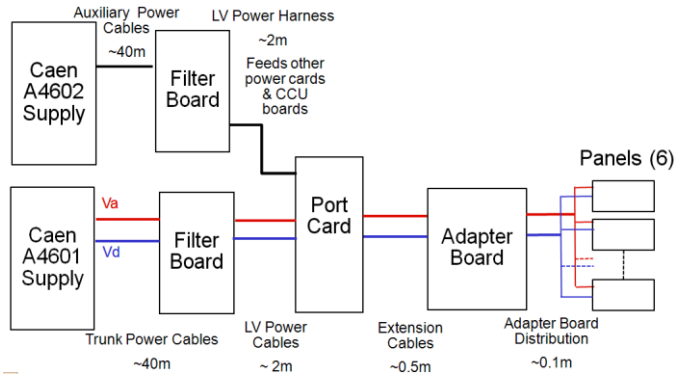

Figure 1. Current power distribution network for the Forward Tracker. Power is distributed from CAEN power supply to filter board, port card, and adapter board to power the blade modules.

The current consumptions for the detector module are as follows: analog current consumption is 3.4A at 1.6V and digital current consumption is 3.8A at 2.6V. The power loss on the cables constitutes the largest power loss on the system which is measured to be up to 66% from the total power delivered from the power supply. Power loss is derived as:

$$P_{loss\_dc} = \sum_i P_{cables_i} \quad (1)$$

Table 1 shows the power loss on the cables for both digital and analog line, respectively.

TABLE 1. Power loss on cables for digital and analog line.

Power	CAEN	Cables	Detector
Analog	26.54W	17.55W	8.96W
Digital	48.6W	26.2W	22.36W

Plans for upgrading the CMS Forward Tracker are being discussed and developed to in order to accommodate higher fluency rates up to 10^9n/cm2 [1]. These upgrades entail an increase in number of ROCs and readout channels which brings additional challenges to the tracker power distribution. The number of ROCs is increasing from 135 to 224, which consequently increases the amount of current flowing on the cables and traces.

To facilitate the power distribution for the FPIX upgraded, two power schemes have been proposed by the research community, serial powering (SP) [3] and DC-DC converters [4]. In SP scheme, sensor modules are powered in series through a current source [5], while in DC-DC powering scheme, modules are powered in parallel where higher voltages at low currents are transmitted through the cables to reduce their voltage drop. In this work, we have investigated the DC-DC powering scheme.

III. Noise Analysis

The noise analysis carried out on this work has as objective to allow realistic planning for the power system upgrade of the CMS Pixel Forward Tracker.

Performance of the pixel readout system is affect by noise present on its power lines. Therefore, an investigation on the performance degradation of the pixel readout chip system is important for any plans that would cause increase of noise on the power lines. The chip used for these studies was the current CMS pixel tracker chip, the PSI46. The studies were performed with single chips and eight ROCs clusters called plaquettes.

Noise on the power lines can be caused by the power supply, by operations of the system itself such as register programming and data readout or by external sources such as EMI coming from other systems of the CMS detector. This work focuses its analyses on noise generated from the power supplies and how this affects the performance of the readout system.

The parameters chosen for judging the degree on which the system is being affected are measurements of noise at the pixel and readout chip levels. Changes of the threshold dispersion of the readout chip are also evaluated.

Initial tests had the objective of finding the limits of the readout chip noise tolerance by injecting noise on the analog and digital power lines. The digital part of the ROC proved to be remarkably immune to noise influence on its power line, being able to support the injection of single tone noise frequencies accounting up to 20% of the power provided to the pixel chip before problems were detected. At these noise levels the test was carried out in the range of 1 kHz to 20 MHz and the effects were basically the same, failure to program the registers on the ROC and shift on the digital levels of the data. Also, at such high noise levels it is impossible to avoid cross-talk between the analog and the digital parts of the circuit and the analog part is therefore also affected. Due to the extremely robustness to noise on the digital lines the focus of the tests was shifted to the analog power supply.

The analog power supply was investigated for noise immunity and show to be very robust to noise at lower frequencies but susceptible to frequencies superior to 3 MHz as shown on Figure 2 and Figure 3. The effects show on figures 2 and 3 where observed with a tone frequency representing 5% of the voltage being transmitted to the analog line.

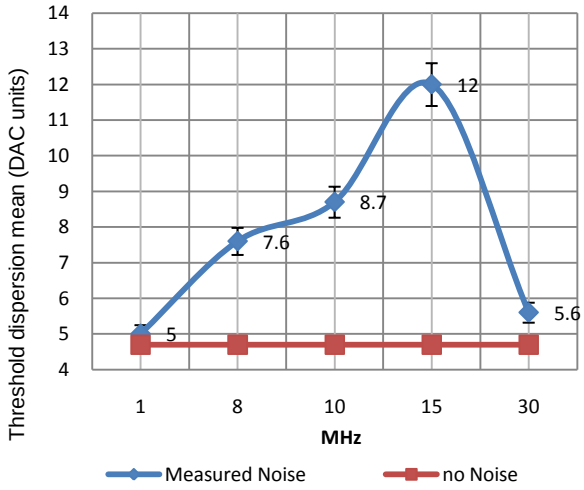

Figure 2. Threshold dispersion mean measurements with and without noise injected.

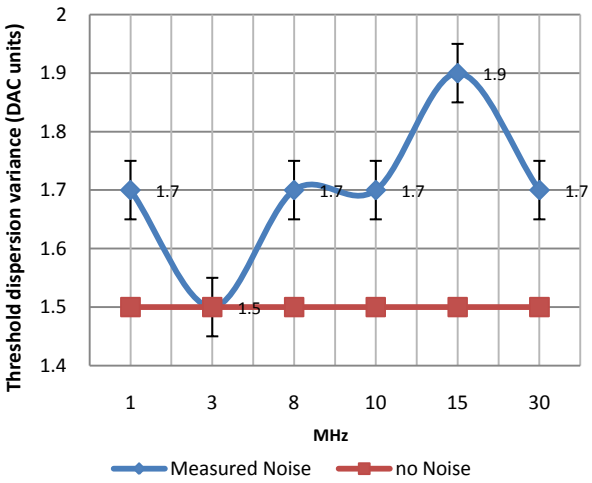

Figure 3. Threshold dispersion variation measurement with and without injected noise.

The influence of the noise amplitude is well portrayed by Figure 4, and it can be scaled to account also the frequency using the results obtained by Figures 2 and 3.

The main objective of these studies was to evaluate how

much noise the power lines can take in order to provide references to new methods of providing power to the CMS pixel readout system, one of such method is DC-DC conversion. Based on this results DC-DC conversion should be possible without compromising the performance of the system. Tests with commercial DC-DC step down inductor based regulator were performed to confirm that this kind of powering scheme is feasible for future upgrades on the power system.

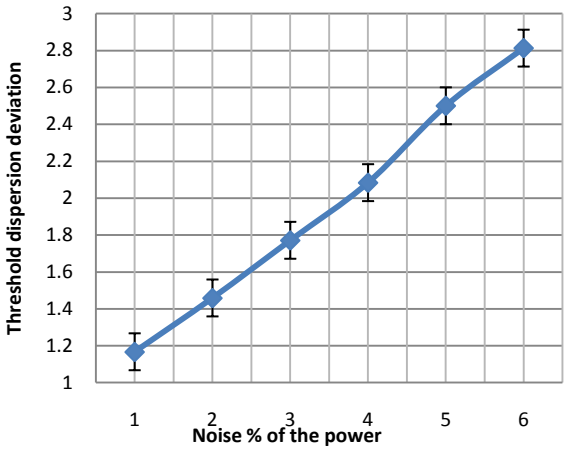

Figure 4. Varying injected noise and measurements on its impact on threshold dispersion deviation.

IV. DC-DC Integration

DC-DC converters are inserted on the existing power network in order to increase the efficiency of the power distribution by transmitting power on higher voltage levels and performing a step-down conversion nearby the detector modules. Figure 5, illustrates the proposed power network distribution with the DC-DC converters residing on the filter board. The converter resides 50 centimeters from the detector modules in order to reduce the impact of radiation on the converter.

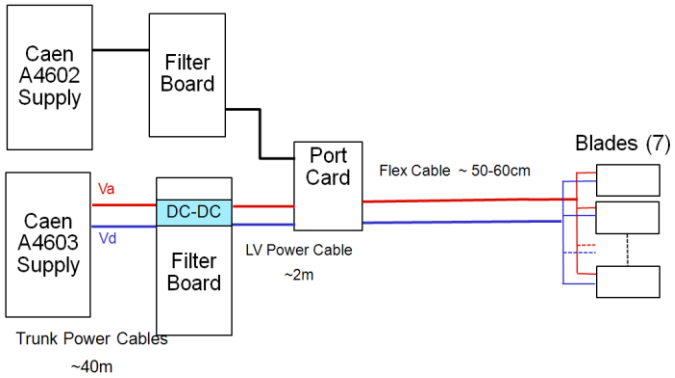

Figure 5. Proposed power distribution network with DC-DC converters.

The estimated current consumptions for the upgraded detector modules with 224 ROCs are as follows: analog current consumption 5.6A at 1.6V and digital current consumption is 8.6A at 2.6V. We have performed a DC analysis on the power network to understand the implications of the DC-DC converter on the system's power dissipation. The analysis was performed as shown in Figure 6. The impedance values are obtained from extracting cables parasitic as shown in Table 2. Table 3 summarizes our calculations.

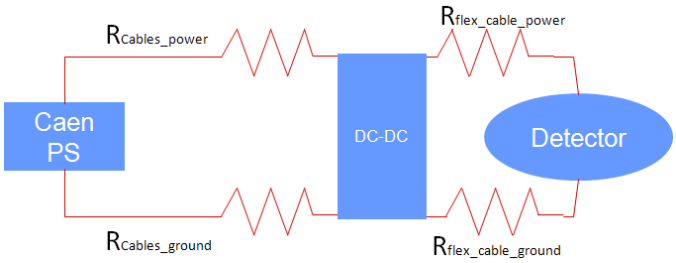

Figure 6. Power network model with extracted parasitic of the cables.

TABLE 2. Parameters for cables parasitic.

Parameters	Analog	Digital
Rcables_power	0.27Ω	0.168Ω
Rcables_ground	0.255Ω	0.153Ω
Rflex_cable_power	0.031Ω	0.031Ω
Rflex_cable_ground	0.004Ω	0.004Ω

TABLE 3. Power loss from DC-DC converter to detector module.

Power	DC-DC out	Flex Cables	Detector
Analog	10W	1.1W	8.96W
Digital	25W	2.58W	22.36W

On Table 3, we derived the amount of power required from the detector and the power loss on cables, which is the amount of output power that DC-DC converter should deliver. The input power of the DC-DC converter varies depending on its efficiency. The derivations of Table 3 show only the power consumptions for the right hand side portion of the circuit in Figure 6. The left portion of the circuit can be solved to derive the current flow on the system as a function of the power supply input voltage. The system can be described using KCL equation as:

$$V_{caen} i = i^2 R_{cables} + P_{DC-DC\_in} \quad (2)$$

where $P_{DC-DC\_in} = P_{DC-DC\_out}/\rho$ and ρ is the DC-DC converter efficiency. Utilizing Eq2, we can derive the current flow, voltage drop and power loss on the cables. The power loss on the system is derived as:

$$P_{loss\_with\_dc} = \sum_i P_{cables_i} + P_{dc\_loss} \quad (3)$$

where $P_{dc\_loss} = P_{DC-DC\_in} - P_{DC-DC\_out}$. We further compare the power gain between current power scheme (without dc-dc conversion) and the proposed DC-DC powering scheme as:

$$P_{gain} = (P_{loss\_no\_dc} - P_{loss\_with\_dc})/P_{loss\_no\_dc} \quad (4)$$

Utilizing these formulas, we can compute the power gain as a function of DC-DC converter efficiency for both analog and digital power lines. Figures 7 and 8 show the plots of power gain with respect to different input voltages from power supply while varying the DC-DC efficiency rates.

As shown in Figure 7, we notice that for certain DC-DC converter efficiencies, the power gain is negative. Negative power gain means that the power loss with DC-DC powering scheme is larger than the existing scheme without any

converters. As the efficiency increases, the power gain increases and we start to observe a positive power gain. We have highlighted the 7V case, as this is the specified input voltage that current power supply can provide to the digital power line. Thus, for an input voltage of 7V, the DC-DC converter efficiency should be greater than 0.78, to obtain a power gain up to 12%. Additionally, we observe that as the input voltage increases, the power gain starts to saturate. As the input voltage increases, the current flowing on the cables decreases, thus, the voltage drop on the cables reduces drastically, therefore the power loss on the DC-DC converter start to dominate, which explains the curvature of the plots.

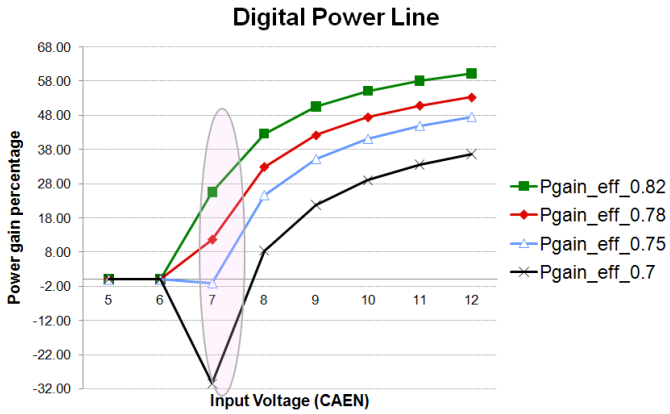

Figure 7. Power gain vs. power supply input voltage for various DC-DC converter efficiency rates for the digital power line.

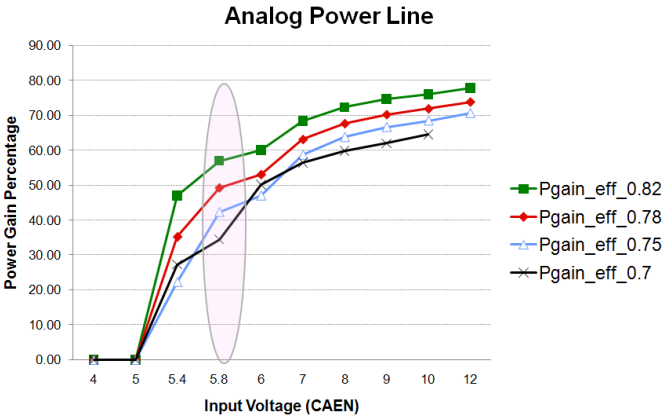

Figure 8. Power gain vs. CAEN input voltage for various DC-DC converter efficiency rates for analog power line.

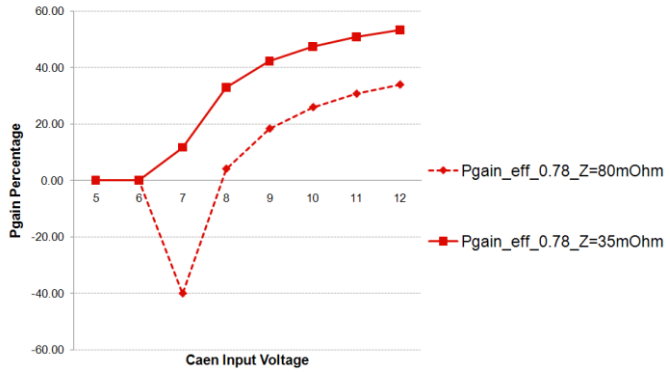

Figure 9. Impact of flex cable impedance on the power gain for 0.78 DC-DC converter efficiency while varying analog input voltage.

For the analog power line, the gain is much higher than for the digital power line. Figure 8, shows that the analog power line is more tolerant than the digital power line to lower DC-DC converter efficiencies. The input voltage that power supply can provide is up to 5.8V for the analog line, and we have highlighted this case. We observe that for this case, with an efficiency of 0.78, a power gain of up to 50% can be achieved.

Additionally, we investigate the importance of the flex cable parasitics on the DC-DC converter efficiency. In Figure 9, we show the plot of power gain vs. power supply input voltage as a function of different impedance values for the flex cable that connects the converter to the pixel modules. The parasitics of the flex cable play an important role on the amount of power required for the DC-DC. This parasitic impedance is not negligible and might have a negative impact on the DC-DC powering scheme. As shown in Figure 9, we observe that higher impedances on the flex cable result into higher voltage drop and consequently larger power loss. To compensate for these losses, a larger power supply input voltage would be needed. This is also portrayed in the Figure 9, where the plot with higher flex circuit impedance values seem to be skewed to the right by 1.5V. From this analysis, we also derive that the efficiency of the DC-DC converter would also have to increase to accommodate for the larger power losses.

V. CONCLUSIONS

In this work, we performed several power distribution studies for the CMS Forward Tracker. We performed power supply noise sensitivities studies, to derive the boundaries that power supply noise start to impact the pixel and readout chip performance. We also performed a detailed study of the proposed upgrades for the CMS Forward Tracker power network using DC-DC powering scheme. We derived the conditions for voltage drop and power loss on the systems for both analog and digital power line and the limitations of the DC-DC converter efficiency in power loss reductions. Our future work will focus on system level test of the DC-DC converters driving detector modules and performing noise and performance characterization. To supplement these efforts, we will develop a simulation platform to allow transient power analysis to study noise sensitivities, voltage drop and power-up issues.

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