



HAL
open science

Low-cost functional test of a 2.4 GHz OQPSK transmitter using standard digital ATE

Thibault Vayssade, Florence Azaïs, Laurent Latorre, Francois Lefèvre

► To cite this version:

Thibault Vayssade, Florence Azaïs, Laurent Latorre, Francois Lefèvre. Low-cost functional test of a 2.4 GHz OQPSK transmitter using standard digital ATE. IOLTS: International On-Line Testing Symposium, Jul 2018, Platja d'Aro, Spain. pp.17-22, 10.1109/IOLTS.2018.8474229 . lirmm-01997910

HAL Id: lirmm-01997910

<https://hal-lirmm.ccsd.cnrs.fr/lirmm-01997910>

Submitted on 29 Jan 2019

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Low-cost functional test of a 2.4 GHz OQPSK transmitter using standard digital ATE

T. Vayssade^(1,2), F. Azais⁽¹⁾, L. Latorre⁽¹⁾, F. Lefevre⁽²⁾

⁽¹⁾ LIRMM, Univ. Montpellier, CNRS, 161 rue Ada, Montpellier, France

⁽²⁾ NXP Semiconductors, 2 Espl. Anton Phillips, 14000 Caen, France

Abstract— This paper presents a low-cost solution to implement a functional test for RF ZigBee transmitter. More precisely, the objective is to enable symbol error detection for a 2.4GHz OQPSK-modulated signal with half sine pulse shaping on a digital ATE. The test is based on 1-bit under-sampled acquisition of the RF signal with a standard digital tester channel. A dedicated post-processing algorithm is then applied, which (i) extracts the phase information from the captured binary sequence, (ii) reconstructs the RF modulated signal and (iii) performs the demodulation. The different steps of the post-processing algorithm are detailed in this paper. Simulation and experimental results are presented, demonstrating the ability of the technique to correctly retrieve the emitted symbol sequence using only the binary data captured by the digital tester channel.

Keywords—RF test; Zigbee; digital modulation; OQPSK; 1-bit acquisition, digital signal processing, digital ATE

I. INTRODUCTION

The booming of the Internet of Things (IoT) leads to a growth of the Radio-Frequency (RF) market and to the necessity to lower the production costs of RF devices. In particular, there is a strong demand to reduce the testing costs of such devices [1], which significantly contribute to the global production costs. Indeed, the test of a RF circuit usually involves the use of an ATE equipped with high-performance analog/RF test instruments. These resources are extremely expensive compared to their digital counterpart, resulting in high testing costs. Moreover, they are usually available in a small number of channels, thus reducing multi-site efficiency.

In this context, some works can be recently found in the literature targeting the development of test solutions based on the use of a digital ATE. In [2], a reference RF transceiver is used to handle test signal generation/reception, accompanied by a FPGA that interfaces the reference transceiver with the digital ATE. In [3], the digital processor embedded in a radio SoC is used to implement a self-test and only low-speed digital signals have to be processed by the digital ATE. In [4], a digital ATE system is developed for RF devices with QAM single interfaces based on the concept of direct modulation/demodulation with multi-level drivers and comparators.

In this work, we target the implementation of a test solution for ZigBee transceivers using only standard digital ATE. Indeed, ZigBee devices are today used in an increasing number of applications, such as home automation, smart energy, telecom services, medical data collection, wireless sensor networks... Our objective is to develop a low-cost test solution for these products, and more specifically the implementation of

a functional test which has been identified as a critical challenge by the International Technology Roadmap for Semiconductors (ITRS) [5].

The paper is organized as follows. In section II, we briefly introduce the main characteristics of the RF signal generated by a ZigBee transmitter. Section III describes the conventional practice for testing such circuits and introduces the principle of the proposed technique. The development of the post-processing algorithm is then detailed in Section IV. Finally, before conclusion, simulation and hardware experimental results are presented in section V.

II. SIGNAL UNDER TEST CHARACTERISTICS

In this paper, we target the functional test of a ZigBee transmitter. All parameters (modulation scheme, spreading method, operating frequency, symbol rate, ...) are set as specified in IEEE Std 802.15.4™. More specifically, we focus on the test of such device in the 2.4 GHz band, which is an ISM band accepted worldwide. In this band, the modulation scheme is Offset Quadrature Phase Shift Keying (OQPSK) with half sine pulse shaping, the coding method is Direct Sequence Spread Spectrum (DSSS) and the data rate is 250 kb/s. Basics of the modulation scheme and spreading method are given in this section, together with the signal characteristics.

A. QPSK and OQPSK

Quadrature-phase shift keying (QPSK) is a form of phase-shift keying which uses four different phase angles, usually separated by 90° spacing. The typical implementation of a QPSK modulator is given in Figure 1. The binary data stream is first split into two branches. Even bits are fed in the in-phase branch (I-branch) and odd bits in the quadrature-phase branch (Q branch). A bipolar NRZ coding is applied on each branch. The in-phase and quadrature-phase components are then modulated onto two orthogonal basis functions, i.e. the I-branch signal is multiplied by a cosine wave and the Q-branch signal by a sine wave. Finally, these two signals are summed to form the modulated QPSK signal.

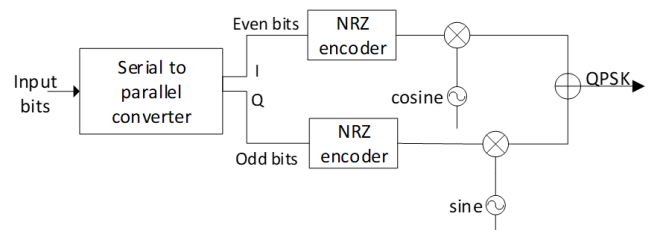


Fig. 1: Generic QPSK modulator block diagram

Note that the bit rate in QPSK is twice the symbol rate. Indeed, the binary input data are combined by groups of two bits, called symbols. The four possibilities (00, 01, 10, 11) correspond to the four possible output phases (45° , 135° , -45° , -135°).

Offset quadrature phase-shift keying (OQPSK) is a variant of QPSK where an offset of one-bit period (half symbol period) is added on the signal in the Q branch, as shown in Figure 2. Indeed, the phase jump on a QPSK signal can be 180° if a change occurs simultaneously on the signals in the I and Q branches. Such phase-shifts result in large amplitude fluctuations, which can affect the communication quality. By delaying the signal in the Q branch with one-bit period, signals in the I and Q branches will never change at the same time and phase jump is limited to 90° , as depicted in Figure 3. OQPSK therefore exhibits enhanced spectral efficiency compared to QPSK.

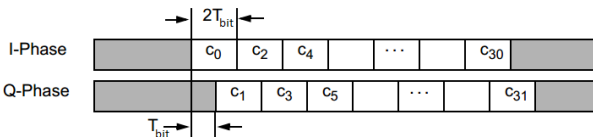


Fig.2: Offset QPSK with a delay of one bit period on the Q- signal

B. OQPSK with half sine pulse shaping

Another feature specified by the standard 802.15.4 is the use of half-sine pulse shaping, which avoids overtones resulting from fluctuating modulation envelope and sharp phase transitions. More precisely, the NRZ data (-1,1) is transformed with a half sine pulse shaping prior to multiplication by the carrier, as illustrated in Figure 3.

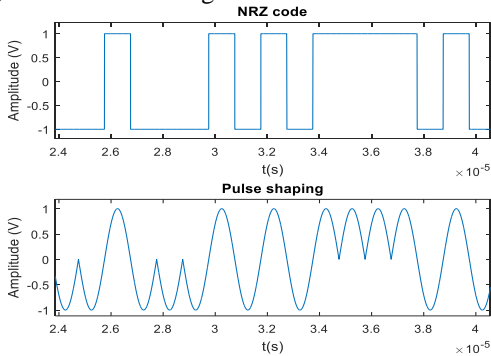


Fig.3: Half sine pulse shaping applied on NRZ data

By combining half sine pulse shaping with OQPSK, the vector diagram changes from a square to a circle (i.e. the phase is continuously travelling along the trigonometric circle) and the modulation envelope is turned into a constant. As an illustration, Figure 4 shows the effect of half sine pulse shaping on the phase of an OQPSK signal.

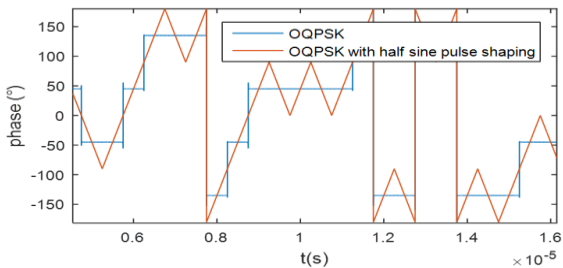


Fig.4: Phase of an OQPSK signal half sine pulse shaping

C. Direct Sequence Spread Spectrum

Finally, the last feature specified by the standard is the use of Direct Sequence Spread Spectrum (DSSS) technique. The general principle consists in multiplying the data being transmitted by a noise signal in order to reduce overall interference.

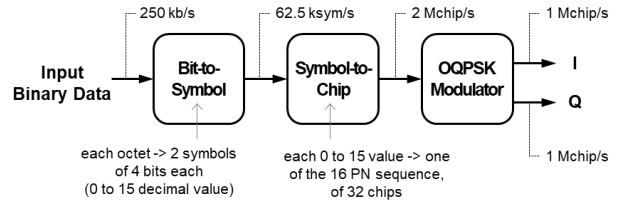


Fig.5: Coding with DSSS technique

Practically as illustrated in Figure 5, the input binary data are first converted to data symbols, i.e. each octet is divided into two symbols of 4 bits each. With a data rate of 250 kb/s, the symbol rate is therefore 62.5 ksymb/s. Each data symbol is then mapped into one of 16 pseudo-random noise sequences (DSSS sequences), composed of 32 bits (called chips) each. Finally, these chips are fed to the OQPSK modulator. The chip rate is therefore 2 Mchip/s at the input of the modulator, and 1 Mchip/s for data in the I- and -Q branches.

III. TESTING PRINCIPLE

A. Current practice

On production floor, the current industrial practice for testing RF devices consists in using an ATE equipped with RF tester channels. As illustrated in Figure 6, an RF tester channel typically comprises hardware resources that perform the down-conversion of the RF signal into an analog signal in the Intermediate Frequency (IF) band by mixing the RF signal with a local oscillator. Software DSP techniques are then applied on the digitized data stream to compute various features of the signal under test, e.g. power spectrum, constellation diagram, code domain sequences. Note that a RF tester channel allows not only to test RF functionality but also to measure RF specifications (e.g. carrier frequency, spectral leakage, EVM, and so on) [6]. In case of a functional test, only the determination of I and Q data in the code domain is required, as highlighted in Figure 6. However due to its high measurement accuracy, the cost of an RF tester channel is extremely high and constitutes a major contributor to the cost of implementing a functional test on RF devices.

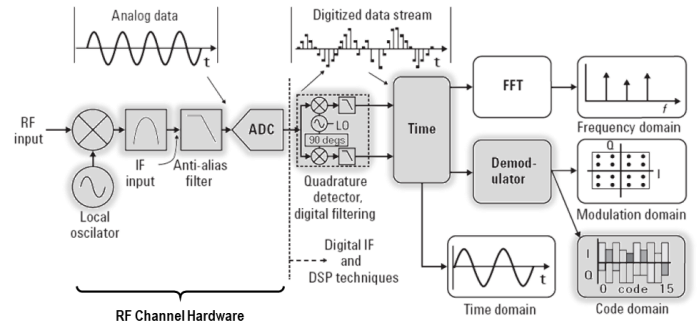


Fig.6: Current industrial setup for testing RF devices

B. Proposed technique

The proposed technique relies on signal acquisition with a standard digital tester channel instead of an expensive RF tester channel. As illustrated in Figure 7, the basic principle is to use the comparator and the latch comprised in a digital tester channel in order to perform 1-bit acquisition of the RF signal under test. A dedicated post-processing algorithm is then applied in order to retrieve I and Q data in the code domain, and therefore verify the DSSS sequence encoded in the RF signal.

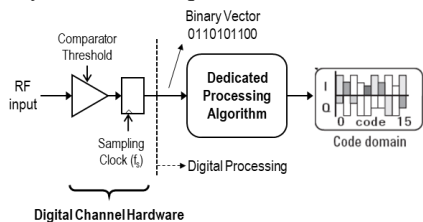


Fig.7: Industrial setup for the proposed digital technique

This strategy of using 1-bit acquisition with a digital tester channel has already been exploited in previous works to perform phase-noise characterization of signals in the IF frequency band [7,8]. Dedicated post-processing algorithms have been developed that provide retrieval of the phase noise information present in the IF signal from an oversampled 1-bit acquisition. The challenge in this work is that the signal to be analyzed is a RF signal at 2.4 GHz, which means that oversampling cannot be used. Indeed, the maximum sampling frequency of a standard digital channel is typically 1.6 GHz. High-speed digital channels that can operate at higher frequency exist, but they are more expensive. With the objective of a low-cost functional test, we focus on a solution that can be implemented using only standard digital channels, so with a sampling frequency below 1.6 GHz.

In this context, the technique proposed in this paper relies on undersampled 1-bit acquisition. The principle is derived from the technique exploited in [9,10] to perform precise on-chip timing measurements on high speed digital signals. In those papers, the idea is to sample the high-speed digital signal with a frequency f_0 by a slightly lower clock frequency f_s . The resulting signal is a digital signal with a fundamental beat frequency at $f_b = f_0 - f_s$. So essentially, this undersampling process translates the signal to be measured from a high frequency to a low frequency.

For our practical case, we cannot directly implement this solution because the RF signal frequency at 2.4 GHz exceeds the sampling capabilities of a standard digital tester channel. Instead, we propose to perform 1-bit acquisition (with the comparator threshold set to 0 V) of the RF signal at a sampling rate close to a sub-multiple of the signal frequency $f_s = f_c/n + f_d$, where f_d is the frequency deviation from the sub-multiple of the carrier frequency. The resulting signal is a digital signal with a fundamental beat frequency $f_b = |nf_s - f_c| = n|f_d|$, which contains the information related to the phase of the original RF signal. Software post-process is then applied to this low frequency digital signal in order to retrieve I and Q data in the code domain. Details on the software post-process are given in the following section.

Note that in our practical case, the use of $n = 2$ is sufficient to satisfy the constraint on the maximum data rate of a standard digital test channel. In the remaining of the paper, we will consider $n = 2$.

IV. POST-PROCESSING ALGORITHM

The software post-process applied on the binary data captured by the digital tester channel comprises three major steps as illustrated in Figure 8. The first step is to extract the information related to the phase of the original RF signal from the binary vector. Based on this result, the second step consists in reconstructing the analog RF waveform. Finally, the last step consists in performing demodulation of the reconstructed RF waveform. Each one of these steps are detailed hereafter.

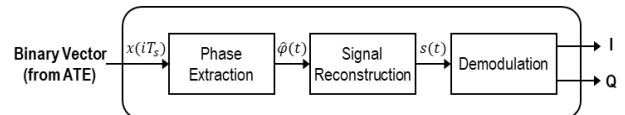


Fig.8: Processing steps for the determination of I and Q data from the binary vector captured by the ATE

A. Phase extraction

The goal of the first step is to retrieve the phase variation of the modulated signal from the binary vector captured by the ATE. This phase variation will then be used to build a reconstructed RF modulated signal.

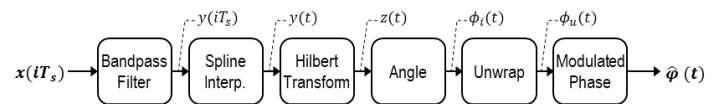


Fig.9: Phase extraction from the binary vector captured by the ATE

Practically, the binary vector captured by the ATE is considered as a sampled square wave $x(iT_s)$ (with $T_s = 1/f_s$ the sampling period) with a fundamental beat frequency $f_b = |2f_s - f_c|$. This signal is processed through a number of operations as illustrated in Figure 9.

First, the discrete-time signal $x(iT_s)$ is filtered by passing through a band pass filter centered on the square wave beat frequency in order to eliminate the harmonics introduced by 1-bit quantization. The resulting signal is a discrete-time sine wave $y(iT_s)$. Spline interpolation is applied to this signal in order to convert it into a continuous-time signal $y(t)$. In the following step, the Hilbert Transform is computed in order to derive the analytic representation of the signal in the complex plane:

$$z(t) = y(t) + jHT[y(t)] \quad (1)$$

The instantaneous phase is then obtained with:

$$\Phi_i(t) = \text{atan} \left(\frac{HT[y(t)]}{y(t)} \right) \quad (2)$$

Note that due to the atan function, the computed instantaneous phase is a wrapped phase. By unwrapping $\Phi_i(t)$, we obtain a linear evolution of the instantaneous phase $\Phi_u(t)$, which can be expressed as:

$$\Phi_u(t) = 2\pi f_b t + \varphi(t) \quad (3)$$

where the first term corresponds to the linear phase of a signal with a fundamental beat frequency f_b and the second term actually corresponds to the phase fluctuation $\varphi(t)$ of the modulated RF signal.

Finally, by using the theoretical value of the fundamental beat frequency and subtracting the first term, an estimation of the phase of the modulated RF signal is given by:

$$\hat{\varphi}(t) = \Phi_u(t) - 2\pi|2f_s - f_c|t \quad (4)$$

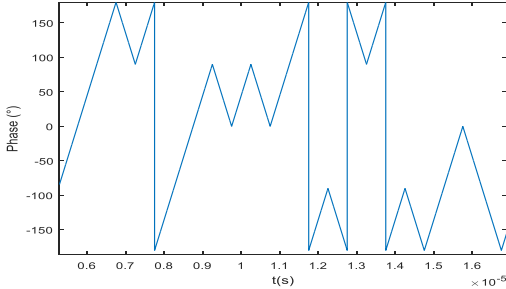


Fig.10: Estimated phase of the modulated RF signal $\hat{\varphi}(t)$

An illustration of this phase estimation is given in Figure 10. Note that the undersampling process introduces a quantization in the estimation of the phase fluctuation. The quantization step is directly related to the frequency deviation between sampling frequency f_s and half the carrier frequency $f_c/2$ with:

$$Q_{\hat{\varphi}} = 180^\circ * \frac{|f_s - \frac{f_c}{2}|}{f_s} = 180^\circ * \frac{|f_d|}{f_s} \quad (5)$$

B. Signal reconstruction

Once the phase fluctuation of the modulated signal is estimated, the emitted RF signal can be easily reconstructed by adding this fluctuation to the ideal instantaneous linear phase of the carrier:

$$s(t) = \sin(2\pi f_c t \pm \hat{\varphi}(t)) \quad (6)$$

Note that depending whether the sampling frequency is chosen with a positive or negative deviation with respect to the carrier half-frequency, the estimated phase should be added or subtracted. In particular, $\hat{\varphi}(t)$ must be subtracted if $f_s > f_c/2$, and added otherwise.

At this point, it should be pointed out that ideal conditions have been assumed for phase estimation of the modulated signal, i.e. the carrier frequency is exactly known and there is a perfect synchronization between the ATE sampling frequency and the carrier frequency of the signal under test. Under such conditions, the estimated phase actually matches the actual phase of the modulated signal. However, such conditions are not easy to achieve in a practical environment. More likely, there will be an offset between the ideal carrier frequency and the actual one. In the same way, synchronization between the ATE sampling frequency and the signal carrier frequency might not be perfect or even not possible. These imperfections will actually introduce errors in the phase estimation, which can be expressed by:

$$\hat{\varphi}(t) = \varphi(t) + 2\pi f_{off} t + \varphi_0 \quad (7)$$

where $\varphi(t)$ is the actual phase fluctuation of the modulated RF signal, f_{off} is the frequency offset between the theoretical

carrier frequency and the actual one, and φ_0 is an unknown phase offset related to unperfected or absent synchronization.

From Eq.(5), it is clear that the reconstructed RF signal incorporates these imperfections. It is therefore mandatory to take into account this element for the demodulation process.

C. Demodulation

The demodulation of the reconstructed RF signal involves several steps, as depicted in Figure 11. First, I and Q time-domain waveforms have to be recovered from the time-domain reconstructed RF signal. The following step is then to extract I and Q binary data. Finally, parallel to serial conversion and ambiguity determination are applied to obtain the demodulated sequence.

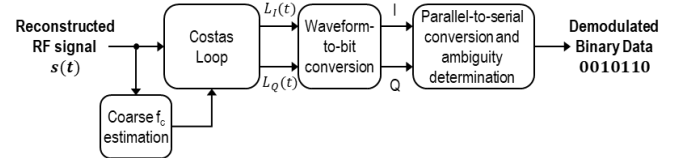


Fig.11: Demodulation from the reconstructed RF signal

1) Extraction of I and Q time-domain waveforms

To ensure proper demodulation, frequency and phase offsets present in the signal captured by the tester must be estimated to recover the carrier signal and permit coherent demodulation. Indeed, they can cause a rotation of the constellation and entail errors in the demodulated data.

A classical technique to perform carrier recovery on QSPK modulated signals is the multiply-filter-divide technique, where the fourth power of the signal is computed to produce a signal with a harmonic component at $4f_c$ and no phase modulation; this component is then filtered and divided by 4 to recover f_c . This technique can also apply for OQPSK modulated signals but not for QPSK modulated signals with half sine pulse shaping, because of the continuous phase evolution instead of sharp transitions between the phase values.

Another possibility is the use of a Costas loop, which performs carrier frequency and phase recovery as well as demodulation. A Costas loop is a PLL-based circuit that uses coherent quadrature signals to measure phase error; this phase error is used to regulate the loop's oscillator. When locked, quadrature signals correspond to the demodulated data.

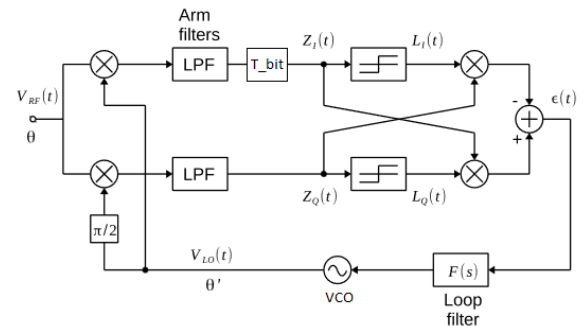


Fig.12: Modified Costas loop for OQPSK with pulse shaping

In this work, we use a software model of the Costas loop based on the design proposed in [11] for QPSK modulation, but adapted to be able to manage half sine pulse shaping. The

modified architecture is given in Figure 12. The incoming RF signal is split in two I and Q branches. Signals on the I and Q branches are then respectively multiplied by a signal tone generated by a Voltage Controlled Oscillator (VCO) and a 90° shifted version of the signal. Low pass filtering removes the double frequency component to complete demodulation. In the specific context of OQPSK with half sine pulse shaping, a delay of one-bit period (T_{bit}) is added on the I branch to compensate for the delay that has been added on the Q branch during the modulation process. Note that this delay is only necessary if pulse shaping is used. By calculating the difference between the absolute value of the demodulated I branch and Q branch, an error is obtained. This error passes through a loop filter and drives the VCO to achieve phase and frequency locking. In the locked state, L_I and L_Q signals actually corresponds to reconstructed waveforms of the I and Q signals generated within the transmitter during the modulation process.

Note that to improve the locking of the Costas loop, the VCO initial frequency should be close to the actual carrier frequency of the incoming signal. With this objective, we have implemented a first step which permits to have an estimation of this frequency. More precisely, we compute the spectrum of the squared RF signal, which exhibits two main components located at $2f_c \pm f_{bit}/2$, where f_{bit} is the 2MHz bit frequency. Taking the mean of these two components, we have an estimation of twice the actual carrier frequency. The accuracy of the estimation depends on FFT resolution but is typically in the range of few kHz. This estimation is not precise enough to perform correct demodulation but constitutes a useful data to set the VCO initial frequency.

2) Waveform-to-bit conversion and ambiguity determination

Finally, the last steps of the procedure consist in converting the reconstructed I and Q waveforms into a binary format and generating the demodulated data. Conversion to binary format is simply realized by performing a zero-crossing and selecting one value each T_{bit} time interval. Parallel-to-serial conversion is then realized to generate demodulated data.

However, an additional step has to be implemented to confirm the generation of demodulated data in order to palliate a weakness of the Costas loop, which locks with a $k * \pi/2$ phase ambiguity. As a consequence, the determined values for I and Q data might be complemented or not. This produces four possible combinations for the demodulated data, i.e. IQ , $\bar{I}Q$, $I\bar{Q}$ and $\bar{I}\bar{Q}$. To raise this phase ambiguity, we actually search for existing DSSS sequences in the demodulated data assuming the four combinations. When a match is found, ambiguity is raised and the corresponding combination is retained.

V. VALIDATION

The software post-processing has been implemented in Matlab/Simulink®. The signal to be analyzed is a OQPSK modulated signal with a carrier frequency $f_c = 2.405 \text{ GHz}$. Undersampled 1-bit acquisition is performed with a sampling frequency $f_s = 1.21212 \text{ GHz}$, which corresponds to a frequency deviation $f_d = 9.62 \text{ MHz}$. The spectrum of the

signal is therefore transposed around $2f_d = 19.2 \text{ MHz}$. Note that according to Eq.(5), the smaller the frequency deviation f_d , the smaller the quantization step $Q_{\hat{\phi}}$ in the phase estimation and the more precise the signal reconstruction. On the other hand, the frequency deviation should not be too small in order to preserve the measurement bandwidth, i.e. the fundamental frequency of the transposed spectrum must be higher than the chip rate of 2 MHz. Here with $f_d = 9.62 \text{ MHz}$, we have a sufficient margin with respect to the chip rate and a satisfactorily small quantization step $Q_{\hat{\phi}} = 1.4^\circ$.

A. Simulation results

To validate the technique, we have first considered a simulated signal generated using a model for the Circuit Under Test. This model consists in a OQPSK modulator with half sine pulse shaping, as depicted in Figure 13. The key interest of using a simulated signal is that we perfectly control its characteristics. Moreover, we have also access to internal information, e.g. the time-domain $I(t)$ and $Q(t)$ signals, which are not generally available when dealing with the RF signal generated by a physical circuit.

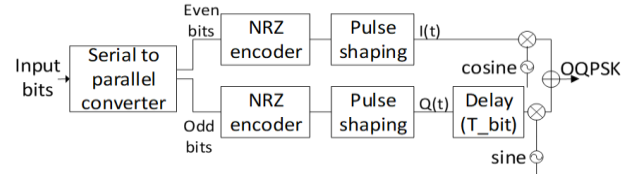


Fig.13: OQPSK modulator with half sine pulse shaping

The generated RF signal has been converted into a square-wave signal using zero-crossing and sampled at f_s rate. The different steps of the post-processing algorithm have then been applied on the undersampled square wave.

The result of the phase extraction process is shown in Figure 14, which compares the phase of the RF signal generated by the OQPSK modulator to the phase estimated from the analysis of the undersampled square-wave. A very good agreement can be observed with a difference that remains below the theoretical quantification error $Q_{\hat{\phi}}$ of 1.4° , demonstrating the ability of the technique to perform accurate phase estimation.

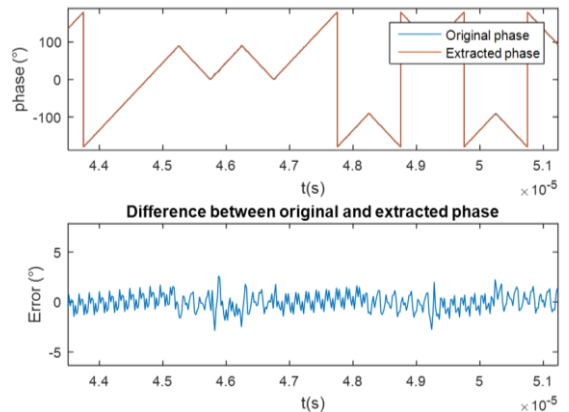


Fig.14: Comparison between original and extracted phase

The result of the demodulation process is illustrated in Figure 15, which compares the waveform $I(t)$ present in the

modulator to the waveform $L_I(t)$ reconstructed from the analysis of the undersampled square-wave. Here again a very good agreement is observed with an rms error of 1.66% and a maximum error that does not exceed 5%.

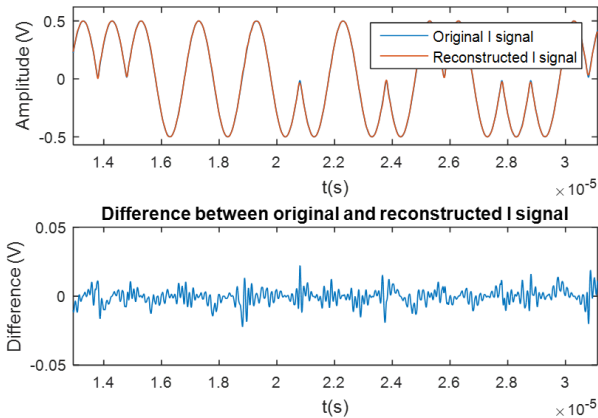


Fig.15: Comparison between original and reconstructed I-waveforms

B. Experimental results

To further validate the technique, the post-processing algorithm has also been applied on NXP ZigBee transceiver. Practically, a test pattern composed of the 16 DSSS sequences has been applied to the transmitting chain and the TX RF port has been captured with a standard digital channel of V93000 ATE (PS 1600 Pin Scale), with a sampling frequency $f_s = 1.21212$ GHz. Data are then transferred from the ATE to a PC to perform the software post-process.

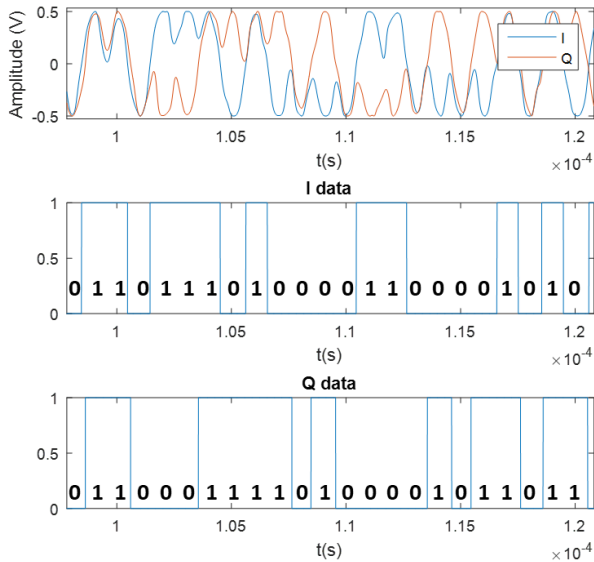


Fig.16: Demodulated chips from capture on standard digital channel

Figure 16 illustrates the result the post-processing algorithm applied on the binary data captured by the ATE. The first graph shows the reconstructed time-domain waveforms $L_I(t)$ and $L_Q(t)$. These waveforms exhibit the expected behavior of I and Q signals generated with half sine pulse shaping. The second and third graphs correspond to the binary interpretation of these signals, for I and Q data respectively. After parallel-to-serial conversion and ambiguity determination, we have been able to

recover the test pattern composed of the 16 DSSS sequences. This experiment demonstrates the validity of the proposed technique to implement a low-cost functional test for RF ZigBee transmitters using only a standard digital tester channel.

VI. CONCLUSION

In this paper, we have developed an original technique that permits to analyze 2.4 GHz signals modulated with OQPSK and half-sine pulse shaping using only standard digital test resources. It relies on undersampled 1-bit acquisition of the RF signal with a sampling frequency close to half the carrier frequency; a dedicated post-process algorithm is then applied on captured binary data which permits to retrieve the symbol sequence present in the RF modulated signal. The technique has been validated on a simulated signal using a software model of the circuit under test, and on an actual physical signal generated by a ZigBee transceiver and captured by a PS 1600 channel of V93000 ATE. To summarize, the proposed technique allows low-cost functional testing of RF ZigBee transmitters. Moreover, it offers the possibility to implement multi-site testing since digital tester channels are usually widely available on standard ATE. Future work will address the optimization of the post-processing algorithm for its practical integration on the production test flow.

ACKNOWLEDGMENT

This work has been carried out under the framework of PENTA-EUREKA project “HADES: Hierarchy-Aware and secure embedded test infrastructure for Dependability and performance Enhancement of integrated Systems”.

REFERENCES

- [1] F. Demmerle, "Integrated RF-CMOS Transceivers challenge RF Test," Proc. IEEE International Test Conference, pp. 1-8, 2006.
- [2] I. Kore et al., "Multi-site test of RF transceivers on low-cost digital ATE," Proc. IEEE International Test Conference (ITC), pp. 1-10, 2011.
- [3] C. H. Peng et al., "A novel RF self test for a combo SoC on digital ATE with multi-site applications," Proc. IEEE International Test Conference (ITC), pp. 1-8, 2014.
- [4] M. Ishida K. Ichiyama, "An ATE System for Testing RF Digital Communication Devices With QAM Signal Interfaces," IEEE Design & Test, vol. 33, no. 6, pp. 15-22, 2016.
- [5] Test and Test Equipment, International Technology Roadmap for Semiconductors 2011 Edition, 2011.
- [6] K. Ichiyama et al., "A functional test of 2-GHz/4-GHz RF digital communication device using digital tester," Proc. IEEE International Test Conference (ITC), pp. 1-10, 2013.
- [7] S. David-Grignot, F. Azais, L. Latorre, F. Lefevre, "Low-cost phase noise testing of complex RF ICs using standard digital ATE," Proc. IEEE International Test Conference (ITC), pp. 1-9, 2014.
- [8] S. David-Grignot, F. Azais, L. Latorre, F. Lefevre, "A new technique for low-cost phase noise production testing from 1-bit signal acquisition," Proc. IEEE European Test Symposium (ETS), pp. 1-6, 2015.
- [9] J-L Huang, K-T Cheng, "An on-chip short-time interval measurement technique for testing high-speed communication links," Proc. IEEE VLSI Test Symposium (VTS), pp. 380-385, 2001.
- [10] S. Sunter, A. Roy, "On-chip digital jitter measurement, from megahertz to gigahertz," IEEE Design & Test of Computers, vol. 21, no. 4, pp. 314-321, 2004.
- [11] M. Tytgat, M. Steyaert, P. Reynaert, "Time Domain Model for Costas Loop Based QPSK Receiver," PRIME; Conference on Ph.D. Research in Microelectronics & Electronics, pp. 1-4, 2012.