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Enabling deep-space CubeSat missions through state-of-the-art radiation-hardened technologies

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Abstract: This work presents a radiation-hardened reconfigurable hardware based platform to be used in deep-space cubesat missions. The platform has been designed for the in-orbit validation of two new technologies: a new radiation-hardened Field-Programmable Gate Array (FPGA) developed in France; and a CCSDS/ECSS IP Core for telemetry (TM) and telecommand (TC) designed at UFSC, Brazil. The printed circuit board (PCB) was designed following the European Space Agency (ESA) space product standards. It has a layered structure that mitigates the effects of radiation and electromagnetic interference on the components signals. All signal layers lie between power and ground planes, avoiding tracks on the outer layers. In addition, all components were selected to tolerate wide temperature variation and some even tolerate radiation – as the microcontroller (MCU) (MSP430FR6989) with ferroelectric program memory and the rad-hard FPGA (NX1H35S-BG625PR). An important architecture feature is to allow changing the hardware configuration of the FPGA through remote uplink of its Bitstream. The MCU is responsible for updating the configuration bitstream stored in a flash non-volatile memory. An aditional bitstream is also stored in the memory, as a fail-safe technique. There are three bitstream copies stored, and a voting scheme is used to ensure the data integrity, as the flash memory is susceptible to Single Event Effects (SEE). The MCU module is responsible for the housekeeping and update management of the rad-hard FPGA. The implementation stored in the FPGA includes not only the TC/TM IP core, but also an abstract execution graph, in the form of a state machine, emulating the basic functionalities of an on-board computer (OBC). The communications module handles TC and TM data and it is an interface between the radio transceiver and the emulated OBC. The emulated OBC is based on the ECSS Telemetry & Telecommand Packet Utilization Standard (PUS), and it performs the validation of the routed telecommand received, and the packaging of the telemetry data acquired by the available sensors. The proposed architecture allows testing all the implementations, exercising its functionalities, and also the module's integration as a payload of the FloripaSat mission.

1. Introduction

In the last decade there has been a significant increase of interest in small satellites, either by space agencies, industries or academia [1]. The low cost, possibility of using commercial off-the-shelf components (COTS), validating technologies and doing science are the main factors that lead to this increase in interest [2].

An emerging technology to be used also in these small satellites is reconfigurable computing and adaptive hardware. The great attraction is the possibility of implementing hardware and system-wide functional changes, transmitted remotely [3]. That is, reconfiguring the satellite with updates coming from the ground station. Usually, the component underlying this functionality is the Field Programmable Gate Array (FPGA).

At the same time, protons and electrons trapped in Earth's radiation belts, as well as cosmic rays, represent a real hazard to electronics, which must operate reliably in the natural space environment. Single-event effects (SEE) can lead to a sudden failure of the device or system, and the effects of total dose (TID) of radiation can reduce the satellite's life time [4].

The disturbing effect of radiation in electronics [5] is well known and it has been widely studied since the loss of the Telestar satellite in 1962, due to a nuclear test at high altitude. The particles of ionizing radiation and electromagnetic radiation can cause a series of sporadic, periodic or permanent damages in circuits, which could result in the loss of the device. When a high-energy particle goes through an integrated circuit junction, extra electrons and holes pairs are created along the path due to the ionization effect, as shown in Figure 1a. These extra carriers can be captured by the sensitive node nearby in two stages, ion drift Figure 1 and ion diffusion (Figure 1c), and if the amount of charge collected exceeds the charge threshold of this node, the state of it can be altered, resulting in a SEE.

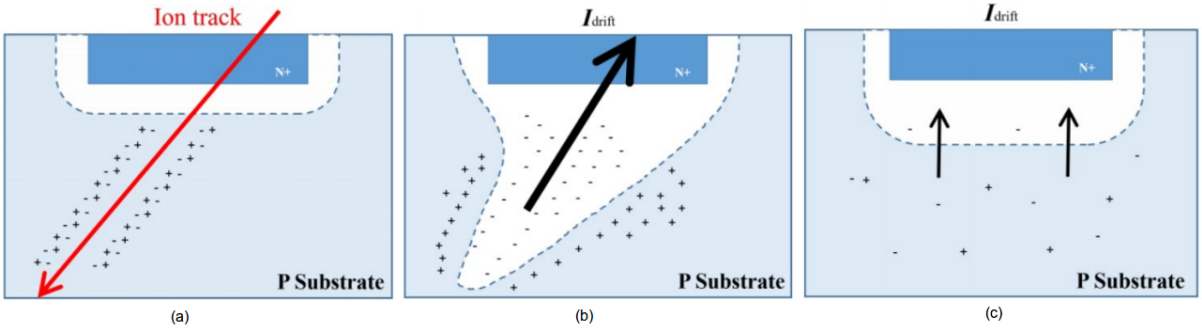

Figure 1: Radiation effect in transistors structure [6].

It is imperative to consider these effects in all the design stages of devices or electronic systems that require robustness and safety in space applications, since this is a naturally radioactive environment. Therefore, FPGAs of high performance, high density and endured to radiation are in great demand, mainly in higher orbit, long time missions, and also for deep space exploration. NanoXplore SAS designed an FPGA, which is implemented using 65nm complementary metal-oxide-semiconductor (CMOS), with radiation protection up to 100,000 Rads and 60 $MeV\ cm^2\ mg^{-1}$, multiple voltage level inputs and outputs, and double data rate type 2 (DDR2) memory support [7]. However this device has never been tested in orbit (In-orbit Validation, IoV).

The selected case study for the designed rad-hard platform is a telecommand (TC) and telemetry (TM) application for CubeSats, using the recommendations from the Consultative Committee for Space Data Systems (CCSDS). These recommendations have already been used in more than 900 space missions [8]. The standardization of communications protocols for nanosatellites has the aim to remove integration barriers between space missions. On this aspect, the idea behind this case study is to bring standardization for space communications in cubesats.

The architeture, hereinafter referred to as Payload-X, is a hardware architecture implemented in a printed circuit board (PCB), designed for a radioactive environment, having as a main feature the possibility to change the hardware configuration of the FPGA through remote uplink of its Bitstream. Also, the proposed architecture aims to be used as a payload of FloripaSat, a nanosatellite under development at the Federal University of Santa Catarina (UFSC) [9, 10, 11]. This payload will perform the IoV of the the rad-hard FPGA, and the CCSDS communications IP core. Additionally, it will use a new strategy for FPGA reconfiguration on-the-fly.

2. Architecture

An overview of the implemented architecture is presented in this section, and its block diagram is shown in Figure 2. It has a layered structure that mitigates the effects of radiation and electromagnetic

interference on the components signals, a microcontroller (MCU) model MSP430FR6989 with ferroelectric program memory, and a radiation-hardened FPGA model NX1H35S-BG625PR.

Its componentes and respective functions are described next.

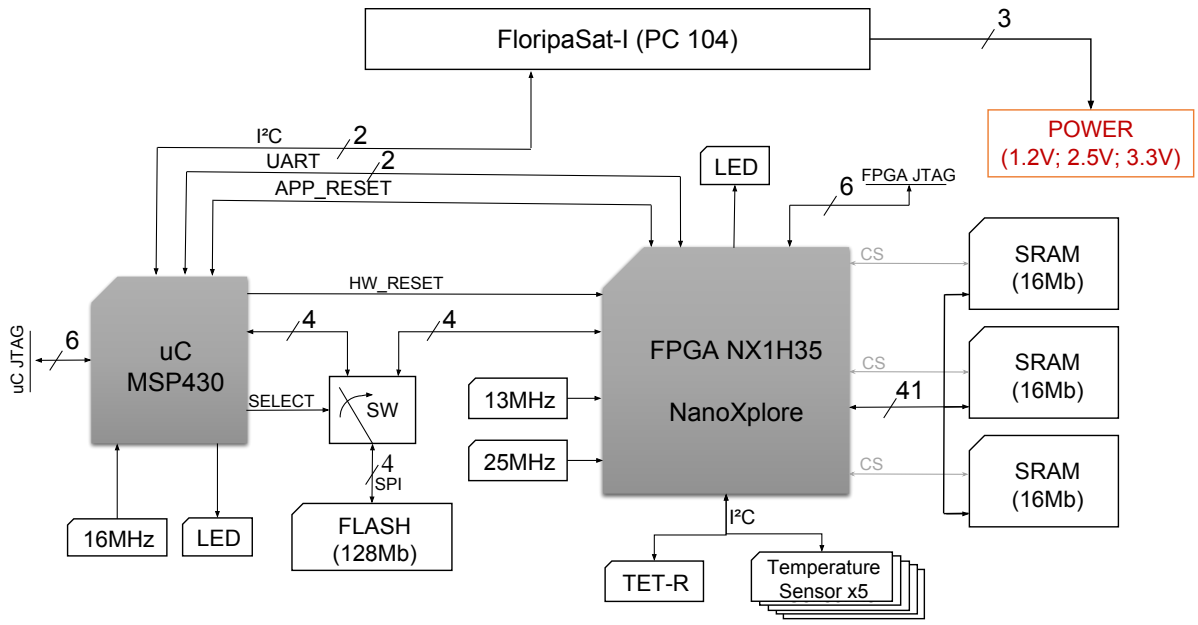

Figure 2: Interconnection diagram.

2.1. Reconfiguration and Housekeeping

Payload-X's MCU module is designated by the acronym HUMAN (Housekeeper and Update MANager), as it has 2 main purposes: manage the FPGA reconfiguration; and perform housekeeping tasks. It is a Texas Instruments MSP430FR series MCU and has an FRAM (Ferroelectric Random-Access Memory) memory to store program data. This specific technology was chosen to ensure a better tolerance against bit-flips.

While in orbit, an important feature of Payload-X is to update its operation based on a new FPGA configuration file sent from a ground station. This new configuration file (also called "bitstream") is sent split in multiple packets, where a few bytes per packet are for sequencing and error detection. HUMAN is responsible for receiving, integrity checking and storing the bitstream segments in a non-volatile memory, as well as waiting for a "commit" telecommand to change the current configuration of the FPGA to the new one.

The non-volatile memory is a flash memory. Although it is more radiation tolerant than SRAM or DRAM memories, some bit-flips are expected [12]. To ensure that data is corrected after a bit-flip occurrence, the bitstream is stored in a redundant way. There are 3 copies of the bitstream stored in different regions of the flash memory. Then, a voting scheme is used to check and correct possible errors.

Even after performing several tests, it is impossible to predict every error that could happen in orbit [13]. Thus, there is a secure fallback bitstream, so in case of a critical error in the current one, HUMAN will replace the current version, by the secure (fallback) version. Therefore, a total of 6 bitstreams, in 2 versions, are stored in the flash memory: 3 for the current configuration in use; and 3 for the fallback version.

HUMAN is also responsible for managing incoming messages to Payload-X. These messages may be related to reconfiguration, such as new bitstream segments or bitstream status requests, or may be telecommands/telemetry arriving/incoming from the communication module.

When a new bitstream segment is received from the OBDH, HUMAN should check the data integrity using the CRC technique (CRC-16-CCITT). If the segment is correct, it will be stored in the flash memory. When a telecommand is received, it is stored in FRAM memory and sent to the communications module via UART. Likewise, a telemetry sent by the communications module is stored in the FRAM memory and sent to the OBDH via I^2C.

Since there is a triple redundancy in the stored bitstreams, a HUMAN secondary activity consists of memory scanning, checking and correcting possible errors. This task is performed when nothing else is being done, such as an idle task. The HUMAN states are shown in Figure 3.

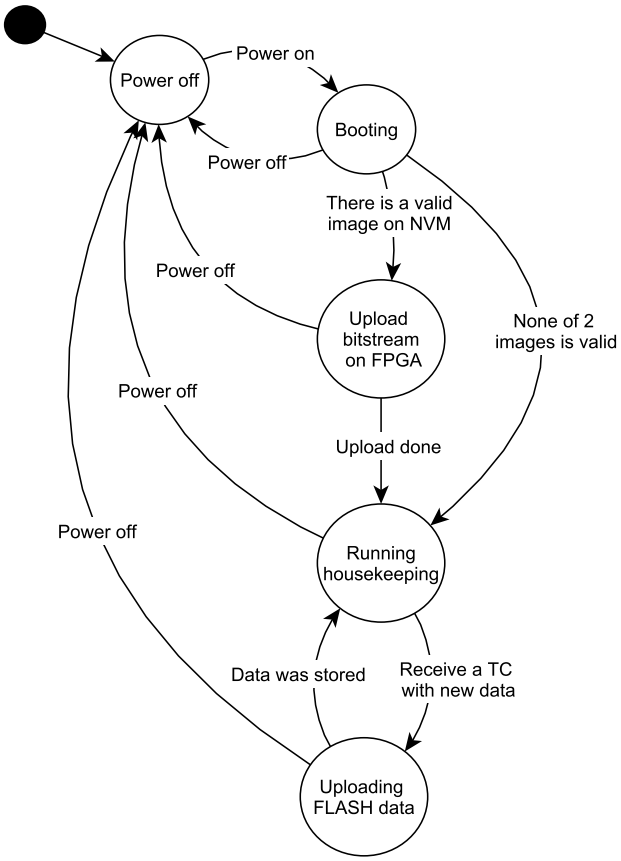

Figure 3: HUMAN state diagram.

2.2. FPGA Implementation

The FPGA implementation is divided in two main blocks. The first block handles the telecommand and telemetry flow and it is used as an interface between the transceiver and the Finite State Machine (FSM) with OBDH functionalities, denominated as the Unit of Telemetry and Telecommand (UTMC).

The second block is composed of the Payload's OBDH which handles the TM and TC packets using Space Packet Protocol, characterizing the last layer of the CCSDS/ECSS protocol. In addition, it acquires data from sensors and, afterwards, it packages the acquired data. Figure 4 presents the architecture implemented in the FPGA.

The UTMC system is divided in two segments dedicated to telemetry data processing and telecommands handlings. In the TC flow, when a TC is delivered to UTMC from the UART interface, the Command Link Transfer Unity (CLTU) is decoded using a BCH algorithm that performs error detection and correction. When a Direct TC (DTC) is detected, the UTMC delivers it to a Command Pulse Distribution Unit (CPDU) layer that interprets and generates a strictly controlled time pulse in one of the

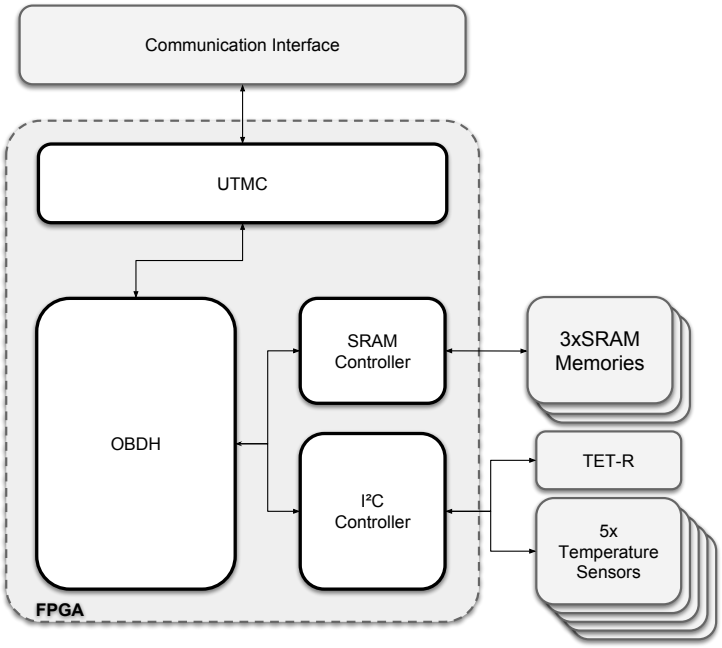

Figure 4: FPGA implementation top level diagram.

available outputs. Also, when a Routed TC (RTC) is detected, the UTMC delivers the Space Packet data to the Payload-X FSM.

Following the TM flow, the data generated by the sensors is processed in the OBDH, which creates a telemetry packet and sends it to the UTMC, then a Telemetry Transfer Frame (TMTF) is generated by the the Transfer Layer. The TMTF can be coded with Reed-Solomon, Convolutional, Reed-Solomon + Convolutional, or LDPC (Low-Density Parity-Check) algorithms, which results in the Channel Access Data Unit (CADU) that is dispatched by the UART interface. Figure 5 presents the architecture implemented by UTMC.

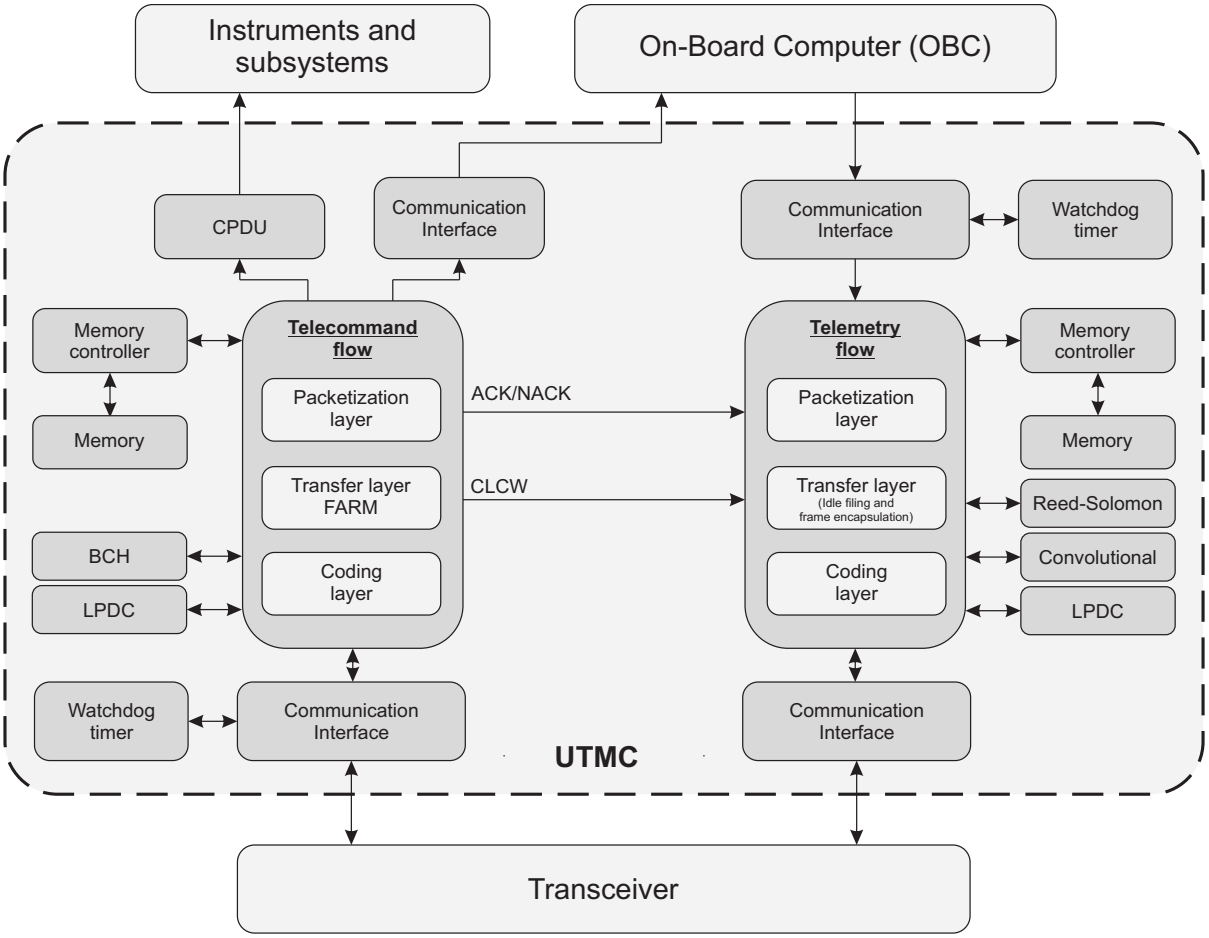

Figure 5: UTMC top level diagram.

The OBDH system has the architecture presented in Figure 6. All telecommands received from UTCM are verified and a report is generated by the Verify layer, in case the TC is inconsistent. The received TC is routed to its destination by the Route layer and could be delivery to Device Control, Test or Configure. The Device Control layer has two main functions, the first is to receive the sensors data, and to deliver it to the Packing layer. The second fucntion is to execute a direct telecommand.

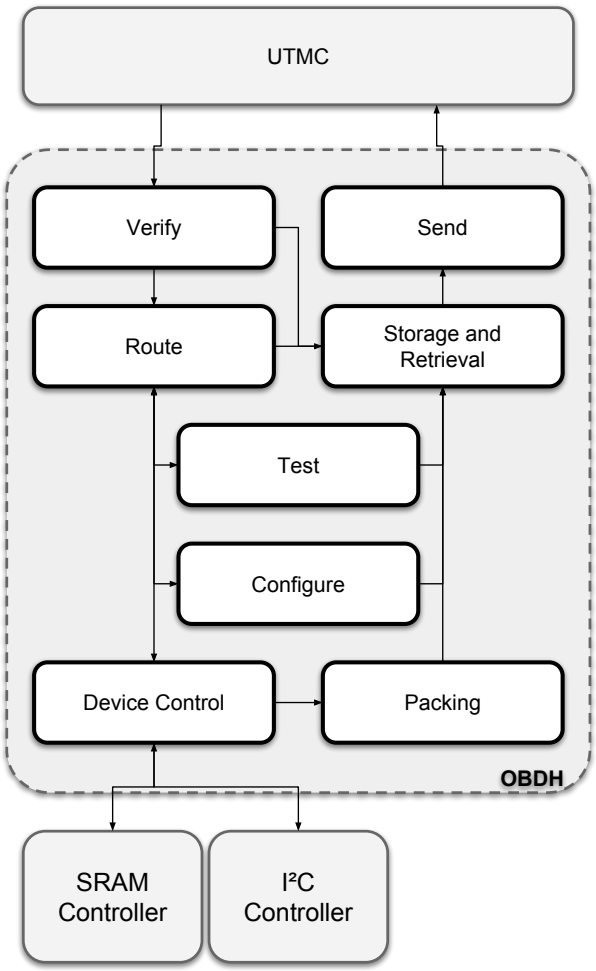

Figure 6: Payload-X OBDH top level diagram.

The Configure layer defines the parameters of system execution (e.g. temperature data acquisition interval) and it makes possible to change these parameters by a TC. The test layer executes test functions and generates a report on the test status.

All reports generated by this layers are dispatched to Storage and Retrieval, then, this layer forwards the full telemetry data by request or when the data limit is achieved. The Send layer uses a UART interface to communicate with the UTMC.

3. Board Implementation

Figure 7 shows a rendering of the developed board, with all the components and interfaces. The board was designed considering that the space environment is much more severe than the terrestrial environment, given high thermal variations coupled with low heat dissipation and high radioactive levels. Therefore, several extra precautions must be taken in the making of space PCBs.

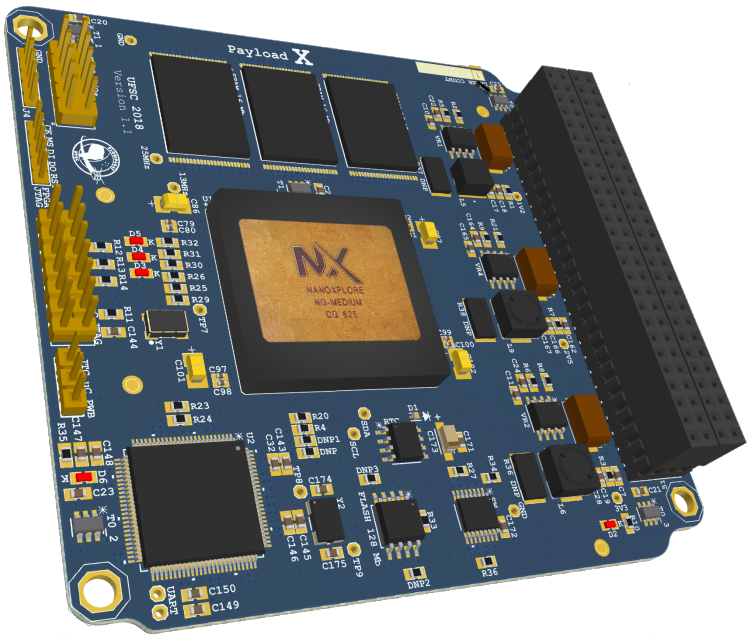

Figure 7: PCB 3D rendering.

In [14], the author developed PCBs to perform radiation effects tests on ICs. For that purpose, it was necessary to implement a PCB structure that isolated from the radioactive effects all circuits except the IC under test. Based on the IEC 62.132-1 standard all layers of the PCB were inserted between layers of VCC and or GND, minimizing routing tracks in the top or bottom layer. Therefore, a similar structure was applied in Payload-X's board layers.

In addition, due to the high thermal variability, great attention was given to the differences in the thermal expansion coefficient of the various components and materials used in the board. Heat dissipation was also considered, as it occurs only by conduction losses and radiation. Also, since electronic space application devices will inevitably be subjected to launch, then soldering, component placement and mechanical fastening points must be properly done to withstand intense vibrations.

Beyond all that, the PCB was designed following the European Space Agency (ESA) design rules for printed circuit boards ECSS-Q-ST-70-12C [15].

4. Conclusion

This paper presented a radiation-hardened reconfigurable hardware architecture to implement a telecommand and telemetry module in CubeSats, called Payload-X. The developed architecture consists of a PCB board designed to be radiation-hardened, an MCU to manage the reconfiguration process, and a radiation-hardned FPGA responsible for implementing the telecommand and telemetry module.

The architecture will be used for the in-orbit validation of two new technologies: the new BRAVE FPGA developed in France; and an IP Core for telemetry and telecommand following the CCSDS standard. This process will be handled along the FloripaSat mission of the Federal University of Santa Catarina, in the form of a payload. The FloripaSat-I consists of a 1U CubeSat with five functional modules: EPS; OBDH; TT&C; battery and interface board, besides the payload modules where the Payload-X is integrated. FloripaSat-I will be lunched as a piggyback of the CBERS-4A satellite, using the Chinese Long March 4B rocket.

Before being placed in orbit, the developed PCB board needs to be further tested in order to verify its radiation-hardened capabilities.

Acknowledgments

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