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Editorial TVLSI Positioning-Continuing and Accelerating an Upward Trajectory

Massimo Alioto, Magdy S. Abadir, Tughrul Arslan, Chirn Chye Boon,
Andreas Burg, Chip-Hong Chang, Meng-Fan Chang, Yao-Wen Chang, Poki
Chen, Pasquale Corsonello, et al.

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Editorial

TVLSI Positioning—Continuing and Accelerating an Upward Trajectory

I. VLSI SYSTEMS: A GLANCE INTO THE LAST DECADES

SINCE their inception in 1970s, VLSI systems have enabled several new technological capabilities and made them accessible to an unceasingly wider range of users, reaching a scale that has been exponentially increasing over the decades [1] (see Fig. 1). Relentless integration of more complex systems has driven such remarkable evolution, as made possible by the inexorable miniaturization. As shown in Fig. 1, more functionality has been crammed in a consistently smaller form factor, as exemplified by the physical volume shrinking of computers by 100 X/decade [2], [3]. At the same time, the energy per task has been decreasing at 10–100 X/decade, as shown in Fig. 2, for several systems and system-on-chip subsystems [4]. This allowed packing more capabilities into the same power envelope, as generally observed in the electronic systems, even before the advent of the integrated circuit [5].

On the cost side, nearly doubled system complexity has been integrated in the same silicon die area at every new technology generation. This has been achieved at marginally increased cost, thanks to the cost/transistor reduction shown in Fig. 3 [1]. Although often narrowly identified with Moore's law [6], such cost reduction trend actually transcends the CMOS technology and has started well before integrated circuits became available [7]. Indeed, this cost reduction comes from the ceaseless learning process of the semiconductor industry as a whole, from materials to devices, CAD tools, circuits, architectures, systems, algorithms, packaging, testing, and so forth. In particular, a learning rate of 55% has been historically observed from the semiconductor industry's learning curve [1], which translates into 55% cost/transistor reduction every time the overall number of manufactured transistors is doubled worldwide (which occurs every 18 months, as shown in Fig. 3). This suggests that Moore's law slowing down and eventual end of device scaling will not really affect the cost trend, as long as the same learning rate is preserved. In other words, the cost/transistor downscaling will be driven by more coordinated effort within our community, rather than mainly focusing on the device downsizing.

The above-mentioned evolution has initiated various decade-long technological waves, whose market growth has iteratively fueled the creation of the next wave (see Fig. 4). Starting from the mainframes and the minicomputers in the 1970s, VLSI systems have made personal computing available to an unprecedented wide range of nonprofessional

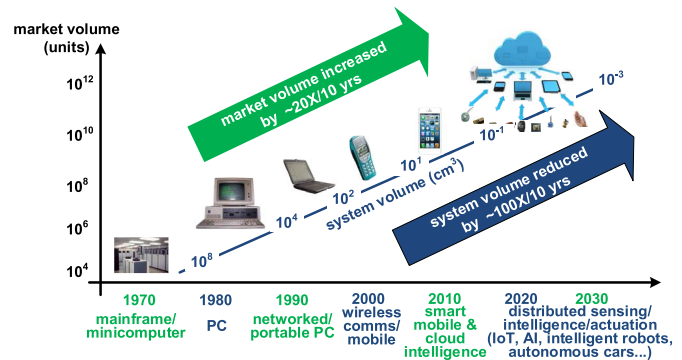


Fig. 1. Exponential trend in market volume (units) and spatial volume of each unit (cm^3) for different technological waves since 1970s [1].

users in the 1980s. Portability and networking have driven the semiconductor market in the 1990s. Wireless communications and mobile platforms have triggered another wave in 2000s, which has culminated in the unprecedented development of cloud intelligence in the 2010s, and the synergistic diffusion of smartphones as clients. Cloud intelligence and its ubiquitous accessibility have enabled beyond-human capabilities in terms of both scale and quality. Cloud intelligence has indeed outperformed human abilities in several fields, such as speech recognition [8], image recognition [9], gaming [10], certain types of medical diagnosis [11], and, even, machine learning model development [12], among others. However, these cloud capabilities are not available to the standalone devices when connectivity or wireless communication bandwidth is limited or when the power consumption associated with the wireless data transfer to the cloud cannot be afforded by the device.

The impact of the above-mentioned technological changes is well depicted by the significant shift in the list of top-10 U.S. companies by market capitalization in the last decade. This list now favors the companies that are delivering services based on the cloud intelligence rather than mere goods and reaching users at a ten-figure scale [13].

II. TECHNOLOGY TRENDS AND THE ROLE OF OUR TVLSI COMMUNITY: A GLANCE INTO THE NEXT DECADE

A. Technology Trends

The decade ahead is likely to drive architectural decentralization and redistribution of cloud intelligence in all respects, both in the physical world and in the cyber world [1] (see Fig. 4). Decentralization and redistribution entail the enablement of autonomous behavior toward the edge, as fueled by local sensing, physical data sensemaking, decision making, actuation, communication/interaction, security/trustworthiness,

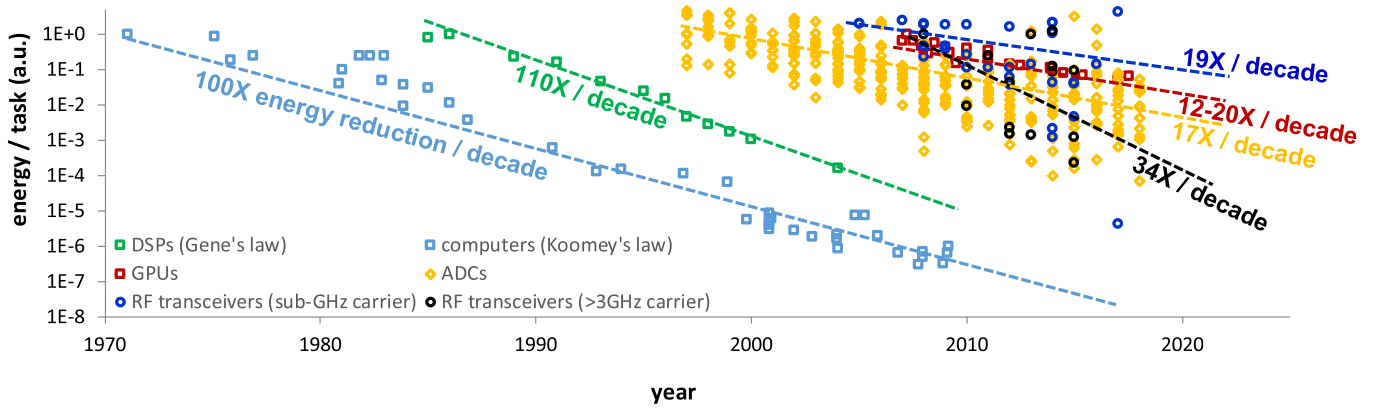


Fig. 2. Exponential trend in the energy reduction per task for various systems and subsystems [4] (energy/instruction in computers, energy/sample in digital signal processors, energy/FLOP in GPUs, energy/conversion in analog–digital converters, and energy/bit in the RF transceivers).

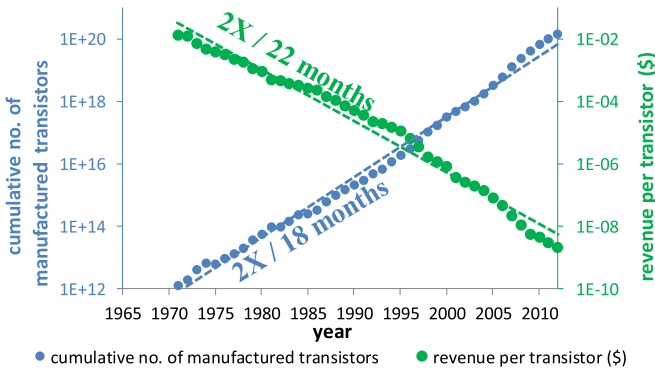


Fig. 3. Exponentially decreasing trend in the cost/transistor, thanks to the exponential increase in the cumulative number of manufactured transistors and 55% learning rate throughout the whole semiconductor industry [1].

- 5) making intelligent and assistive robots part of our daily life;
- 6) incorporating on-chip machine intelligence and learning;
- 7) integrating intelligent and proactive biomedical devices;
- 8) sharing goods and services more responsibly, fairly and efficiently (sharing economy), and progressively decoupling socioeconomic progress from the intensive use of resources, and many others.

From a timescale viewpoint, such intelligence along with its physical root is expected to be directed toward the nearly immediate response to events or queries (i.e., low latency in a broad sense, not confined to communications [14]). In addition, this will progress toward more predictive, proactive, and personalized frameworks, where the demand for services, goods, or physical actuation is driven by the context, rather than being explicitly requested by the individual user. In other words, devices and services will “avoid pushing buttons,” and will instead provide answers and take actions based on the expected demand, rather than waiting for explicit request. This will call for tremendous progress in natural human–technology interaction and allow further shrinkage of systems whose form factor is currently limited by the user interface (e.g., wearables). Such a level of technology proactivity will require constant user context awareness, as enabled by the distributed sensing and its convergence with more traditional human interaction in the cyber world (e.g., social media and web recommendations).

The above-mentioned trends are expected to drive an even stronger demand for more advanced cloud intelligence at an even more abstract level of semantic understanding of data and users. In the end, the cloud will play an even stronger role than in the past in stitching data into a cohesive “big picture” for larger-scale data understanding, knowledge creation, taking appropriate, and immediate actions in the physical world.

In summary, applications will impel a more distributed nature of intelligence, sensing, actuation, communication, and security, along with unprecedented responsiveness and prediction abilities at all scales (i.e., from energy-frugal to energy-intensive integrated systems). Thanks to their key role in the enablement of the above-mentioned capabilities, VLSI systems have a bright future ahead.

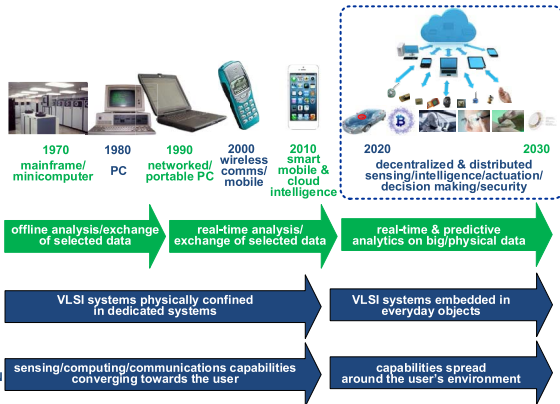


Fig. 4. General technological trends and evolution of capabilities of the VLSI systems.

and more heterogeneous integration. As few examples, such process of decentralizing and redistributing capabilities will be instrumental in the following:

- 1) making the Internet of Things a reality at scale;
- 2) managing transactions with distributed ledgers (e.g., blockchain, not limited to cryptocurrency);
- 3) making cars truly autonomous, connected, and collaborative;
- 4) enhancing the human body with new capabilities with augmented senses and powers (e.g., wearable augmented reality, multiscale vision with the ability to zoomed-in view, or abstract elements in complex scenes);

B. Role of Our TVLSI Community

Enabling the above-mentioned new capabilities will clearly demand for further fundamental advances in VLSI systems, at a larger scale than in the past. VLSI systems will be pushed toward an unprecedented range of performance, energy efficiency, form factor, cost, and scale. Such advances will be needed to continue (and possibly accelerate) the historical scaling trends in Section I. Due to the limited energy and performance gains offered by technology scaling, such advances will need a more coordinated effort at all levels of abstraction, rather than traditionally relying mostly on the device shrinkage.

VLSI systems will be more relevant than ever from an application perspective and pose even harder challenges that make innovation even more important than in the past. This creates obvious opportunities (e.g., room for new exciting ideas and market creation/expansion), challenges (e.g., relentless and cross-disciplinary innovation), and responsibilities (e.g., being highly relevant to global challenges and leading the change). Innovation in the VLSI systems has certainly changed the world in the recent and less recent past and will continue to do so in the foreseeable future.

As a community, we have the power and the responsibility to sustain and strengthen the transformational impact of ideas that translate into faster, more energy efficient, economical, and pervasive VLSI systems. To meet the above-mentioned expectations from our society, a well-coordinated effort of our community is needed more than ever, from materials for semiconductors to modeling and design methodologies, verification, integration/packaging, testing, circuits, architectures, systems, algorithms, and so on. In other words, we are all asked to step out of our comfort zone of our traditional domain of expertise (e.g., level of abstraction) and explore the boundaries and the interactions with other domains.

In view of its systems' nature, TVLSI is a natural venue to share and breed ideas that transcend the traditional boundaries of domains of expertise. Accordingly, TVLSI will need to keep evolving and transforming to serve our community and society at best and contribute to drive this change.

III. OUR TVLSI JOURNAL: TRAJECTORY IN THE YEARS TO COME

Starting my term as Editor-in-Chief of TVLSI in 2019, I feel the responsibility to rethink and reassess the role of our journal. I take the opportunity of this first editorial to share some of the prospective changes and initiatives that will hopefully contribute to make TVLSI stronger, more impactful, and ultimately a change driver.

Quality will be the main driver of all aspects of journal operations, both on the inside and the outside, as will be discussed in the following. Regarding the journal positioning and identity, we will reinforce the unique role of TVLSI at the crossroad of the three different communities (and related IEEE societies) that it engages: the Circuits and Systems Society (CASS), the Computer Society (CS), and

the Solid-State Circuits Society (SSCS). Being TVLSI about systems, it indeed amalgamates the contribution from three different and complementary angles.

- 1) *CASS [15]*: Theory, analysis, design, implementation of circuits, and their application to systems and signal processing, among others.
- 2) *CS [16]*: Computer organization and architectures, software systems and communication protocols, specification/design/verification/testing methods, and aspects related to reliability, security, and testability, among others
- 3) *SSCS [17]*: Circuit techniques and the state-of-the-art silicon demonstrations, systems design, modeling, technology, and testing that relate directly to the integrated design, among others.

TVLSI focuses on the systems and the overlap between the above-mentioned three areas, including across-level innovation at the boundary of circuits, architectures, and systems, including enabling emerging technologies from novel devices to system integration and packaging, as well as design/simulation/verification/testing methodologies. Experimental demonstrations (e.g., ASICs and field-programmable gate arrays) will be definitely encouraged, and simulation validation will be welcomed for approaches when no fabrication process is available or when the proposed ideas can be credibly and solidly demonstrated without resorting to experimental validation. Theoretical work with adequate demonstration will also be highly valued, including modeling aspects (e.g., device–circuit and circuit–architecture cosimulation) and design methodologies (e.g., automated design, with an emphasis on the interaction of multiple levels of abstraction).

To improve the quality of service, the turnaround time of the review process will be further shortened to meet the widely perceived need for more immediate impact, narrowing the gap between traditional journals and electronic preprint repositories. For regular papers, the targeted average turnaround time from submission to decision will be cut down to seven weeks, thanks to the laudable and explicit commitment of the entire Editorial Board that I would like to deeply thank.

Brief papers will be revamped as high-quality publications with innovation that can be described in a concise manner and published with a shorter turnaround time (six-week maximum turnaround time and shorter, on average). This will make briefs a the compelling publication venue in areas that are rapidly developing while maintaining the rigor and the quality of the selection through a full review process, as opposed to the electronic preprint repositories.

As another initiative to make journal issues more cohesive and compelling, their table of contents will be organized by aggregating the papers with similar topics in the same issue, instead of scattering them across different contiguous issues. This aims to fill the existing gap between regular (papers in the same area are scattered across issues, continuous publication) and special issues (papers in the same area are aggregated, publication is sparse in time). This will be achieved at no impact on the publication schedule, as the early

diffusion through IEEE Xplore will maintain the very same timeline.

New services will be delivered to the readers by leveraging the social media to distill the journal contents (e.g., newsletter with recently published papers) in a personalized fashion. This will foster stronger impact and the expansion of the journal in the fast-growing IEEE Regions. Excellence will be recognized and nurtured by Best Associate Editors and Best Reviewers Awards on an annual basis, which will be made official through the TVLSI webpage and newsletters.

The impact of TVLSI will be further enhanced through regularly invited keynote papers from leaders in our community and industry, to take stock of the advances in areas of broad interest, or to introduce new and highly promising areas. Impact will be also pursued through synergy with other journals and the IEEE societies, via joint thematic issues that reach out to multiple communities in areas of common interest across journals and societies.

TVLSI will also actively promote the publication of papers incorporating supplemental materials to progressively go beyond the traditional articles based on the solely textual and graphical form. Supplemental materials will be in the form of graphical abstracts [18], models and algorithms in the form of software code and scripts to improve the reusability and verifiability [19], benchmarks, and data sets for improved result replicability [20] (e.g., training and test data, classification results, design results, and reports), and other multimedia files, such as videos [21] (e.g., demonstration and testing setup description). Supplemental materials are the additional citable assets for the authors, hence increasing the impact and the visibility of the publications. To recognize the effort in the exploration of such media, strong articles with particularly interesting supplemental materials will be acknowledged in the TVLSI website and newsletters.

Further initiatives are on the way, thanks to the valuable contribution of the entire Editorial Board.

ACKNOWLEDGMENT

The above-described initiatives and the new trajectory of TVLSI are made possible by the hard work of many dedicated colleagues in our community. First of all, I would like to thank the members of the TVLSI Steering Committee for their strong support and valuable advice. I also deeply thank each and every member of the Editorial Board for their personal contribution and commitment to the journal. Among them, I would like to thank Prof. M. Stan, Associate Editor-in-Chief, and S. Weber, Editorial Assistant, for their invaluable experience, insight, and dedication to TVLSI.

There is no better opportunity than this editorial to introduce the members of our Editorial Board to our community, as listed in the following. We really look forward to interacting with authors and reviewers to push TVLSI and the field of VLSI systems to new heights.

MASSIMO ALIOTO, *Editor-in-Chief*
 Department of Electrical and
 Computer Engineering
 National University of Singapore
 Singapore 117583
 e-mail: malioto@ieee.org

APPENDIX RELATED WORK

- 1) M. Alioto, Ed., *Enabling the Internet of Things—From Integrated Circuits to Integrated Systems*. Cham, Switzerland: Springer, 2017.
- 2) G. Bell, "Bell's law for rise and death of computer classes," *Commun. ACM*, vol. 51, no. 1, pp. 86–94, Jan. 2008.
- 3) M. Alioto, V. De, and A. Marongiu, "Energy-quality scalable integrated circuits and systems: Continuing energy scaling in the twilight of Moore's law," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 8, no. 4, pp. 653–678, Dec. 2018.
- 4) M. Alioto, V. De, and A. Marongiu, "Guest editorial energy-quality scalable circuits and systems for sensing and computing: From approximate to communication-inspired and learning-based," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 8, no. 3, pp. 361–368, Sep. 2018.
- 5) J. Koomey, S. Berard, M. Sanchez, and H. Wong, "Implications of historical trends in the electrical efficiency of computing," *IEEE Ann. Hist. Comput.*, vol. 33, no. 3, pp. 46–54, Mar. 2011.
- 6) G. E. Moore, "No exponential is forever: But 'forever' can be delayed!" in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2003, pp. 20–23.
- 7) M. Alioto, E. Sanchez-Sinencio, A. Sangiovanni-Vincentelli, "Guest editorial special issue on circuits and systems for the Internet of Things—From sensing to sensemaking," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 9, pp. 2221–2225, Sep. 2017.
- 8) W. Xiong *et al.*, "Achieving human parity in conversational speech recognition," Microsoft Res., Redmond, WA, USA, Tech. Rep. MSR-TR-2016-71, 2017.
- 9) R. C. Johnson. Microsoft, Google beat humans at image recognition—Deep learning algorithms compete at ImageNet challenge. EETimes, Feb. 2015. [Online]. Available: https://www.eetimes.com/document.asp?doc_id=1325712
- 10) Artificial intelligence: Google's AlphaGo beats Go master Lee Se-Dol, *BBC News*, London, U.K., Mar. 2016.
- 11) H. A. Haenssle *et al.*, "Man against machine: Diagnostic performance of a deep learning convolutional neural network for dermoscopic melanoma recognition in comparison to 58 dermatologists," *Ann. Oncol.*, vol. 29, no. 8, pp. 1836–1842, Aug. 2018.
- 12) (May 17, 2017). *Using Machine Learning to Explore Neural Network Architecture*. [Online]. Available: <https://ai.googleblog.com/2017/05/using-machine-learning-to-explore.html>
- 13) *List of Public Corporations by Market Capitalization*. Accessed: Jan. 3, 2019. [Online]. Available: https://en.wikipedia.org/wiki/List_of_public_corporations_by_market_capitalization
- 14) AT&T. *The Dawn of the 5G World—How 5G Technology Will Ultimately Alter the DNA of the Digital Experience*. Accessed: Jan. 3, 2019. [Online]. Available: <https://www.business.att.com/content/dam/atbusiness/reports/5g-for-business-whitepaper.pdf>
- 15) *IEEE Circuits and Systems Society*. Accessed: Jan. 3, 2019. [Online]. Available: <https://iee-cas.org/about-cass>
- 16) *IEEE Computer Society*. Accessed: Jan. 3, 2019. [Online]. Available: <https://www.computer.org/web/about/>
- 17) *IEEE Solid-State Circuits Society*. Accessed: Jan. 3, 2019. [Online]. Available: <https://sscs.ieee.org/about>
- 18) *IEEE Author Center*. Accessed: Jan. 3, 2019. [Online]. Available: <https://ieeauthorcenter.ieee.org/create-your-ieee-article/prepare-supplementary-materials-for-your-article/developing-a-graphical-abstract/>
- 19) *Code Ocean*. Accessed: Jan. 3, 2019. [Online]. Available: <https://codeocean.com/2018/06/28/on-writing-reproducible-and-interactive-papers/code>
- 20) *IEEE DataPort*. Accessed: Jan. 3, 2019. [Online]. Available: <https://iee-dataport.org/submit-dataset>
- 21) *IEEE Preparing Multimedia Materials*. Accessed: Jan. 3, 2019. [Online]. Available: http://ieeauthorcenter.ieee.org/wp-content/uploads/Preparing_multimedia.pdf



Massimo Alioto (M'01–SM'07–F'16) received the Laurea (M.Sc.) degree in electronics engineering and the Ph.D. degree in electrical engineering from the University of Catania, Catania, Italy, in 1997 and 2001, respectively. He held various positions at the University of Siena, EPFL, in 2007, BWRC, University of California at Berkeley, from 2009 to 2011, the University of Michigan at Ann Arbor, from 2011 to 2012, and CRL, Intel Labs, in 2013. He is currently with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore, where he leads the Green IC Group and is the Director of the Integrated Circuits and Embedded Systems Area. He has authored or coauthored 270 publications on journals and conference proceedings. One of them is the second most downloaded TCAS-I paper in 2013. He is the coauthor of three books: *Model and Design of Bipolar and MOS Current-Mode Logic: CML, ECL and SCL Digital Circuits* (Springer, 2005), *Flip-Flop Design in Nanometer CMOS: From High Speed to Low Energy* (Springer, 2015), and *Enabling the Internet of Things: From Integrated Circuits to Integrated Systems* (Springer, 2017). His current

research interests include self-powered wireless integrated systems, near-threshold circuits for green computing, energy-quality scalable integrated systems, data-driven integrated systems, hardware-level security, and emerging technologies, among others.

Prof. Alioto is the Editor in Chief of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (2019–2020), and Deputy Editor in Chief of the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS (2018). In 2009–2010 he was Distinguished Lecturer of the IEEE Circuits and Systems Society, for which he is/was also member of the Board of Governors (2015–2020), and Chair of the “VLSI Systems and Applications” Technical Committee (2010–2012). In the last five years, he has given 50+ invited talks in top conferences, universities and leading semiconductor companies. He served as Guest Editor of several IEEE journal special issues (e.g., TCAS-I, TCAS-II, JETCAS), and Associate Editor of a number of IEEE and ACM journals. He is/was Technical Program Chair (ISCAS 2022, SOCC, ICECS, NEWCAS, VARI, ICM, PRIME) and Track Chair in numerous conferences. Currently, he is also in the IEEE “Digital circuits” ISSCC subcommittee, and the IEEE ASSCC technical program committee.



Magdy S. Abadir received the B.S. degree (honors) in computer science and automatic control from Alexandria University, Alexandria, Egypt, in 1978, the M.S. degree in computer science from the University of Saskatchewan, Saskatoon, SK, Canada, in 1981, and the Ph.D. degree in electrical engineering from the University of Southern California at Los Angeles, Los Angeles, CA, USA, in 1986.

He was the General Manager of the Best IC Labs, Austin, TX, USA. He was an Adjunct Faculty Member with The University of Texas at Austin, Austin, TX, USA. He spent almost 20 years with Freescale/Motorola Austin, TX, USA, in various roles. He was the Director of the Design Automation, Technology Solutions Organization. From 1986 to 1994, he was with the Microelectronics and Computer Technology Corporation, Austin, TX, USA. He is currently on the Board of Directors of Helic Inc., Santa Clara, CA, USA. He also serves as the Vice President of Corporate Marketing. He has published over 300 technical papers in the areas of design for test, test economics, verification, electronic design automation, and data mining. He

holds 12 patents issued plus several that have been filed.

Dr. Abadir was selected as an IEEE Fellow for his contribution of the verification and testing of microprocessors in 2005. Five of his papers received best paper awards: DATE 1998, ASP-DAC 2002, DATE 2003, VLSI-DAT 2011, and ITC 2014. He founded and chaired a series of international workshops on the economics of design, test and manufacturing, microprocessor and SOC test and verification (MTV), and international verification and security (IVSW). He serves on the Editorial Board of the *IEEE Design&Test Magazine* and Springer's *JETTA Journal*.



Tughrul Arslan is currently the Personal Chair of Integrated Electronic Systems with the School of Engineering, University of Edinburgh, Edinburgh, U.K. He is also a member of the Integrated Micro and Nano Systems Institute and leads the Embedded Mobile, Wireless, and wearable Sensor Systems Group, University of Edinburgh. He has supervised over 40 successful Ph.D. research theses. He is the author of over 500 refereed research papers and the inventor of over 20 patents in these areas. He has led a number of successful projects in the design of low-power embedded wireless systems. These have resulted in new patented technologies, such as the Reconfigurable Instruction Cell Architecture, highly directional low power MEMS-based antenna systems, and embedded systems for wireless navigation indoors and areas of poor GPS signal visibility. Most of these technologies have been licensed to spinouts that he formed or sold to Tier-1 companies. His current research interests include adaptive circuits and systems, reconfigurable hardware and systems, circuits and systems for mission critical applications, adaptive and reconfigurable computing for high-performance computing, and big

data. His research has targeted numerous applications, such as wireless and wearable devices, indoor and urban navigation, aerospace, healthcare and medical imaging, high-performance computing, and big data.

Dr. Arslan has been a member of the IEEE CAS executive Committee on VLSI Systems and Applications since 1999. He is also a member of the steering and technical committees of a number of international conferences. He is a Co-Founder of the NASA/ESA Conference on Adaptive Hardware and Systems and currently serves as a member of its Steering Committee. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 2005 to 2006 and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2008 to 2009.



Chirn Chye Boon (M'09–SM'10) received B.E. (honors) and Ph.D. degrees in electrical engineering from Nanyang Technological University (NTU), Singapore, in 2000 and 2004, respectively.

He was a Senior Engineer with Advanced RFIC. Since 2005, he has been with NTU, where he is currently an Associate Professor. He specializes in the areas of radio frequency (RF) and mm-wave circuits and systems design for biomedical and communications applications. He has conceptualized, designed, and silicon-verified 80 circuits/chips for biomedical and communication applications. He has published over 120 refereed publications and over 20 invention disclosures in the fields of RF and mm-wave. He is the author of the book: *Design of CMOS RF Integrated Circuits and Systems* (World Scientific Publishing).

Dr. Boon serves as a committee member for various conferences. He was a recipient of the Year-2 Teaching Excellence Award and the Commendation Award for Excellent Teaching Performance from the School of Electrical and Electronic Engineering, NTU. He is also an

Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and the IEEE Electron Devices Letters Golden Reviewer. Since 2010, he has been the Programme Director of the RF and mm-wave research at the S\$50 million Research Centre of Excellence, VIRTUS, NTU. He is also the principal investigator for industry/government research grants of S\$8,646,178.22.



Andreas Burg (S'97–M'05) was born in Munich, Germany, in 1975. He received the Dipl.Ing. degree from the Swiss Federal Institute of Technology (ETH Zurich), Zürich, Switzerland, in 2000, and the Dr.Sc.Techn. degree from the Integrated Systems Laboratory, ETH Zurich, in 2006.

In 1998, he was with Siemens Semiconductors, San Jose, CA, USA. During his Ph.D. studies, he was with the Bell Labs Wireless Research for one year. From 2006 to 2007, he was a Post-doctoral Researcher with the Integrated Systems Laboratory and the Communication Theory Group, ETH Zurich. In 2007, he co-founded Celestrius, an ETH spin-off in the field of MIMO wireless communication, where he was responsible for the ASIC development as the Director for VLSI. In 2009, he joined ETH Zurich as an SNF Assistant Professor and the Head of the Integrated Systems Laboratory, Signal Processing Circuits and Systems Group. Since 2011, he has been a Tenure Track Assistant Professor with the École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, where he is currently leading the Telecommunications

Circuits Laboratory. He was promoted to Associate Professor in 2018.

Dr. Burg is a member of the EURASIP SAT SPCN, the IEEE TC-DISPS, and the CAS-VSATC. In 2000, he received the Willi Studer Award and the ETH Medal for his diploma and his diploma thesis, respectively. He was also received the ETH Medal for his Ph.D. dissertation in 2006. In 2008, he received a four-year grant from the Swiss National Science Foundation (SNF) for an SNF Assistant Professorship. Along with his students, he received the Best Paper Award from the *Journal on Image and Video Processing* (EURASIP) in 2013 and the best demo/paper awards at ACSSC 2007, the International Symposium of Circuit and Systems 2013, and ICECS 2013. He serves on the Editorial Board of the *Microelectronics Journal* (Springer). He has served on the TPC of various conferences on signal processing, communications and VLSI. He was the TPC Co-Chair for VLSI-SoC 2012 and the TCP Co-Chair for ESSCIRC 2016 and SiPS 2017. He is also the General Co-Chair of the International Symposium on Low Power Electronics and Design 2019. Throughout his career, he was involved in the tape-out of more than 35 ASICs. He has served as an Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS in 2013. He is also an Editor of the *Journal of Signal Processing Systems* (Springer) and *Journal of Low Power Electronics and Applications* (MDPI).



Chip-Hong Chang (S'92–M'98–SM'03–F'18) received the B.Eng. (honors) degree from the National University of Singapore, Singapore, in 1989, and the M.Eng. and Ph.D. degrees from Nanyang Technological University (NTU), Singapore, in 1993 and 1998, respectively.

He served as a Technical Consultant in industry, prior to joining the School of Electrical and Electronic Engineering (EEE), NTU, in 1999, where he is currently an Associate Professor. He held joint appointments with NTU as the Deputy Director of the Center for High Performance Embedded Systems from 2000 to 2011, the Program Director of the Center for Integrated Circuits and Systems from 2003 to 2009, and an Assistant Chair of Alumni of the School of EEE from 2008 to 2014. He has coedited four books, published ten book chapters and 97 international journal papers (more than two-third of them are IEEE publications), and around 170 refereed international conference papers (mostly IEEE). His current research interests include hardware security and digital forensic, low-power and fault-tolerant computing, residue number systems, and application-specific digital signal processing.

Dr. Chang was the Editorial Advisory Board Member of the *Open Electrical & Electronic Engineering Journal* from 2007 to 2013, *Journal of Electrical and Computer Engineering* from 2008 to 2014, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 2010 to 2013, *Integration*, and *VLSI Journal* from 2013 to 2015. He is an IET Fellow. He has been serving as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS since 2011, IEEE ACCESS since 2013, *Microelectronics Journal* since 2014, IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS and IEEE TRANSACTIONS ON INFORMATION FORENSICS AND SECURITY since 2016, and *Journal of Hardware and Systems Security* (Springer) since 2016. He has guest edited several special issues and served in the organizing and technical program committee of more than 60 international conferences (mostly IEEE). He is also the IEEE Circuits and Systems Society Distinguished Lecturer (2018–2019).



Meng-Fan Chang (M'05–SM'14–F'19) received the M.S. degree from Pennsylvania State University, State College, PA, USA, and the Ph.D. degree from National Chiao Tung University, Hsinchu, Taiwan.

Before 2006, he was with industry for over ten years. From 1996 to 1997, he designed memory compilers at Mentor Graphics, NJ, USA. From 1997 to 2001, he designed the embedded SRAMs and Flash at the Design Service Division, TSMC, Hsinchu. From 2001 to 2006, he was the Co-Founder and the Director of IPLib Company, Taiwan, where he developed the embedded SRAM and ROM compilers, Flash macros, and flat-cell ROM products. He is currently a Full Professor with National Tsing Hua University, Hsinchu. He is the corresponding author of numerous International Solid-State Circuits Conference (ISSCC), Symposium VLSI Circuits, IEDM, and DAC papers. His current research interests include circuit designs for volatile and nonvolatile memory, ultralow-voltage systems, 3-D memory, circuit–device interactions, spintronics circuits, memristor logics for neuromorphic computing, and computing-in-memory for artificial intelligence.

Dr. Chang has been a Technical Committee Member of the IEEE Circuits and Systems Society (CASS) and the Administrative Committee Member of the IEEE Nanotechnology Council. He was a recipient of several prestigious national-level awards in Taiwan, including the Ta-You Wu Memorial Award in 2011, the Academia Sinica Junior Research Investigators Award in 2012, the Outstanding Electrical Engineering Professor Award in 2017, and the Outstanding Research Award of the Ministry of Science and Technology (MOST), Taiwan in 2018. He also received numerous awards from the Taiwan's National Chip Implementation Center, National Tsing Hua University, MXIC Golden Silicon Awards, and ITRI. He is currently the Chair of the IEEE Taipei Section. He has been serving on the Technical Program Committees for ISSCC, IEDM, DAC, the International Symposium of Circuit and Systems, A-SSCC, VLSI-DAT, and numerous international conferences. He is also an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS. He has been a Distinguished Lecture Speaker of the IEEE CASS and SSCS. He is currently the Chair of the IEEE Taipei Section. He has also been serving as the Program Director of the Micro-Electronics Program, MOST (2018–2020) and the Associate Executive Director of Taiwan's National Program of Intelligent Electronics (NPiE) and the NPiE Bridge Program since 2011.



Yao-Wen Chang (S'94–A'96–M'96–SM'12–F'13) received the B.S. degree from National Taiwan University (NTU), Taipei, Taiwan, in 1988, and the M.S. and Ph.D. degrees from The University of Texas at Austin, Austin, TX, USA, in 1993 and 1996, respectively, all in computer science.

He was a Visiting Professor with Waseda University, Tokyo, Japan, from 2004 to 2011, and a Visiting Scholar with the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2014. He is currently the Dean of the College of Electrical Engineering and Computer Science and a Distinguished Professor with the Department of Electrical Engineering, NTU. He has co-edited one textbook on electronic design automation (EDA) and over 300 ACM/IEEE conference/journal papers in these areas, including highly cited works on physical design, manufacturability, and FPGA. His NTUplace3 placer was the core engine of the popular Digital Custom Placer of SpringSoft, acquired by the #1 EDA vendor, Synopsys, in 2012, for U.S. \$406 million. His NTUplace4 is a champion circuit placer from three top contests, DAC, the

IEEE/ACM International Conference on Computer-Aided Design, and ISPD, and now the core engine of MaxPlacer, the flagship circuit placer of the Maxeda Technology. His current research interests include EDA.

Dr. Chang has served as a TPC member for all major EDA conferences. He received four awards at the 50th DAC in 2013 for the 1st Most Papers in the fifth decade (34 DAC papers in the fifth decade; #1 worldwide), and so on. He is the 1st-place winner of six recent EDA Contests as well as received over 20 top-3 contest awards. He was a recipient of ten Best Paper Awards (2017 DAC BPA and so on) and 24 BPA nominations from top international conferences. He has received many research awards, such as the Distinguished Research Awards (highest honor) from the Ministry of Science and Technology of Taiwan (three times), the IBM Faculty Awards (three times), the TECO Award, and the MXIC Chair Professorship and Distinguished Teaching Award (highest honor for top 1% teachers) from NTU. He has served as the Steering Committee/General/Program Chair for ISPD, the General/Program Chair for the IEEE/ACM International Conference on Computer-Aided Design (ICCAD), and the Program Chair for ASP-DAC and FPT. He has served as the Chair for the EDA Consortium of the Ministry of Education of Taiwan and the Independent Board Director of Genesys Logic, Inc., a technical consultant of MediaTek, Inc., RealTek Semiconductor Corporation, and Faraday Technology, Inc. He has served on the IEEE Council on Electronic Design Automation, ICCAD Executive Committees, and the ASP-DAC Steering Committee. He was an Associate Editor of the IEEE TCAD from 2008 to 2013. He is an Editor of the *IEEE Design & Test*. He is the Co-Founder of Maxeda Technology. He is currently the IEEE Council on Electronic Design Automation President-Elect.

Poki Chen (M'05) was born in Chiayi, Taiwan, in 1963. He received B.S., M.S., and Ph.D. degrees from the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, in 1985, 1987, and 2001, respectively.

From 1998 to 2011, he was a Lecturer, an Assistant Professor, and an Associate Professor with the Department of Electronic Engineering, National Taiwan University of Science and Technology (NTUST), Taipei, where he is currently a Professor with the Department of Electronic and Computer Engineering. He has been the Director of the System-on-Chip Research Center/Business Incubation Center, the Department Chair of Electronic and Computer Engineering, and the Dean of Industry and Academia Collaboration Office, NTUST, since 2010. He serves as the Dean of Applied Sciences College, NTUST. His current research interests include FPGA analog applications, such as smart temperature sensor, digital-to-time and time-to-digital converters, analog/mixed-signal integrated circuits design and layout, and time-domain signal processing circuits.



Dr. Chen is currently the Organizer of the IEEE International Conference on Intelligent Green Building and Smart Grid. He is also an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and IEEE ACCESS.



Pasquale Corsonello was born in Cosenza, Italy, in 1964. He received the master's degree in electronics engineering from the University of Naples Federico II, Naples, Italy, in 1988.

He joined the Institute of Research on Parallel Computers, National Research Council, Naples, where he was involved in the design and modeling of electronic transducers for high precision measurement, receiving a post-graduate two + one year grant. In 1992, he joined the Department of Electronics, Computer Science and Systems, University of Calabria, Rende, Italy, as a Research Associate. In 1997, he was appointed as an Assistant Professor of Electronics with the Department of Electronics Engineering and Applied Mathematics, University of Reggio Calabria, Reggio Calabria, Italy, where he also served as the Director of the Microelectronics Laboratory. In 2001, he was appointed as an Associate Professor of Electronics and the Chair of the Ph.D. Program in Electronics Engineering at the University of Reggio Calabria. In 2004, he was a Visiting Researcher with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY, USA, where he was an

Adjunct Associate Professor from 2005 to 2009. In 2004, he joined the Department of Electronics, Computer Science and Systems (Department of Informatics, Modeling, Electronics and Systems Engineering), University of Calabria, as an Associate Professor of Electronics. His current research interests include low-power CMOS design, VLSI architecture for image and video processing, heterogeneous digital systems, and emerging nanoarchitectures. He has coauthored over 160 technical papers and holds two patents in these fields.

Mr. Corsonello was a recipient of the Best Associate Editor Award for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS in 2016. He serves on technical committees of several VLSI conferences and as a peer reviewer for several VLSI journals. He has served as the Guest Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I. He is the Editor-in-Chief of the *Journal of Low Power Electronics and Applications*.



Paolo Crovetto (S'00–M'04) was born in Turin, Italy, in 1976. He received the Laurea (*summa cum laude*) and Ph.D. degrees in electronics engineering from the Politecnico di Torino, Turin, in 2000 and 2003, respectively.

He is currently an Associate Professor with the Department of Electronics and Telecommunications, Politecnico di Torino. He is/has been a (co)supervisor of several M.S./Ph.D. students and postdoctoral graduates, including a Marie Curie Fellow. He is the coauthor of more than 50 papers appearing in top journals and international conference proceedings (one of which was awarded the Excellent Paper Award of the EMC Kyoto 2009 symposium). He holds one patent. His current research interests include the fields of analog, mixed-signal and power integrated circuits, nonlinear circuits, and electromagnetic compatibility at the integrated circuit and system level. His current research activities are focused on nonconventional information processing aimed at the implementation of analog functions by digital techniques and the design of ultralow-power VLSI circuits for the Internet-of-Things and machine learning applications.

Dr. Crovetto is serving as a Regular Reviewer for several international journals, including the IEEE TCAS-I, TCAS-II, TPEL, TMTT, TEMC, and *Electronics Letters* (IET), and for several international conferences. In 2015, he has joined the Editorial Board of *Electronics Letters* (IET) first as an Associate Editor and, then, in 2016, as a Subject Editor in the area of circuits and systems.



Shiro Doshō (M'89) was born in Toyama, Japan, in 1964. He received the M.S. and D.S. degrees from the Tokyo Institute of Technology, Yokohama, Japan, in 1989 and 2005, respectively.

In 1989, he joined the Semiconductor Research Center, Matsushita Electric Industrial Co., Ltd., Osaka, Japan, where he developed the high-performance circuit cores for mixed-signal LSI for multimedia and communication systems, such as CMOS filters, PLLs, oscillators, and ADCs. In 2015, he moved to the Tokyo Institute of Technology as a Professor for developing a high-performance sensor system. He is currently a Specially Appointed Professor with the Institute of Innovative Research, Tokyo institute of technology, and an Analog Expert with Synkom, Co., Ltd. In his 26 years of work at Matsushita (Panasonic), he got 27 U.S. Patents and 65 Japanese Patents in his research work.

Dr. Doshō was a member of the Program Committee at the IEEE VLSI Circuit Symposium from 2009 to 2015. Since 2015, he has been a member of the Program Committee at the Asian Solid-State Circuits Conference. He received the IEEE Transactions on VLSI Systems

Circuits and Systems Society Best Reviewer Award in 2016. He was the Guest Editor-in-Chief for special issues on analog LSI technology of the *IEICE Transactions on Electronics* in 2011.



Rolf Drechsler (F'15) received the Diploma and Dr.Phil.Nat. degrees in computer science from the J. W. Goethe University Frankfurt am Main, Frankfurt am Main, Germany, in 1992 and 1995, respectively.

He was with the Institute of Computer Science, Albert Ludwigs University of Freiburg, Freiburg im Breisgau, Germany, from 1995 to 2000, and the Corporate Technology Department, Siemens AG, Munich, Germany, from 2000 to 2001. Since 2001, he has been with the University of Bremen, Bremen, Germany, where he is currently a Full Professor and the Head of the Group for Computer Architecture, Institute of Computer Science. In 2011, he became the Director of the Cyber-Physical Systems Group, German Research Center for Artificial Intelligence (DFKI), Bremen. His current research interests include the development and design of data structures and algorithms, with a focus on circuit and system design.

Dr. Drechsler was a member of the Program Committees of numerous conferences, including DAC, the IEEE/ACM International Conference on Computer-Aided Design (ICCAD), DATE, ASP-DAC, the Forum on specification & Design Languages (FDL), MEMOCODE, and FMCAD. He received best paper awards at the Haifa Verification Conference in 2006, the FDL in 2007 and 2010, the IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems in 2010, and the ICCAD in 2013 and 2018. He was the Symposium Chair at ISMVL 1999 and 2014 and the Topic Chair for Formal Verification at DATE 2004, DATE 2005, DAC 2010, and DAC 2011. He is an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, *IET Cyber-Physical Systems: Theory & Applications*, *International Journal on Multiple-Valued Logic and Soft Computing*, and *ACM Journal on Emerging Technologies in Computing Systems*. He is a co-founder of the Graduate School of Embedded Systems and the coordinator of the Graduate School System Design funded within the German Excellence Initiative.



Ibrahim (Abe) M. Elfadel (M'88–SM'02) received the Ph.D. degree from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 1993.

From 1996 to 2010, he was with the Corporate CAD Organizations at IBM Research and the IBM Systems and Technology Group, Yorktown Heights, NY, USA, where he was involved in the research, development, and deployment of CAD tools and methodologies for IBM's high-end microprocessors. From 2012 to 2015, he was the Founding Co-Director of Mubadala's TwinLab 3DSC, Abu Dhabi, United Arab Emirates, a joint research center on 3-D integrated circuits with the Technical University of Dresden, Dresden, Germany. He also headed the Masdar Institute Center for Microsystems (iMicro), Abu Dhabi, from 2013 to 2016. From 2013 to 2018, he was the Founding Co-Director of the Abu Dhabi Center of Excellence on Energy-Efficient Electronic Systems, Abu Dhabi. He is currently a Professor of Electrical and Computer Engineering with Khalifa University, Abu Dhabi. Since 2014, he has been the Program Manager of TwinLab MEMS, a joint collaboration with GLOBALFOUNDRIES and

the Singapore Institute of Microelectronics on Micro-Electromechanical Systems. He is the inventor or co-inventor of 50 issued U.S. patents, with several more pending. He is the co-editor of two Springer books: *3D Stacked Chips: From Emerging Processes to Heterogeneous Systems* (2016) and *The IoT Physical Layer: Design and Implementation* (2019). His current research interests include platform prototyping for the Internet-of-Things (IoT), energy-efficient edge and cloud computing, IoT communications, low-power, embedded digital-signal processing, 3-D integration, and CAD for VLSI, MEMS, and silicon photonics.

Dr. Elfadel was a recipient of six Invention Achievement Awards, one Outstanding Technical Achievement Award, and one Research Division Award, all from IBM, for his contributions in the area of VLSI CAD. In 2014, he was a co-recipient of the D. O. Pederson Best Paper Award from the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS. He received (with Prof. M. Ismail) the SRC Board of Director Special Award for pioneering semiconductor research in Abu Dhabi. He was the General Co-chair of the 2017 IFIP/IEEE 25th International Conference on Very Large Scale Integration, Abu Dhabi, United Arab Emirates. He has served on the Technical Program Committees of several leading conferences, including DAC, ICCAD, ASPDAC, DATE, ICCD, ICECS, and MWSCAS. He was an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS from 2009 to 2013. He is currently serving as an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and on the Editorial Board of the *Microelectronics Journal* (Elsevier).



Ruonan Han (S'10–M'14) received the B.Sc. degree in microelectronics from Fudan University, Shanghai, China, in 2007, the M.Sc. degree in electrical engineering from the University of Florida, Gainesville, FL, USA, in 2009, and the Ph.D. degree in electrical and computer engineering from Cornell University, Ithaca, NY, USA, in 2014.

In 2012, he was an Intern with Rambus, Inc., Sunnyvale, CA, USA. He is currently an Associate Professor with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology (MIT), Cambridge, MA, USA. His current research interests include microelectronic circuits and systems operating at millimeter-wave and terahertz frequencies.

Dr. Han is a member of the IEEE Solid-State Circuits Society and the IEEE Microwave Theory and Techniques Society. He was a recipient of the Cornell ECE Director's Ph.D. Thesis Research Award, the Cornell ECE Innovation Award, and two Best Student Paper Awards of the IEEE Radio-Frequency Integrated Circuits Symposium in 2012 and 2017. He received the IEEE Microwave Theory and Technique Society Graduate Fellowship Award and the IEEE Solid-State Circuits Society Predoctoral Achievement Award. He held MIT E. E. Landsman (1958) Career Development Chair Professorship and received the National Science Foundation CAREER Award in 2017. He is also an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and the Guest Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He serves on the Technical Program Committee of the IEEE RFIC Symposium, the IEEE International Microwave Symposium (IMS), and the Steering Committee of IMS in 2019.



Masanori Hashimoto (S'00–A'01–M'03–SM'11) received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1997, 1999, and 2001, respectively.

Since 2016, he has been a Professor with the Department of Information Systems Engineering, Osaka University, Osaka, Japan. His current research interests include computer-aided design for digital integrated circuits, especially design for manufacturability and reliability, timing and power integrity analysis, and low-power circuit design.

Dr. Hashimoto is currently a member of the ACM, the Institute of Electronics, Information, and Communication Engineers (IEICE), and the Information Processing Society of Japan (IPJSJ). He was a recipient of the Best Paper Awards at ASP-DAC 2004 and RADECS 2017 and the Best Paper Award of the IEICE Transactions in 2016. He was on the Technical Program Committees of international conferences, including DAC, ICCAD, ASP-DAC, DATE, ISPD, and ITC, and the Symposium on VLSI Circuits. He has served/serves as an Associate Editor

for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, *ACM Transactions on Design Automation of Electronic Systems*, *Microelectronics Reliability* (Elsevier), and *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences* and an Associate Editor-in-Chief of the *IPJSJ Transactions on System LSI Design Methodology*.



Chun-Huat Heng (S'96–M'04–SM'13) received the B.Eng. and M.Eng. degrees from the National University of Singapore, Singapore, in 1996 and 1999, respectively, and the Ph.D. degree from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 2003.

From 2001 to 2004, he was with Wireless Interface Technologies, which was later acquired by Chrontel. Since 2004, he has been with the National University of Singapore, where he is currently an Associate Professor. He has been working on the CMOS integrated circuits involving synthesizer, delay-locked loop, and transceiver circuits.

Dr. Heng has served as a Technical Program Committee Member for the International Solid-State Circuits Conference and the Asian Solid-State Circuits Conference. He received the NUS Annual Teaching Excellence Award in 2008, 2011, and 2013. He was in the ATEA Honor Roll in 2014. He also received the 2018 IES Prestigious Engineering Award and the Faculty Innovative Teaching Award in 2009. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II.



Deukhyoun Heo received the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2000.

In 2000, he joined National Semiconductor Corporation, where he was a Senior Design Engineer involved in the development of silicon RFICs for cellular applications. In 2003, he joined the Faculty of the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA, USA, where he is currently the Frank Brands Analog Distinguished Professor of Electrical Engineering. He has authored or coauthored approximately 140 publications, including 66 peer-reviewed journal papers and 74 international conference papers. His current research interests include RF/microwave transceiver design based on CMOS, SiGe BiCMOS, and GaAs technologies for wireless and wireline data communications, batteryless wireless sensors and intelligent power management system for sustainable energy sources, adaptive beam formers for phased-array communications, low-power high data-rate wireless links for biomedical applications, and multilayer module development

for system-in-package solution.

Dr. Heo was a recipient of the 2000 Best Student Paper Award presented at the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS) and the 2009 National Science Foundation CAREER Award. He has served on the Technical Program Committee of the DATE, IEEE MTT-S IMS, and the International Symposium of Circuit and Systems. He has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS from 2007 to 2009 and IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. Since 2018, he has been serving as an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.



Tsung-Yi Ho (SM'12) received the Ph.D. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2005.

He is currently a Professor with the Department of Computer Science of National Tsing Hua University, Hsinchu, Taiwan. His current research interests include design automation and test for microfluidic biochips and neuromorphic computing systems.

Dr. Ho was a recipient of the Invitational Fellowship of the Japan Society for the Promotion of Science, the Humboldt Research Fellowship by the Alexander von Humboldt Foundation, the Hans Fischer Fellowship by the Institute of Advanced Study of the Technische Universität München, and the International Visiting Research Scholarship by the Peter Wall Institute of Advanced Study, The University of British Columbia. He received the Best Paper Awards at the VLSI Test Symposium in 2013 and the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS in 2015. He has served as the Chair of the IEEE Computer Society Tainan Chapter from 2013 to 2015 and the ACM SIGDA Taiwan

Chapter from 2014 to 2015. He has served as a Distinguished Visitor of the IEEE Computer Society from 2013 to 2015 and a Distinguished Lecturer of the IEEE Circuits and Systems Society from 2016 to 2017. He is currently serving as an ACM Distinguished Speaker, an Associate Editor for the *ACM Journal on Emerging Technologies in Computing Systems*, *ACM Transactions on Design Automation of Electronic Systems*, *ACM Transactions on Embedded Computing Systems*, IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, and IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and the Guest Editor of the *IEEE Design & Test of Computers*. He is also serving on the Technical Program Committees of major conferences, including DAC, ICCAD, DATE, ASP-DAC, ISPD, and ICCD.



Houman Homayoun received the B.S. degree in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 2003, the M.S. degree in computer engineering from the University of Victoria, Victoria, BC, Canada, in 2005, and the Ph.D. degree from the Department of Computer Science, University of California at Irvine, Irvine, CA, USA, in 2010.

He spent two years at the University of California at San Diego, La Jolla, CA, USA, as the National Science Foundation Computing Innovation Fellow awarded by the Computing Research Association and the Computing Community Consortium. He is currently an Associate Professor with the Department of Electrical and Computer Engineering, George Mason University (GMU), Fairfax, VA, USA. He also holds a joint appointment at the Department of Computer Science and the Information Science and Technology Department. He is also the Director of the Accelerated, Secure, and Energy-Efficient Computing Laboratory, GMU. His current research interests include computer security, applied machine learning, big data computing, heterogeneous computing, computer architecture, embedded system design, memory design,

DRAM Design, and low-power computing. His research projects of more than \$7.2 million have been funded by the National Science Foundation, the General Motors Company, the National Institute of Standards and Technology, the Defense Advanced Research Projects Agency, and the Air Force Research Laboratory.

Dr. Homayoun has served as a member of the Advisory Committee, the Cybersecurity Research and Technology Commercialization working group in the Commonwealth of Virginia. He has also served as the Technical Program Committee Member for several international conferences, including ISPASS, DAC, DATE, CODES-ISSS, CASES, FCCM, ICCD, the Great Lakes Symposium on VLSI (GLSVLSI), IGSC, the IEEE International Symposium on Quality Electronic Design (ISQED), the International Symposium on Low Power Electronics and Design, DSD, the Hardware Oriented Security and Trust, IPDPS, and CF. He has served as a Conference Organizing Committee Member for GLSVLSI, ISPASS, GLOBECOM, ISQED, and the IEEE Big Data conferences. He was a recipient of the four-year Computer Science Department, University of California at Irvine, Chair Fellowship. He received the Best Paper Award of the GLSVLSI 2016 Conference. He was the Technical Program Co-Chair of the GLSVLSI 2018. He is currently serving as the General Chair for the GLSVLSI 2019 Conference. He also organized several special sessions and tutorials on the topics of big data computing and heterogeneous architectures in DAC, ICCAD, DATE, CASES, and CODES-ISSS conferences. He is currently serving as an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.



Yuh-Shyan Hwang (M'04–SM'14) was born in Taipei, Taiwan, in 1966. He received the Ph.D. degree from the Department of Electrical Engineering, National Taiwan University, Taipei, in 1996.

He was a Lecturer with the Department of Electrical Engineering, Lee-Ming Institute of Technology, Taipei, from 1991 to 1996, and an Associate Professor with the Department of Electrical Engineering, Hwa Hsia University of Technology, Taipei, from 1996 to 2003. In 2003, he joined the Department of Electronic Engineering, National Taipei University of Technology, Taipei, where he was a Full Professor and served as the Department Chair from 2011 to 2017. He is currently a Distinguished Professor and the Dean of the College of Electrical Engineering and Computer Science. He has authored over 100 international SCI journal and conference papers. His current research interests include analog/power/mixed-signal integrated circuit design, VLSI design, current-mode analog signal processing, and integrated circuits for power management.

Dr. Hwang was a Technical Program Committee Member of the VLSI Design/CAD Symposium in Taiwan (2010–2019). He was the General Chairs of the 2017 IEEE International Conference on Consumer Electronics-Taiwan and the 2018 IEEE International Symposium on Next-Generation Electronics. He has been serving on the Editorial Board of *Active and Passive Electronic Components* since 2010, *Journal of Engineering* since 2012, and *Far East Journal of Electronics and Communications* since 2013. He has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2014 to 2015. He has been serving as an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and the IEEE ACCESS since 2013. He has been serving as an Associate Editor and the Subject Editor of the *Electronics Letters* (IET) since 2016. He currently serves as a reviewer for over ten technical journals.



Ajay Joshi (M'98) received the B.Eng. degree in computer engineering from the University of Mumbai, Mumbai, India, in 2001, and the M.S. and Ph.D. degrees from the Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA, in 2003 and 2006, respectively.

He was an Intern with Intel Corporation, Santa Clara, CA, USA, in 2003, a Postdoctoral Researcher with the Massachusetts Institute of Technology, Cambridge, MA, USA, from 2006 to 2009, and a Visiting Researcher with Google Inc., Mountain View, CA, USA, from 2017 to 2018. He is currently an Associate Professor with the Department of Electrical and Computer Engineering, Boston University, Boston, MA, USA. He has published over 70 technical papers in peer-reviewed journals, conferences, and workshops. His current research interests include security, silicon-photonic network architectures, hardware accelerators, and cross-layer optimization.

Dr. Joshi was a recipient of the IEEE Micro Top Picks from Hot Interconnects in 2009, the NSF CAREER Award in 2012, the Boston University ECE Award for Excellence in Teaching in 2014, and the Best Paper Award at the Asia Conference on Computer and Communication Security in 2018. He has served on the Technical Program Committee or External Review Committee of numerous conferences, including the Design Automation Conference, the Design Automation and Test in Europe, the International Symposium on Computer Architecture, the International Symposium on Microarchitecture, the International Symposium on High Performance Computer Architecture, the International Symposium on Networks-on-Chip (NOCS), the Symposium on High Performance Interconnects (HOTI), the IEEE International Symposium on Quality Electronic Design, and VLSI Design.



Rajiv V. Joshi (M'89–SM'94–F'02) received the B.Tech. degree from IIT Bombay, Mumbai, India, the M.S. degree from the Massachusetts Institute of Technology, Cambridge, MA, USA, and the Dr.Eng.Sc. degree from Columbia University, New York, NY, USA.

He is currently a Distinguished Visiting Professor with IIT Roorkee, Roorkee, India. He is also a Research Staff Member and the Key Technical Lead with the T. J. Watson Research Center, IBM. He is also a member of the IBM Academy of Technology. He is also an Industry Liaison for universities as a part of the Semiconductor Research Corporation. His novel interconnects processes and structures for aluminum, tungsten, and copper technologies that are widely used in IBM for various technologies from sub-0.5 μm to 14 nm. He has led successfully predictive failure analytic techniques for yield prediction and also the technology-driven SRAM at the IBM Server Group. He has extensively involved in novel memory designs. He commercialized these techniques. He has authored and coauthored over 200 papers. He holds 60 invention plateaus, 235 U.S. patents, and over 354 international patents. His current research interests

include in-memory computation, CNN/DNN accelerators and quantum computing.

Dr. Joshi is a fellow of the IEEE International Symposium on Quality Electronic Design and the World Technology Network and a Distinguished Alumnus of the IIT Bombay. He received three Outstanding Technical Achievement, three highest Corporate Patent Portfolio Awards for licensing contributions. He was a recipient of the 2013 IEEE CAS Industrial Pioneer award and the 2013 Mehboob Khan Award from Semiconductor Research Corporation. In 2014, he is inducted into the New Jersey Inventor Hall of Fame along with pioneer Nicola Tesla. He also received the Best Editor Award from the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He was a recipient of the 2015 BMM Award. He received the prestigious IEEE Daniel Noble Award for 2018. He has served as the General Chair for IEEE ISLPED. He has served as a Distinguished Lecturer for IEEE CAS and EDS societies. He has served on the Board of Governors for IEEE CAS as an Industrial Liaison. He will and has served on the committees of AICAS 2019, the International Symposium of Circuit and Systems, the International Symposium on Low Power Electronics and Design (ISLPED), the IEEE VLSI design, the IEEE Custom Integrated Circuits Conference, the IEEE International SOI Conference, ISQED, and the Advanced Metallization Program Committees. He serves as an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He initiated IBM CAS EDS Symposium at IBM in 2017 and will continue into 2018 with AI as the focal area. He is in the Industry Liaison Committee of the IEEE CAS Society. He has given over 45 invited/keynote talks and given several seminars.



Tanay Karnik (S'88–M'90–SM'04–F'13) received the Ph.D. in computer engineering from the University of Illinois at Urbana–Champaign, Champaign, IL, USA.

He was the Director of the Intel's University Research Office. In 1995, he joined Intel Corporation, Santa Clara, CA, USA. He is currently a Principal Engineer and the Director of the Heterogeneous Platforms Lab, Intel Labs, Hillsboro, OR, USA. His current research interests include the areas of small form factor systems, 3-D architectures, variation tolerance, power delivery, and architectures for novel devices. He has published over 80 technical papers, has 92 issued, and 35 pending patents in these areas.

Dr. Karnik was a member of the International Solid-State Circuits Conference, DAC, ICCAD, ICICDT, the IEEE International Symposium on VLSI, the International Symposium of Circuit and Systems, 3DIC, and the IEEE International Symposium on Quality Electronic Design (ISQED) program committees and JSSC, TCAD, TVLSI, and TCAS review committees. He is a Senior Advisory Board Member of JETCAS. He is also an ISQED Fellow. He received

the Intel Achievement Award for the pioneering work on integrated power delivery. He was the General Chair of ISQED 2008 and ICICDT 2008, ISQED 2009, ASQED 2010, and the 2014 International Symposium on Low Power Electronics and Design. He has presented several keynotes, invited talks, and tutorials and has served on seven Ph.D. students' committees. He was the Guest Editor for JSSC. He is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.



Chulwoo Kim (S'98–M'02–SM'06) received the B.S. and M.S. degrees in electronics engineering from Korea University, Seoul, South Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 2001.

In 2001, he joined the IBM Microelectronics Division, Austin, TX, USA, where he was involved in cell processor design. Since 2002, he has been with the School of Electrical Engineering, Korea University, where he is currently a Professor. He has coauthored two books: *High-Bandwidth Memory Interface* (Springer, 2013) and *CMOS Digital Integrated Circuits: Analysis and Design* (McGraw Hill, 4th edition, 2014). His current research interests include wireline transceiver, memory, power management, and data converters.

Dr. Kim was a recipient of the Samsung HumanTech Thesis Contest Bronze Award in 1996, the International Symposium on Low Power Electronics and Design Low-Power Design Contest Award in 2001 and 2014, the DAC Student Design Contest Award in 2002, the SRC Inventor

Recognition Awards in 2002, the Young Scientist Award from the Ministry of Science and Technology of Korea in 2003, the Seoktop Award for Excellence in Teaching in 2006 and 2011, the ASP-DAC Best Design Award in 2008, the Special Feature Award in 2014, and the Korea Semiconductor Design Contest: Prime Minister Award in 2016. He has served on the Technical Program Committee of the IEEE International Solid-State Circuits Conference. He is currently on the Editorial Board of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He has served as the Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He was the Distinguished Lecturer of the IEEE Solid-State Circuits Society from 2015 to 2016.



Tae-Hyoung (Tony) Kim (M'06-SM'14) received the B.S. and M.S. degrees in electrical engineering from Korea University, Seoul, South Korea, in 1999 and 2001, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Minnesota, Minneapolis, MN, USA, in 2009.

From 2001 to 2005, he was with Samsung Electronics, where he performed research on the design of high-speed SRAM memories, clock generators, and I/O interface circuits. From 2007 to 2009, he was with the IBM T. J. Watson Research Center and Broadcom Corporation, where he performed research on circuit reliability, low-power SRAM, and battery-backed memory design, respectively. In 2009, he joined Nanyang Technological University, Singapore, where he is currently an Associate Professor. He is the author/coauthor of over 140 journal and conference papers and has 17 U.S. and Korean patents registered. His current research interests include low-power and high-performance digital, mixed-mode, and memory circuit design, ultra low-voltage circuits and systems design, variation and aging tolerant circuits and systems, and circuit

techniques for 3-D ICs.

Dr. Kim has served as a committee member for numerous conferences. He received the Samsung Humantec Thesis Award in 1999, 2001, and 2008, the ETRI Journal Paper of the Year Award in 2005, the AMD/CICC Student Scholarship Award at the 2008 IEEE Custom Integrated Circuits Conference (CICC), the Departmental Research Fellowship from the University of Minnesota in 2008, the DAC/International Solid-State Circuits Conference Student Design Contest Award in 2008, the best paper awards at the 2014 and 2011 ISOC, the Best Demo Award at APCCAS2016, and the Low Power Design Contest Award at the 2016 International Symposium on Low Power Electronics and Design. He was the Chair of the IEEE Solid-State Circuits Society Singapore Chapter from 2015 to 2016. He serves as an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and IEEE ACCESS.



Jaydeep Kulkarni (S'03-M'09-SM'15) received the Ph.D. degree in electrical and computer engineering (ECE) from Purdue University, West Lafayette, IN, USA, in 2009.

From 2009 to 2017, he was a Senior Staff Research Scientist at Intel Labs, Hillsboro, OR, USA. In 2017, he joined The University of Texas at Austin, Austin, TX, USA, as an Assistant Professor of ECE, where he currently holds the AMD Endowed Chair in Computer Engineering. He has filed 33 patents and published two book chapters and 70 papers in peer-reviewed journals and conferences. His current research interests include energy-efficient integrated circuits and design methodologies, emerging nanodevices, and machine learning hardware accelerators.

Dr. Kulkarni received the 2008 Intel Foundation Ph.D. Fellowship Award, the 2010 Purdue School of ECE Outstanding Doctoral Dissertation Award, the 2015 IEEE Transactions on VLSI Systems Best Paper Award, and the 2015 SRC Outstanding Industrial Liaison Award. He has served as the TPC Co-Chair and the General Co-Chair for the 2017 and 2018 International Symposium on Low Power Electronics and Design (ISLPED), respectively. He has participated

in the Technical Program Committees of DAC, ICCAD, the IEEE Custom Integrated Circuits Conference, A-SSCC, ISLPED, the IEEE International Symposium on Quality Electronic Design, DCAS, the International Symposium of Circuit and Systems, and VLSID conferences. He has served as an Industrial Distinguished Lecturer for the IEEE Circuits and Systems Society and as an Industrial Liaison for SRC and the National Science Foundation programs. He is currently serving as an Associate Editor for the IEEE SOLID-STATE CIRCUITS LETTERS and IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.



Volkan Kursun (S'01-M'04-SM'11) received the B.S. degree in electrical and electronics engineering from the Middle East Technical University, Ankara, Turkey, in 1999, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Rochester, Rochester, NY, USA, in 2001 and 2004, respectively.

He is currently a Tenured Associate Professor of Electronic and Computer Engineering with The Hong Kong University of Science and Technology, Hong Kong. He has more than 162 publications and nine issued USA and China patents on novel high-speed and low-power semiconductor devices and integrated circuits for high-performance computing. He is the author of the book *Multi-Voltage CMOS Circuit Design* (John Wiley & Sons Ltd., 2006). His current research interests include the fields of heterogeneous 3-D system-on-chip for neuromorphic engineering, energy-efficient and reliable computing, advanced information storage and processing technologies for the Internet of intelligent things, and portable biomedical electronics.

Dr. Kursun is a member of the technical program and organizing committees of a number of IEEE and ACM conferences. He received the Institute of Electronics Engineers of Korea Systems-on-Chip Design Group Award in 2012. He also received the Best Paper Award—First Place at the IEEE 26th International Conference on Microelectronics in 2014. He has served as the Technical Program Committee Chair of the Asia Symposium on Quality Electronic Design in 2010 and 2011. He has served on the editorial boards of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2005 to 2008, *Journal of Circuits, Systems, and Computers* from 2005 to 2011, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 2007 to 2010, and IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS from 2007 to 2015. He currently serves on the Editorial Board of the *Microelectronics Journal*, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and *Journal of Low Power Electronics and Applications*.



Yoonmyung Lee (S'08–M'12–SM'18) received the B.S. degree in electronic and electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2004, and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2008 and 2012, respectively.

From 2012 to 2015, he was a Research Faculty with the University of Michigan, where he performed research on ultralow-power circuit design for mm-scale sensor platforms. In 2013, he co-founded CubeWorks Inc., a start-up company specialized in the mm-scale sensor platforms. In 2015, he joined Sungkyunkwan University, Suwon, South Korea, as an Assistant Professor. His current research interests include energy-efficient integrated circuits design for low-power high-performance VLSI systems and millimeter-scale wireless sensor systems.

Dr. Lee has been serving as a Technical Program Committee Member for A-SSCC since 2017. He has received numerous awards and scholarships, including the Distinguished Undergraduate Scholarship from the Korea Foundation for Advanced Studies in 2001, the Samsung Scholarship

in 2005, the Best Paper Award at the International Symposium on Low Power Electronics and Design in 2009, the DAC/International Solid-State Circuits Conference Student Design Contest in 2009 and 2011, the Intel Ph.D. Fellowship in 2011, and the Samsung Human Tech Thesis Contest Silver Award in 2012.



Hai (Helen) Li (M'08–SM'16–F'19) received the B.S. and M.S. degrees from Tsinghua University, Beijing, China, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA, in 2004.

She was with Qualcomm Inc., San Diego, CA, USA, Intel Corporation, Santa Clara, CA, USA, Seagate Technology, Bloomington, MN, USA, the Polytechnic Institute of New York University, Brooklyn, NY, USA, and the University of Pittsburgh, Pittsburgh, PA, USA. She is currently the Clare Boothe Luce Associate Professor with the Department of Electrical and Computer Engineering, Duke University, Durham, NC, USA. She has authored or coauthored more than 200 technical papers in peer-reviewed journals and conferences and a book *Nonvolatile Memory Design: Magnetic, Resistive, and Phase Change* (CRC Press, 2011). Her current research interests include neuromorphic architecture for brain-inspired computing systems, machine learning and deep neural network, memory design and architecture, and architecture/circuit/device cross-layer optimization for low power and high performance.

Dr. Li was a technical program committee member of over 30 international conference series. She is a Distinguished Member of ACM. She was a recipient of the NSF Career Award, the DARPA Young Faculty Award, and the TUM-IAS Hans Fisher Fellowship from Germany. She received seven best paper awards and additional seven best paper nominations from international conferences. She was the General Chair or the Technical Program Chair of multiple IEEE/ACM conferences. She is currently a Distinguished Lecturer of the IEEE CAS society and a Distinguished Speaker of ACM. She serves as an Associate Editor for the IEEE TCAD, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, IEEE TCAS-II, IEEE TRANSACTIONS ON MULTI-SCALE COMPUTING SYSTEMS, *ACM Transactions on Embedded Computing Systems*, IEEE CEM, ACM TODAES, and IET CPS.



Huawei Li (M'00–SM'09) received the B.S. degree in computer science from Xiangtan University, Xiangtan, Hunan, China, in 1996, and the M.S. and Ph.D. degrees from the Institute of Computing Technology (ICT), Chinese Academy of Sciences (CAS), Beijing, China, in 1999 and 2001, respectively.

She visited the University of California at Santa Barbara, Santa Barbara, CA, USA, from 2009 to 2010. Since 2008, she has been a Professor with ICT, CAS. She has published over 160 technical papers. She holds 20 Chinese patents. Her current research interests include the testing of VLSI/SOC circuits, design verification, design for reliability, fault tolerance, and approximate computing.

Dr. Li was a recipient of the 2012 National Technology Invention Award of China. She was the Technical Program Co-Chair of the IEEE Asian Test Symposium (ATS) in 2007 and 2018, the General Co-Chair in 2014, and the Technical Program Co-Chair of the IEEE International Test Conference in Asia in 2018. She has served/been serving as the Steering Committee Chair

for IEEE Workshop on RTL and High Level Testing (2014–2016), the Steering Committee Vice Chair of ATS (2017–2019), the Secretary General (2008–2015) and Chair (since 2016) of the China Computer Federation Technical Committee on Fault-Tolerant Computing, and the technical program committees for several IEEE conferences. She has been serving as an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION since 2015. She has been serving on the Editorial Board of the *Journal of Computer-Aided Design and Computer Graphics* (Chinese) since 2011 and *Journal of Computer Research and Development* (Chinese) since 2014.



Prabhat Mishra (M'04–SM'08) received the Ph.D. degree in computer science and engineering from the University of California at Irvine, Irvine, CA, USA, in 2004.

He is currently a Professor with the Department of Computer and Information Science and Engineering (CISE), University of Florida, Gainesville, FL, USA, where he leads the CISE Embedded Systems Lab. He has coauthored seven books, 25 book chapters, and more than 150 research articles in premier international journals and conferences. His current research interests include embedded and cyber-physical systems, hardware security and trust, energy-aware computing, system-on-chip validation, formal verification, and postsilicon debug.

Dr. Mishra's research has been recognized by several awards, including the NSF CAREER Award from the National Science Foundation, the IBM Faculty Award, three Best Paper Awards (CODES+ISSS 2003, VLSID 2011, and the IEEE International Symposium on Quality Electronic Design 2016) as well as six Best Paper Nominations (DAC 2009, VLSID 2009, DATE 2012, NANOARCH 2013, VLSID 2013, and ASPDAC 2017), and the EDAA Outstanding

Dissertation Award from the European Design Automation Association. He currently serves as an Associate Editor for the *ACM Transactions on Design Automation of Electronic Systems*, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and the *Journal of Electronic Testing*. He is currently serving as an ACM Distinguished Speaker. He is also an ACM Distinguished Scientist.



Baker Mohammad (M'04–SM'13) received the B.S. degree from The University of New Mexico, Albuquerque, NM, USA, the M.S. degree from Arizona State University, Tempe, AZ, USA, and the Ph.D. degree from The University of Texas at Austin, Austin, TX, USA, in 2008, all in electrical and computer engineering (ECE).

He was a Senior Staff Engineer/Manager with Qualcomm, Austin, TX, USA, for six years, where he was engaged in designing high-performance and low-power DSP processor used for communication and multimedia application. He was with Intel Corporation, Santa Clara, CA, USA, for ten years, where he was involved in a wide range of microprocessors design from high performance, server chips > 100 W (IA-64), to mobile embedded processor low-power sub-1 W (XScale). He has over 16 years of industrial experience in microprocessor design with an emphasis on memory, low-power circuit, and physical design. He is currently an Associate Professor of ECE and the Director of the System-on-Chip Research Center, Khalifa University, Abu Dhabi, United Arab Emirates. He has authored/coauthored over 100 referred

journals and conference proceedings, three books, 18 U.S. patents, and multiple invited seminars/panelist. He is also the presenter of three conference tutorials, including one tutorial on Energy harvesting and Power management for WSN at the 2015 International Symposium of Circuit and Systems. His current research interests include VLSI, power-efficient computing, high-yield embedded memory, emerging technology, such as memristor, STTRAM, and in-memory computing. He is also engaged in microwatt range computing platform for wearable electronics and WSN focusing on energy harvesting, power management, and power conversion, including efficient dc/dc and ac/dc convertors.

Dr. Mohammad received several awards, including the KUSTAR Staff Excellence Award in Intellectual Property Creation, the IEEE TVLSI Best Paper Award, the 2009 Best Paper Award for Qualcomm Qtech Conference, the Intel Involve in the Community Award for Volunteer and Impact on the Community, the 2016 IEEE MWSCAS Myrill B. Reed Best Paper Award, the Qualcomm Qstar Award for Excellence on Performance and Leadership, and the SRC Techon Best Session Papers in 2016 and 2017. He is an Associate Editor of the *Microelectronics Journal* (Elsevier) and participates in many technical committee at the IEEE conferences and reviews for journals, including the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and IEEE Circuits and Systems.



Mehran Mozaffari Kermani (S'00–M'11–SM'16) received the B.Sc. degree in electrical and computer engineering from the University of Tehran, Tehran, Iran, in 2005, and the M.E.Sc. and Ph.D. degrees from the Department of Electrical and Computer Engineering, University of Western Ontario, London, ON, Canada, in 2007 and 2011, respectively.

He joined Advanced Micro Devices as a Senior ASIC/Layout Designer, where he is integrating sophisticated security/cryptographic capabilities into accelerated processing. In 2012, he joined the Electrical Engineering Department, Princeton University, Princeton, NJ, USA, as an NSERC Postdoctoral Research Fellow. From 2013 to 2017, he was an Assistant Professor with the Rochester Institute of Technology, Rochester, NY, USA. In 2017, he joined the Computer Science and Engineering Department, University of South Florida, Tampa, FL, USA.

Dr. Kermani has been the TPC Member for a number of conferences, including Hardware Oriented Security and Trust (Publications Chair), DAC, DATE, RFIDSec, LightSec, WAIFI, FDTC, and DFT. He was a recipient of the prestigious Natural Sciences and Engineering Research Council of Canada Postdoctoral Research Fellowship in 2011 and the Texas Instruments Faculty Award (Douglas Harvey) in 2014. He was the Lead Guest Editor of the IEEE/ACM TRANSACTIONS ON COMPUTATIONAL BIOLOGY AND BIOINFORMATICS and IEEE TRANSACTIONS ON EMERGING TOPICS IN COMPUTING for special issues on security. He has served as the Guest Editor for the IEEE TRANSACTIONS ON DEPENDABLE AND SECURE COMPUTING for the special issue of Emerging Embedded and Cyber Physical System Security Challenges and Innovations in 2016 and 2017. He is currently serving as an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, *ACM Transactions on Embedded Computing Systems*, and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I.



Makoto Nagata (S'95–M'02–SM'07) received the B.S. and M.S. degrees in physics from Gakushuin University, Tokyo, Japan, in 1991 and 1993, respectively, and the Ph.D. degree in electronics engineering from Hiroshima University, Hiroshima, Japan, in 2001.

He was a Research Associate with Hiroshima University from 1994 to 2002, an Associate Professor with Kobe University, Kobe, Japan, from 2002 to 2009, and then promoted to Full Professor in 2009. He is currently a Professor with the Graduate School of Science, Technology and Innovation, Kobe University. His current research interests include design techniques toward high-performance mixed analog, RF, and digital VLSI systems with particular emphasis on power/signal/substrate integrity and electromagnetic compatibility, testing and diagnosis, advanced packaging, as well as their applications for hardware security and safety.

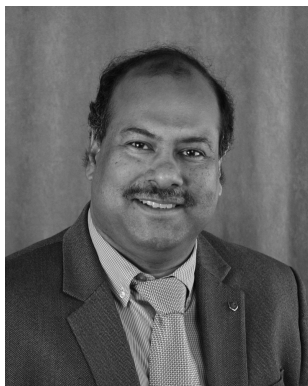
Dr. Nagata is a Senior Member of IEICE. He has been a member of a variety of technical program committees of international conferences, such as the Symposium on VLSI Circuits from 2002 to 2009, the Asian Solid-State Circuits Conference from 2005 to 2009, the Custom Integrated Circuits Conference from 2007 to 2009, the International Solid-State Circuits Conference from 2014 to 2017, and many others. He was a co-recipient of the best paper awards from IEEE 3D-Test 2013, IACR CHES 2014, and IEEE APEMC 2015. He has served as a Technical Program Chair from 2010 to 2011 and the Symposium Chair from 2012 to 2013 for the Symposium on VLSI circuits and the Chapter Chair for the IEEE SSCS Kansai Chapter from 2017 to 2018. He has been the Chair of the Technology Directions subcommittee for International Solid-State Circuits Conference since 2018. He has served as an Associate Editor for the *IEICE Transactions on Electronics* from 2002 to 2005. He is currently an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS since 2015.



Koji Nii (M'99–SM'11) received the B.E. and M.E. degrees from Tokushima University, Tokushima, Japan, in 1988 and 1990, respectively, and the Ph.D. degree in informatics and electronics engineering from Kobe University, Hyogo, Japan, in 2008.

In 1990, he joined Mitsubishi Electric Corporation, Hyōgo, Japan, where he was involved in designing 0.8- μm to 45-nm embedded SRAMs and CAMs for CMOS low-power SoCs and researching on SOI SRAM development. In 2003, he was transferred to Renesas Technology Corporation, Hyōgo, which is a joint company of Mitsubishi Electric Corporation and Hitachi, Ltd., in the semiconductor field. In 2013, he was involved in the research and development of embedded SRAM/TCAM/ROM with assist circuits techniques and/or low-power design techniques in advanced technology nodes (28, 16, and 10 nm, and beyond) with Renesas Electronics Corporation, Tokyo, Japan. In 2018, he joined Floadia Corporation, Tokyo, a SONOS eFlash IP company. He was a Visiting Professor with the Graduate School of Natural Science and Technology, Kanazawa University, Kanazawa, Japan, from 2011 to 2018. His current jobs are Marketing, Sales, and R&D. He holds over 100 U.S. patents, published 50 IEEE/IEICE journals, and over 100 talks at major international conferences.

Dr. Nii was a Technical Program Committee Member of the IEEE CICC from 2010 to 2016 and IEEE IEDM from 2015 to 2016. He received the Best Paper Awards at the IEEE International Conference on Microelectronic Test Structures in 2007 and the IEEE International Symposium on Quality Electronic Design in 2013. He has been an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS since 2015.



Partha Pratim Pande (M'05–SM'11) is currently a Professor, the Boeing Centennial Chair in Computer Engineering, and the Director of the School of Electrical Engineering and Computer Science, Washington State University (WSU), Pullman, WA, USA. His current research interests include novel interconnect architectures for many core chips, on-chip wireless communication networks, and hardware accelerators for big data computing.

Dr. Pande received the NSF CAREER Award in 2009 and the Anjan Bose Outstanding Researcher Award from the College of Engineering, WSU, in 2013. He was the Technical Program Committee Chair of the IEEE/ACM Network-on-Chip Symposium 2015. He serves on the program committee of many reputed international conferences. He currently serves as the Editor-in-Chief (EIC) for the IEEE TRANSACTIONS ON MULTI-SCALE COMPUTING SYSTEMS (TMSCS) and an Associate EIC for the *IEEE Design and Test*. He is on the Editorial Board of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and *ACM Journal on Emerging Technologies in Computing Systems*.



Bipul C. Paul (SM'05) has developed SRAM IPs for customer products in 14- and 7-nm technologies. He was with Toshiba America Research, Alliance Semiconductor, and as a Research Associate at Purdue University, West Lafayette, IN, USA, and developed several nanoscale device and circuit design techniques, including statistical design for yield and reliability, 3-D nanoarchitecture, and ultralow-power design. He was a Visiting Scientist at Stanford University, Stanford, CA, USA, from 2005 to 2010. He is currently with Globalfoundries, where he is responsible for research and development of SRAM and embedded nonvolatile memory in advanced technology nodes. He has published more than 75 technical papers in international journals and conferences, four book chapters, and more than 50 U.S. patents (approved and pending).

Dr. Paul received the Best Thesis Award in 1999 and the IEEE VLSI Transaction Best Paper Award in 2006. He also received the Excellence Award and the Spot Light Award at Globalfoundries in 2012. He is currently on the Editorial Board of the IEEE TRANSACTIONS

ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, *IET Computers and Digital Techniques* (CDT), and *Journal of Low Power Electronics*. He has served on the editorial board of the *ACM Journal on Emerging Technologies in Computing Systems* (JETC) and the Guest Editor for special issues published by IET CDT and ACM JETC in 2009 and 2013, respectively.



Vasilis F. Pavlidis (M'03) received the Diploma and M.Eng. degrees in electrical and computer engineering from the Democritus University of Thrace, Komotini, Greece, in 2000 and 2002, respectively, and the M.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Rochester, Rochester, NY, USA, in 2003 and 2008, respectively.

From 2008 to 2012, he was a Postdoctoral Researcher with the Integrated Systems Laboratory, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland. He is currently a Senior Lecturer (Associate Professor) with the Advanced Processor Technologies Group, School of Computer Science, The University of Manchester, Manchester, U.K. He is the co-creator of the Rochester cube, contributor to the software tool, Manchester Thermal Analyzer, and the leading author of the book *Three-Dimensional Integrated Circuit Design* (1st and 2nd editions). His current research interests include the area of interconnect modeling, 3-D integration, networks on chip, and related design issues in VLSI.

Dr. Pavlidis is a member on the Editorial Boards of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, *Microelectronics Journal*, *Integration*, and *VLSI Journal*. He is also a member of the IEEE Council on Electronic Design Automation, where he serves as the VP Publicity. He also served as a member of the ICT Working Group of the IEEE European Public Policy Initiative in 2017. He has served on several organizing committees and technical program committees of several international conferences, including the International Conference on Computer Design, the International Symposium on Circuits and Systems, and the IEEE Conference on Design, Automation and Test in Europe.



Jose Pineda de Gyvez (F'09) received the Ph.D. degree from the Eindhoven University of Technology, Eindhoven, The Netherlands, in 1991.

He was a Tenured Faculty Member with the Department of Electrical Engineering, Texas A&M University, College Station, TX, USA. He currently holds the position of Fellow at NXP Semiconductors. He also holds the professorship Resilient Nanoelectronics at the Department of Electrical Engineering, Eindhoven University of Technology. He has published numerous papers in the fields of testing, nonlinear circuits, and low-power design. He has coauthored several books. He is also the co-inventor in a number of U.S. granted patents.

Dr. Gyvez has served as an Associate Editor for several IEEE TRANSACTIONS and is continuously involved in the technical program committees of scientific symposia.



Ioannis Savidis (S'03–M'13–SM'18) received the B.S.E. degree in electrical and computer engineering and biomedical engineering from Duke University, Durham, NC, USA, in 2005, and the M.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Rochester, Rochester, NY, USA, in 2007 and 2013, respectively.

In 2013, he joined the Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA, USA, where he is currently an Assistant Professor and directs the Integrated Circuits and Electronics Design and Analysis Laboratory. He has authored or coauthored over 60 technical papers published in peer-reviewed journals and conferences, including a book entitled *Three-Dimensional Integrated Circuit Design* (Morgan Kaufmann, 2nd Edition, 2017). He holds three issued and six pending patents. He has presented several invited talks and tutorials and has served as a panelist on the topic of hardware security at multiple conferences and workshops. His current research interests include analysis, modeling, and design methodologies for high-performance digital and mixed-signal integrated circuits, power management for SoC

and microprocessor circuits, hardware security including digital and analog obfuscation and trojan detection, and electric and thermal modeling and characterization, signal and power integrity, and power and clock delivery for heterogeneous 2-D and 3-D circuits.

Dr. Savidis is a member of the ACM, the IEEE Circuits and Systems Society, the IEEE Communications Society, and the IEEE Electron Devices Society. He is a recipient of the 2018 National Science Foundation Early Faculty (CAREER) Award. He serves on the organizing committees of the IEEE International Symposium on Hardware Oriented Security and Trust (HOST), the International Verification and Security Workshop (IVSW), the International Symposium on Circuits and Systems, and the Great Lakes Symposium on VLSI (GLSVLSI). He is on the Technical Program Committees of international conferences, including HOST, DAC, ICCAD, the International Symposium on Quality Electronic Design, IVSW, ICCD, and GLSVLSI. He serves on the VLSI Systems and Applications Technical Committee of the IEEE Circuits and Systems Society. He also serves on the Editorial Boards of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, *Microelectronics Journal*, and *Journal of Circuits, Systems and Computers*.



Patrick Schaumont received the M.S. degree in computer science from Ghent University, Ghent, Belgium, in 1990, and the Ph.D. degree in electrical engineering from the University of California at Los Angeles (UCLA), Los Angeles, CA, USA, in 2004.

From 1992 to 2000, he was a Staff Researcher with imec, Leuven, Belgium. From 2001 to 2005, he was a Graduate-Level and Postdoctoral Researcher with UCLA. In 2005, he joined Virginia Tech, Blacksburg, VA, USA. From 2012 to 2014, he served as the Director of the Center for Embedded Systems for Critical Applications, Virginia Tech. In 2014, he was a Visiting Researcher with the National Institute of Information and Telecommunications Technology, Koganei, Japan. In 2018, he was a Visiting Researcher with the Laboratoire d'Informatique de Paris 6, Paris, France. He is currently a Professor of Computer Engineering with Virginia Tech. His current research interests include design and design methods of secure, efficient, and real-time embedded computing systems.

Dr. Schaumont was named the Dean's Faculty Fellow by the College of Engineering, Virginia Tech, in 2013. He received the National Science Foundation CAREER Award in 2007. He has served as the Program Co-Chair for several conferences in cryptographic and secure engineering, including CHES, Hardware Oriented Security and Trust, WESS, and RFIDsec.



Fabio Sebastiano (S'09–M'10–SM'17) received the B.Sc. and M.Sc. degrees (*cum laude*) from the University of Pisa, Pisa, Italy, in 2003 and 2005, respectively, the M.Sc. degree (*cum laude*) from the Sant'Anna School of Advanced Studies, Pisa, in 2006, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 2011.

From 2006 to 2013, he was with NXP Semiconductors Research, Eindhoven, The Netherlands, where he conducted research on fully integrated CMOS frequency references, nanometer-CMOS temperature sensors, and area-efficient interfaces for magnetic sensors. In 2013, he joined the Delft University of Technology, where he is currently an Assistant Professor. His research has resulted in ten patents, one book, and over 60 technical publications. His current research interests include cryogenic electronic interfaces, quantum computation, fully integrated frequency references, and electronic interfaces for smart sensors.

Dr. Sebastiano was a co-recipient of the 2008 International Symposium of Circuit and Systems Best Student Paper Award and the 2017 Design Automation and Test in Europe Best IP Award.

He is on the Program Committee of the IEEE RFIC Symposium. He is currently serving as an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He has given invited talks and courses at several international conferences, including the International Solid-State Circuits Conference. He is a Distinguished Lecturer of the IEEE Solid-State Circuit Society.



Anirban Sengupta received the M.A.Sc. and Ph.D. degrees in electrical and computer engineering from Ryerson University, Toronto, ON, Canada.

He is currently an Associate Professor with the Discipline of Computer Science and Engineering, IIT Indore, Indore, India, where he directs the research lab on Behavioural Synthesis of Digital IP Core. He has been an active researcher in the emerging areas of hardware security, IP core protection, and digital rights management for electronics devices. He has around 180 publications and patents. He is the author of a book *IP Core Protection and Hardware-Assisted Security for Consumer Electronics* (IET, 2019).

Dr. Sengupta is an Invited Member of the IEEE CESoc Education and Distinguished Lecturer Nominations Committee. He has been awarded the prestigious IEEE Distinguished Lecturer by the IEEE Consumer Electronics Society in 2017. His research achievements have received wide media coverage as IET International News, U.K., in 2017. He was awarded the Outstanding Associate Editor Award by the IEEE TCVLSI Letter Editorial Board, IEEE Computer Society, in 2017. He is the General/Conference Chair of the 37th IEEE International Symposium on Consumer Electronics (ICCE) 2019, Las Vegas, USA, and the Technical Program Chair of the 15th IEEE International Conference on Information Technology 2016, the 3rd IEEE International Symposium on Nanoelectronic and Information Systems 2017, the 36th IEEE International Conference on Consumer Electronics (ICCE) 2018, Las Vegas, and the 2019 IEEE International Symposium on VLSI, Florida. He has been inducted into the Executive Committee of IEEE Computer Society Technical Committee on VLSI in 2017. His works have been awarded with the IEEE Consumer Electronics Society Best Research Paper Award 2019 at the IEEE CE Society's Flagship Conference—ICCE 2019, the IEEE Computer Society Technical Committee on VLSI—Best Paper Award at the 2017 IEEE International Symposium on Nanoelectronic and Information Systems, and the IETE Best Research Award by IETE Sub-Center in 2018. He was a recipient of the Visvesvaraya Faculty Research Fellow by Digital India Corporation, Ministry of Electronics & IT. More than a dozen of his IEEE publications have appeared in Top 50 Most Popular Articles with few in Top 5 Most Popular Articles from the IEEE Periodicals. His patents have been cited in industry patents of IBM Corporation, Siemens Corporation, Qualcomm, Amazon Technologies, Siemens, Germany, Mathworks, Inc., Ryerson University, and STC University of Mexico, multiple times. His professional works have received wide media coverage nationally and internationally, such as in IET International News (U.K.), The Times of India, Central Chronicle, DBPOST News, The Free Press Journal, and Dainik Bhaskar. He has supervised more than 15 candidates including several graduated Ph.D. candidates all of whom are/were placed in academia and industry. He has successfully commissioned special issues in the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, *IET Computers and Digital Techniques*, IEEE ACCESS, and IEEE CEM. He was a recipient of the Best Research Paper Award 2017 from IIT Indore. He was awarded the highest rating Excellent by the Department of Science & Technology (DST) based on the performance in funded project in 2017. His ideas have been awarded funding from DST, the Council of Scientific and Industrial Research, and the Department of Electronics & IT. He is the Deputy Editor-in-Chief of the *IET Computers & Digital Techniques*. He is currently the Editor-in-Chief of the IEEE VLSI CIRCUITS & SYSTEMS LETTER of the IEEE Computer Society TCVLSI. He is currently the Chairman of the IEEE Computer Society TCVLSI. He currently serves in several editorial positions as a Senior Editor, an Associate Editor, an Editor, and the Guest Editor of several IEEE TRANSACTIONS/journals, IET, and Elsevier journals, including the IEEE TRANSACTIONS ON AEROSPACE AND ELECTRONIC SYSTEMS, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, IEEE TRANSACTIONS ON CONSUMER ELECTRONICS (to join in 2019), IEEE ACCESS, *IET Computer & Digital Techniques*, *IEEE Consumer Electronics*, IEEE CANADIAN JOURNAL OF ELECTRICAL AND COMPUTER ENGINEERING, IEEE VLSI CIRCUITS & SYSTEMS LETTER, and *Microelectronics Journal* (Elsevier). He also serves as the Guest Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and *IET Computers & Digital Techniques*. He is a registered Professional Engineer of Ontario.



Mingoo Seok (S'05–M'11–SM'18) received the B.S. degree (*summa cum laude*) in electrical engineering from Seoul National University, Seoul, South Korea, in 2005, and the M.S. and Ph.D. degrees from the University of Michigan at Ann Arbor, Ann Arbor, MI, USA, in 2007 and 2011, respectively, all in electrical engineering.

He was a Member of the Technical Staff with Texas Instruments Inc., Dallas, TX, USA, in 2011. Since 2012, he has been with Columbia University, New York, NY, USA, where he is currently an Associate Professor of Electrical Engineering. His current research interests include ultralow-power SoC design for emerging embedded systems, machine-learning VLSI architecture and circuits, variation, voltage, aging, thermal-adaptive circuits and architecture, on-chip integrated power circuits, and nonconventional hardware design.

Dr. Seok is the Technical Program Committee Member for several conferences, including the IEEE International Solid-State Circuits Conference (ISSCC) and the IEEE Custom Integrated Circuits Conference (CICC). He received the 1999 Distinguished Undergraduate Scholarship from the Korea Foundation for Advanced Studies, the 2005 Doctoral Fellowship from the Korea Foundation for Advanced Studies, and the 2008 Rackham Pre-Doctoral Fellowship from the University of Michigan. He also received the 2009 AMD/CICC Scholarship Award for picowatt voltage reference work and the 2009 DAC/ISSCC Design Contest for the 35-pW sensor platform design. He also received the 2015 NSF CAREER Award. He has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS from 2013 to 2015. He has been serving as an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS since 2015 and IEEE SOLID-STATE CIRCUITS LETTER since 2017.



Mircea R. Stan (F'14) received the Diploma degree in electronics and communications from Politehnica University of Bucharest, Bucharest, Romania, in 1984, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Massachusetts, Amherst, MA, USA, in 1994 and 1996, respectively.

Since 1996, he has been with the Charles L. Brown Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, VA, USA, where he is currently a Professor. He has over eight years of industrial experience. He was a Visiting Faculty with Intel MRL/CRL, Hillsboro, OR, USA, in 1999 and 2002, the IBM ASIC Division, Essex Junction, VT, USA, in 2000, and the University of California at Berkeley, Berkeley, CA, USA, from 2004 to 2005. At the University of Virginia, he is an Associate Director of the Center for Automata Processing and an Assistant Director of the JUMP Center for Research in Intelligent Storage and Processing-in-Memory and leads the High Performance Low-Power Lab. He is teaching and involved in researching of high-performance low-power VLSI, processing in memory, temperature-aware

circuits and architecture, embedded systems, spintronics, and nanoelectronics.

Dr. Stan is a member of the ACM, Eta Kappa Nu, Phi Kappa Phi, and Sigma Xi. He was a recipient of the NSF CAREER Award in 1997 and the Best Paper Awards at SHAMAN 2002, ISCA 2003, the Great Lakes Symposium on VLSI (GLSVLSI) 2006, the IEEE International Symposium on Quality Electronic Design 2008, and SELSE 2017. He was the Chair of the VLSI Systems and Applications Technical Committee of the IEEE Circuits and Systems Society (CAS) from 2005 to 2007, the General Chair for GLSVLSI 2004 and the 2006 International Symposium on Low Power Electronics and Design, the Technical Program Chair for the 2005 International Symposium on Low Power Electronics and Design, NanoNets 2007, and SoCC 2018, and on technical committees for numerous conferences. He was the Guest Editor of the IEEE COMPUTER SPECIAL ISSUE ON POWER-AWARE COMPUTING in 2003. He was an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS from 2001 to 2003, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 2004 to 2008, and IEEE TRANSACTIONS ON NANOTECHNOLOGY from 2012 to 2014. Since 2014, he has been a Senior Editor of the IEEE TRANSACTIONS ON NANOTECHNOLOGY. He was a Distinguished Lecturer of the IEEE CAS in 2004, 2005, 2012, and 2013 and the Solid-State Circuits Society in 2008 and 2007.



Mark M. Tehranipoor (F'18) is currently the Intel Charles E. Young Preeminence Endowed Chair Professor in Cybersecurity with the University of Florida, Gainesville, FL, USA. He is also serving as the Founding Director of the Florida Institute for Cybersecurity (FICS) Research and Associate Chair for Research in the Electrical and Computer Engineering (ECE) Department. He has published over 400 journal articles and refereed conference papers and has delivered about 200 invited talks and keynote addresses. He has also published 11 books and more than 20 book chapters. His current research interests include hardware security and trust, supply chain security, the Internet-of-Things security, and VLSI design, test, and reliability. Dr. Tehranipoor is a Golden Core Member of the IEEE Computer Society (CS) and a member of ACM and ACM SIGDA. He was a recipient of a dozen best paper awards and nominations, as well as the 2008 IEEE CS Meritorious Service Award, the 2009 NSF CAREER Award, the 2012 IEEE CS Outstanding Contribution, and the 2014 AFOSR MURI Award. He serves on the program committee of more than a dozen leading conferences and workshops. He has also served as

Program Chair for a number of IEEE and ACM sponsored conferences and workshops, including the Hardware-Oriented Security and Trust (HOST), ITC, IVSW, DFT, D3T, DBT, and NATW. He co-founded the IEEE International Symposium on HOST and served as the HOST-2008 and HOST-2009 General Chair. He is currently serving as a Founding Editor-in-Chief for the *Journal of Hardware and Systems Security* and an Associate Editor for the JETTA, JOLPE, IEEE TVLSI, and ACM TODAES.



Aida Todri-Sanial received the B.S. degree in electrical engineering from Bradley University, Peoria, IL, USA, in 2001, the M.S. degree in electrical engineering from Long Beach State University, Long Beach, CA, USA, in 2003 and the Ph.D. degree in electrical and computer engineering from the University of California at Santa Barbara, Santa Barbara, CA, USA, in 2009.

She was an R&D Engineer with the Fermi National Accelerator Laboratory, Batavia, IL, USA. She has also held summer and visiting research positions at Mentor Graphics, NJ, USA, Cadence Design Systems, STMicroelectronics, and the IBM T. J. Watson Research Center. She is currently a Research Scientist with the French National Council of Scientific Research (CNRS), Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier, Montpellier, France. Her current research interests include nanometer-scale issues in high-performance VLSI design with an emphasis on power, thermal, signal integrity, and reliability issues as well as on circuits and systems for emerging technologies.

Dr. Todri-Sanial serves as a Technical Program Committee Member for the IEEE International Symposium on VLSI, NEWCAS, the Great Lakes Symposium on VLSI, the IEEE International Symposium on Quality Electronic Design, EDSSC, and DATE. She was a recipient of the John Bardeen Fellow in Engineering in 2009, the CNRS Prime d'Excellence Scientifique in 2012, the and CNRS Bronze Medal in 2016.



Marian Verhelst received the Ph.D. degree from KU Leuven, Leuven, Belgium, in 2008.

From 2008 to 2011, she was a Research Scientist at the Radio Integration Research Lab, Intel Labs, Hillsboro, OR, USA. She is currently an Associate Professor with the Microelectronics and Sensors Laboratory, Electrical Engineering Department, KU Leuven. She has published over 100 papers in conferences and journals. Her current research interests include embedded machine learning, hardware accelerators, self-adaptive circuits and systems, and low-power sensing and processing for edge devices.

Dr. Verhelst was a member of the ESSCIRC and the International Solid-State Circuits Conference (ISSCC) TPCs and the ISSCC Executive Committee. She was also a member of the Young Academy of Belgium. She is a member of the DATE Conference Executive Committee and the STEM Advisory Committee of the Flemish Government. She currently holds a prestigious ERC Starting Grant from the European Union. She is also an Associate Editor of TCAS-II and JSSC. She is an SSCS Distinguished Lecturer.



Valerio Vignoli (S'92–M'94) received the Laurea degree in electronics engineering and the Ph.D. degree in nondestructive testing from the University of Florence, Italy, in 1989 and 1994, respectively.

He is currently an Associate Professor of Electronics with the Department of Information Engineering and Mathematical Sciences, University of Siena, Siena, Italy. His research activity is documented by more than 180 papers (peer-reviewed journals or international conference papers), three invited book chapters, and five patents. His current research interests include analog and digital electronic design; design, characterization, and modeling of advanced sensors for monitoring physical quantities; development of data acquisition and processing systems.



Xiaoqing Wen (M'89–SM'08–F'12) received the B.E. degree from Tsinghua University, Beijing, China, in 1986, the M.E. degree from Hiroshima University, Hiroshima, Japan, in 1990, and the Ph.D. degree from Osaka University, Osaka, Japan, in 1993.

From 1993 to 1997, he was an Assistant Professor with Akita University, Akita, Japan. From 1995 to 1996, he was a Visiting Researcher with the University of Wisconsin–Madison, Madison, WI, USA. In 1998, he joined SynTest Technologies, Inc., Sunnyvale, CA, USA, where he served as the Chief Technology Officer until 2003. In 2004, he joined Kyushu Institute of Technology, Iizuka, Japan, where he is currently a Professor and the Chair of the Department of Creative Informatics. He holds 43 U.S. Patents and 14 Japanese Patents on VLSI testing. His current research interests include VLSI testing, diagnosis, and testable designs.

Dr. Wen was a recipient of the Institute of Electronics, Information, and Communication Engineers-ISS Best Paper Award in 2008. He is currently the Co-Chair of the Technical Activity Committee on Power-Aware Testing, the Test Technology Technical Council, and the IEEE Computer Society. Since 2012, he has been an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS.

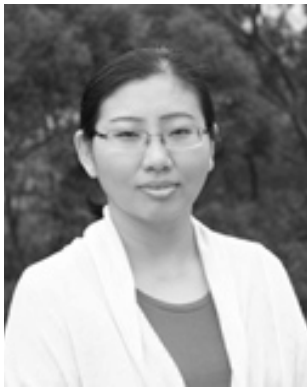


Jiang Xu (S'02–M'07) received the Ph.D. degree from Princeton University, Princeton, NJ, USA, in 2007.

From 2001 to 2002, he was a Research Associate with Bell Labs, NJ, USA, where he discovered the First Generation Dilemma in platform-based SoC design methodologies. From 2003 to 2005, he was a Research Associate with the NEC Laboratories America, NJ, USA, where he was involved in Network-on-Chip (NoC) designs and implementations. From 2005 to 2007, he was with Sandbridge Technologies, NY, USA, a startup company, where he was involved in the development and implementation of two generations of NoC-based ultralow-power multiprocessor system-on-chip for mobile platforms. He established the Big Data System Lab, the Xilinx-HKUST Joint Lab, and the Optical/Photonic Technology for Interconnected Computing System Lab at The Hong Kong University of Science and Technology. He has authored or coauthored more than 110 book chapters and papers in peer-reviewed international journals and conferences. He coauthored a book *Algorithms, Architecture and System-on-Chip*

Design for Wireless Applications (Cambridge University Press). His current research interests include big data system, heterogeneous computing, optical interconnection network, power delivery and management, MPSoC, low-power embedded system, and hardware/software codesign.

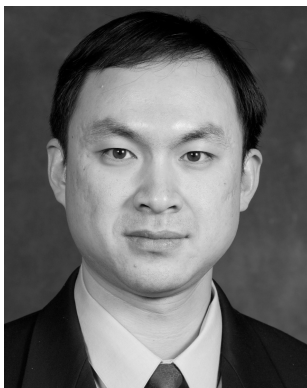
Dr. Xu and his students received the Best Paper Award from IEEE Computer Society Annual Symposium on VLSI in 2009, the Best Poster Award from AMD Technical Forum and Exhibition in 2010, and the Best Paper Award from IEEE Technical Committee on VLSI in 2018. He has served on the steering committees, organizing committees, and technical program committees of many international conferences, including DAC, DATE, ASP-DAC, ICCAD, CASES, ICCD, CODES+ISSS, NOCS, and HiPEAC. He currently serves as an Associate Editor for the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS and IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and the Area Editor for the *ACM Transactions on Embedded Computing Systems* for Hardware and Architecture Design. He was an IEEE Distinguished Lecturer and an ACM Distinguished Speaker.



Wei Zhang received the B.S. and M.S. degrees from the Harbin Institute of Technology, Harbin, China, in 1999 and 2001, respectively, and the Ph.D. degree from Princeton University, Princeton, NJ, USA, in 2009.

From 2010 to 2013, she was an Assistant Professor with the School of Computer Engineering, Nanyang Technological University, Singapore. She is currently an Associate Professor with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, where she established the Reconfigurable System Laboratory. She has authored over 100 technical papers in referred international journals and conferences and three book chapters. Her current research interests include reconfigurable system, power and energy management, embedded system security, and emerging technology.

Dr. Zhang received the Best Paper Award at the 2009 IEEE International Symposium on VLSI and ICCAD 2017. She serves on many organization committees and technical program committees, including DAC, ICCAD, ASPDAC, CASES, FPGA, FCCM, and FPL. She currently serves as an Associate Editor for the *ACM Transactions on Embedded Computing Systems*, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, and *ACM Journal on Emerging Technologies in Computing Systems*.



Zhengya Zhang received the B.A.Sc. degree in computer engineering from the University of Waterloo, Waterloo, ON, Canada, in 2003, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Berkeley (UC Berkeley), Berkeley, CA, USA, in 2005 and 2009, respectively.

Since 2009, he has been with the Faculty of the University of Michigan at Ann Arbor, Ann Arbor, MI, USA, where he is currently an Associate Professor with the Department of Electrical Engineering and Computer Science. His current research interests include low-power and high-performance VLSI circuits and systems for computing, communications, and signal processing.

Dr. Zhang was a recipient of the National Science Foundation CAREER Award in 2011, the Intel Early Career Faculty Award in 2013, the David J. Sakrison Memorial Prize for outstanding doctoral research in electrical engineering and computer sciences from UC Berkeley, and the Best Student Paper Award at the Symposium on VLSI Circuits. He serves on the Program Committees of the Symposium on VLSI Circuits and the IEEE Custom Integrated Circuits

Conference. He was also an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS from 2013 to 2015 and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS from 2014 to 2015. He has been an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS since 2015.



Jun Zhou (M'07–SM'14) received the dual B.S. degree in communication engineering and microelectronics from the University of Electronic Science and Technology of China in 2004, and the Ph.D. degree in microelectronics system design from Newcastle University, Newcastle upon Tyne, U.K., in 2008.

Since 2017, he has been with the School of Information and Communication Engineering, University of Electronic Science and Technology of China, where he is currently a Professor and the Director of the Smart ICs and Systems Research Group. From 2008 to 2011, he was with the Ultra-Low Power Digital Signal Processor Group, IMEC Netherlands, as a Research Scientist, where he was involved in ultra-low power processor design for intelligent sensing applications in collaboration with Philips and NXP. In 2011, he joined the Institute of Microelectronics, Agency for Science, Technology, and Research (A*STAR), Singapore, where he leads projects and supervises Ph.D. students on energy-efficient processor design for intelligent sensing and machine learning applications. He has published papers in prestigious conferences and journals,

including ISSCC, DAC, ESSCIRC, A-SSCC, JSSC, TCAS-I, and TVLSI. His current research interests include energy-efficient processor design for intelligent sensing and machine learning applications.

Prof. Zhou has served as a TPC Member and the Session Chair for several IEEE conferences, including A-SSCC, ICCD, ISCAS, NEWCAS, and EDSSC. He is currently a Committee Member of the IEEE CAS VLSI Systems and Applications Technical Committee.



Mark Zwolinski (M'93–SM'00) received the B.Sc. degree in electronic engineering and the Ph.D. degree in electronics from the University of Southampton, Southampton, U.K., in 1982 and 1986, respectively.

He is currently a Professor with the School of Electronics and Computer Science and the Associate Dean International of the Faculty of Engineering and Physical Sciences, University of Southampton. He has authored two textbooks and coauthored one textbook. He has written over 200 papers in the areas of electronic design automation, test, and reliability and supervised 30 Ph.D. students to completion. His current research interests include reliability, hardware security, and behavioral modeling and simulation.

Dr. Zwolinski is a fellow of IET and BCS and a Senior Member of ACM.



Stacey Weber received the B.A. degree in sociology and the M.S.W. degree in social work from Rutgers University—New Brunswick, New Brunswick, NJ, USA, in 1998 and 2002, respectively.

She is a New Jersey state-certified social worker. Since 2003, she has been on the Staff of Princeton University, Princeton, NJ, USA, as a Grants Administrator/Financial Manager. From 2009 to 2013, she served as a Financial Administrator of the Gigascale Systems Research Center.

Ms. Weber was a recipient of the Donald Griffin '23 Management Award. Since 2007, she has been serving as the Editorial Assistant for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.