Improvement of Active-Input Current Mirrors Using Adaptive Biasing Technique

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***Abstract*—Dynamic CMOS current mirrors are used in a large variety of circuits as fundamental elements of analog design. Several topologies have been proposed over the years to improve their performances. Among these solutions, the active-input technique is intended to increase speed-power ratio and input compliance. However, it has been proven that this structure suffers from a restricted input-current dynamic. In this paper, we propose an enhancement of the active-input structure relying on adaptive biasing to overcome the input current range limitation at low cost in terms of power consumption, noise and silicon area. Theoretical analysis demonstrates the efficiency of the proposed enhancement. Then, an example circuit realized in AMS CMOS $0.18\,\mu\mathrm{m}$ technology at $1.8\,\mathrm{V}$ supply is validated by simulation results.**

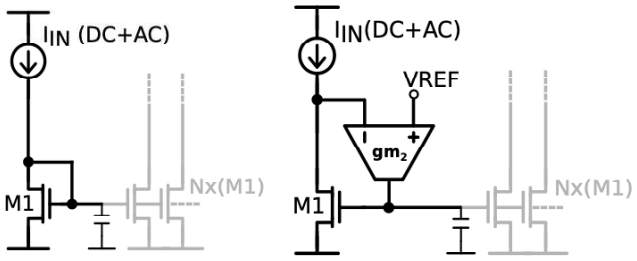
***Keywords*—CMOS analog design, Current mirror, Active-input current mirror, Operational transconductance amplifier, Linear feedback, Adaptive bias, High-current drive**

I. INTRODUCTION

Elementary circuit blocks such as current mirrors must balance power, speed, accuracy and voltage compliance as soon as they have to face dynamic inputs. Typically, current mirrors with large copy ratios, as illustrated Fig. 1a are used to decrease power consumption. Multiple output branches offer large output currents while saving static power. In addition, an increase in transistor sizes limits v_{ds}-induced errors and lowers sensitivity to geometrical mismatch or other process variations. But these design choices necessarily result in speed degradation of the current mirror [1], [2].

The active-input current mirror, first introduced by Serrano *et al.* [3] is shown Fig. 1b. It has been proposed to enhance input compliance and speed-power ratio of dynamic current mirrors for various applications such as biostimulators in [4] or signal processing circuits [5]. The structure is based on a shunt-shunt feedback configuration using Operational Transconductance Amplifiers (OTA) around the current mirror. It has the advantages of a voltage-regulated input and possible bandwidth-improvement operation when compared to equivalent diode-connected current mirrors (Fig. 1a). However, significant changes of the input current level, either to adjust the DC component or for large signal operation, involves variations in performances of transistors composing the current mirror. The consequences are a detuned feedback loop and a degraded frequency behaviour for the system. Therefore, speed performances cannot be maintained across the all input range when signals with large magnitudes are targeted.

In this work, a new feedback structure for the active-input current mirror is proposed. The feedback loop gain, fixed by the OTA gain-bandwidth product, is made dependent on the input current level as depicted in Fig. 3. This ensures that speed performances of the classical active-input topology are preserved over a wider input dynamic range.



(a) Basic diode-connected current mirror

(b) Classic active-input current mirror

Figure 1. Current mirrors used as references

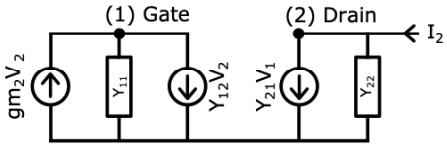


Figure 2. Mid-frequency 2nd order model of a classic active-input current mirror. With adaptive biasing the gain g_{m2} is made dependant of I_2.

II. CALCULATION OF THE INITIAL FEEDBACK LOOP GAIN

In the classical active-input structure Fig. 1b, an OTA replaces the diode connection to realize the feedback between gates and input drain of the current mirror. An input current change is measured by sensing on the OTA negative input, the voltage it generates across the input impedance. Then, according to the designed OTA transconductance, a certain amount of current is injected on the current mirror gate to adjust it voltage and produce the expected output current.

In [6], a dedicated formalism based on a 2nd order generic model is introduced to design active-input current mirrors. It is shown that the OTA transconductance must be carefully defined to achieve the best speed-power ratio without any undesired oscillatory behavior. For a given operating point, one OTA gain value corresponds to one specific damping factor with one specific bandwidth. Because we want to preserve the use of this topology as an elementary current source, possibly implemented in place of classical current mirrors, here we are interested in the critically damped response. The damping factor m is equal to 1, this is the fastest response we can achieve without any pseudo-oscillations.

The generic modelling mentioned above is reused to derive

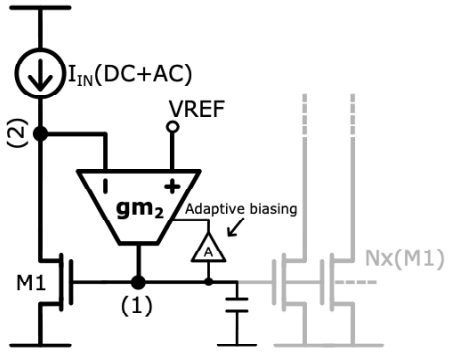


Figure 3. Principle of the adaptive biasing. The current mirror gate is measured, amplified and used to tune accordingly the OTA bias source.

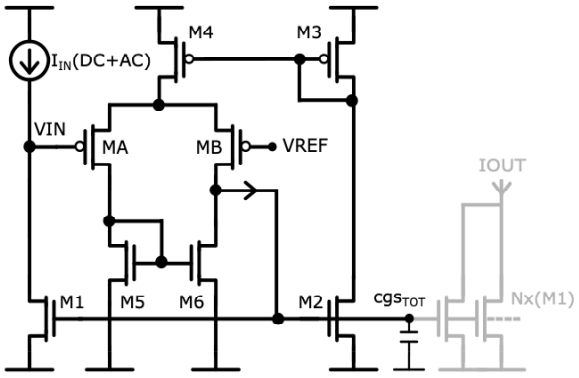


Figure 4. Proposed implementation of active-input current mirror with adaptive biasing

in (2) the OTA gain $g_{m2@m=1}$ leading to a critically damped response and in (3) the related system bandwidth. $BW_{\mathrm{ai@m=1}}$. The corresponding small-signal representation is drawn in Fig. 2. The OTA is considered as an ideal voltage controlled current source and a two-port admittance matrix models the current mirror which expresses as:

$$Y_{CM} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} C_{11}s & -C_{12}s \\ g_{21} - C_{21}s & g_{22} + C_{22}s \end{bmatrix} \quad (1)$$

Components C_{11}, C_{22}, g_{22}, g_{21} model respectively the overall gate-to-ground capacitance, the overall drain-to-ground capacitance, the overall output conductance of the input branch and the input MOS transconductance. The gate-drain capacitance is represented by C_{21} and C_{12} for gate and drain voltage variations.

OTA gain $g_{m2@m=1}$ and system bandwidth. $BW_{\mathrm{ai@m=1}}$ are calculated by studying poles of the transimpendance transfert function $\frac{V_1}{I_2}$ ($\frac{V_{gate}}{I_{in}}$) .

$$g_{m2@m=1} = \frac{(g_{22}C_{11})^2 + (g_{21}C_{12})^2 + 2g_{21}g_{22}C_{11}C_{12}}{2g_{22}C_{11}C_{21} + g_{21}(4C_{11}C_{22} - 2C_{12}C_{21})} \quad (2)$$

$$BW_{\mathrm{ai@m=1}} = \sqrt{\left(\sqrt{2} - 1\right) \frac{g_{21}(g_{m2@m=1})}{C_{11}C_{22} - C_{21}C_{12}}} \quad (3)$$

Eventually, for a given operating point we extract values of current mirror components C_{ij} and g_{ij} and then deduce the optimum OTA gain g_{m2}. If the operating point varies, two cases have to be considered:

- the OTA gain g_{m2} becomes lower than expected, the system is getting slower, and for large differences, the active-input current mirror may show poorer speed-ratio than the equivalent diode-connected current mirror.
- the OTA gain g_{m2} is higher than expected, the system becomes under-damped and the amounts of overshoot and oscillation directly relate to the difference between the actual OTA transconductance and the expected one.

III. Adaptive Biasing Operation

To ensure speed performance of the basic active-input topology over a bigger input current range, we implement an adaptive biasing of the OTA, to link its transconductance to the DC input current level. When M1 device characteristics are changing, the adaptive bias tunes the OTA transconductance to reduce the difference with its expected value. A simple implementation of the active-input structure with adaptive biasing is shown Fig. 4.

As a first approximation, it is known that the output conductance of M1 (g_{22} here) varies proportionally to the input current I_{IN} and the transconductance of M1 (g_{21} here) varies proportionally to the square root of the input current I_{IN}. Thus, using (2) and the previous assumptions, we can prove that the OTA gain should increase to maintain the desired speed when the input current increases. If we define the coefficient α as $I_{IN} = \alpha I_{INmin}$ and assume as an approximation that only g_{22} and g_{21} of the current mirror are varying, then the bandwidth of the active input with adaptive biasing (indices $_{\mathrm{aai}}$) and the basic active input (indices $_{\mathrm{bai}}$) can be expressed according to input current variation.

$$BW_{\mathrm{aai}} = \omega_{\mathrm{ai}min}\sqrt{\alpha\left(\sqrt{(2\alpha-1)^2+1} - (2\alpha-1)\right)} \quad (4)$$

$$\text{with} \quad g_{m2aai} = \sqrt{\alpha} g_{m2min} \quad (5)$$

$$BW_{\mathrm{bai}} = \omega_{\mathrm{ai}min}\sqrt{\sqrt{\alpha}\left(\sqrt{(2\alpha\sqrt{\alpha}-1)^2+1} - (2\alpha\sqrt{\alpha}-1)\right)} \quad (6)$$

Finally, we prove the theoretical efficiency of our proposed enhancement by comparing the evolution of bandwidths in (5) and (6) when α increases. For instance, when $\alpha = 1$ (meaning $I_{IN} = I_{INmin}$) we have $BW_{\mathrm{aai}} = BW_{\mathrm{bai}}$ as expected, the same speed is achieved. But when $\alpha = 5$ then $BW_{\mathrm{aai}} = 2.3BW_{\mathrm{bai}}$, the adaptive active-input shows better speed performance. A graphical example is given in section *Validation Results*. In the proposed implementation, the OTA and its adaptive bias circuit are initially designed from (2) and (3) to achieve the desired frequency behaviour at the minimum input current I_{INmin}.

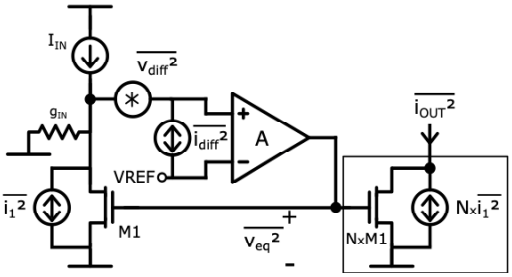


Figure 5. Noise model of the active-input structure

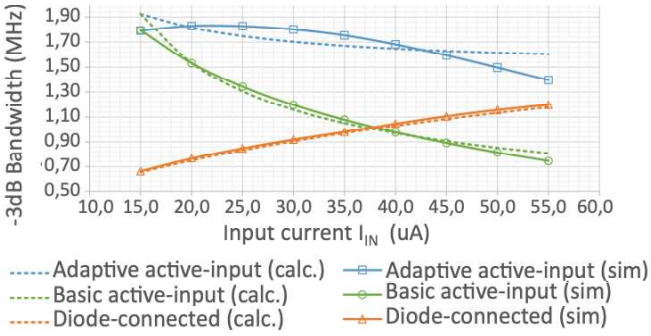


Figure 6. Cut-off frequencies versus input currents for the three compared types of current mirror

We can notice as well, that the relative speed improvement over the input current range, between a basic active-input and an adaptive active-input solution, is independent of the mirror characteristics. And by extension, it is also independent of the MOS sizes or if the current mirror have been turned into a cascode configuration.

IV. Design Considerations and Noise Analysis

In Fig. 4, the adaptive bias circuit (M2, M3) is a common-source amplifier placed between the mirror gates and the gate of the transistor biasing the differential pair of the OTA. The input capacitance of this common-source amplifier has to be negligible compared with the total gate-to-ground capacitance, or taken into account in the parameter C_{11} when calculating the optimum OTA gain value with (2) and (3). Moreover, for large signal variation, we must ensure that the common-source amplifier bandwidth is equal or larger than the overall system bandwidth, needed to guarantee that the OTA gain tuning is fast enough to follow system variations. Relative aspect ratio for transistors M2, M3 and M4 can be derived from the OTA bias current I_{D4} required to perform a transconductance gain of g_{m2min} at I_{INmin}, and from the common-source amplifier bandwidth which needs to be greater than $BW_{\mathrm{ai@m=1}}$. With α defined as $I_{IN} = \alpha I_{INmin}$, V_{eff} of M4, MA and MB are seen proportional to $\sqrt{\alpha}$. High level DC input current might saturate the OTA gain. Hence, To maximize the speed benefits of this structure, these transistors should be designed with large W/L ratio for low V_{eff} at minimum input current I_{INmin}.

In the following analysis, we are interested in the output current noise, when considering both thermal and flicker noise sources. Noise introduced by the adaptive OTA bias circuit (M2 to M4) and has not been included as it is assumed negligible compared with the differential pair noise. Indeed, when referred to the input, this noise appears to be rejected by the common mode path of the OTA. Fig 5 shows the model considered to estimate output noise contributions. The output noise power spectral density $\overline{i_{out}^2}$ can be expressed in relation with the intrinsic noise of the current mirror elementary transistor $\overline{i_1^2}$ and with the noise generated by the differential pair $\overline{v_{diff}^2}$ as in (7). N is the copy ratio of the current mirror.

$$\overline{i_{out}^2} \approx (N^2+N)\overline{i_1^2} + N^2\overline{i_{IN}^2} + (g_{IN}N)^2\overline{v_{diff}^2} \qquad (7)$$

with :

$$\overline{i_1^2} = 4KT\gamma g_{m1} + \frac{K_f g_{m1}^2}{W_1 L_1 C_{ox} f} \qquad (8)$$

$$\overline{v_{diff}^2} = 8KT\gamma\left(\frac{g_{mA}+g_{m5}}{g_{mA}^2}\right) + \frac{2K_f}{C_{ox}f}\left(\frac{1}{W_A L_A} + \frac{g_{m5}^2}{g_{mA}^2 W_5 L_5}\right) \qquad (9)$$

From (7), we denote that the noise of the current mirror itself is not affected by the feedback loop, as it can be proven to be equal to $(N^2+N)\overline{i_1^2} + N^2\overline{i_{IN}^2}$. Also, the feedback circuit contribution to the output current noise has become mainly dependent on the overall input impedance g_{IN}. Which brings a trade-off between speed and output noise. Indeed, equations (2) and (3) demonstrate that an increase of the input impedance results in a reduction of the the maximum speed reachable at given damping factor.

V. Validation Results

In the context of high output current application, we have compared the diode-connected, the basic active-input and the adaptive active-input topologies with identical MOS devices. Current mirrors described in this section have been simulated using the Cadence® Virtuoso® Analog Design Environment, and the AMS $0.18\,\mu\mathrm{m}$ CMOS models, under a $1.8\,\mathrm{V}$ supply voltage. Transistors of the current mirror have a W/L ratio of 0.7, with $L = 10\,\mu\mathrm{m}$. All current mirrors have a copy-ratio of $N = 40$, where the output branch is composed of N transistor equivalent to M1 connected in parallel. The input current ranges form $15\,\mu\mathrm{A}$ to $55\,\mu\mathrm{A}$, Leading to an output current dynamic of $600\,\mu\mathrm{A}$ to $2.2\,\mathrm{mA}$

For the theoretical calculations displayed in Fig.6 (dotted lines), admittance parameters such as C_{11}, g_{21} or g_{22} have been evaluated by simulation with the system biased at minimal input current, and then extrapolated along the input range using assumption introduced in section *Adaptive Biasing Operation*. Table I shows Y-parameters measured at $I_{IN} = 15\,\mu\mathrm{A}$ for the proposed adaptive active-input current mirror. Numerical results give for the initial OTA gain a value of $g_{m2min} = 0.9\,\mu\mathrm{A\,V^{-1}}$. Which has been achieved with an OTA bias current of $0.3\,\mu\mathrm{A}$ and a common-source amplifier bias current of $1\,\mu\mathrm{A}$.

Table I. Simulated admittance parameters at $I_{IN} = 15\,\mu\mathrm{A}$.

g_{21} (μA V^{-1})	C_{11} (pF)	C_{12} (fF)	C_{21} (pF)	C_{22} (fF)	g_{22} (nA V^{-1})
67.1	16.5	16.4	0.15	9.7	445.1

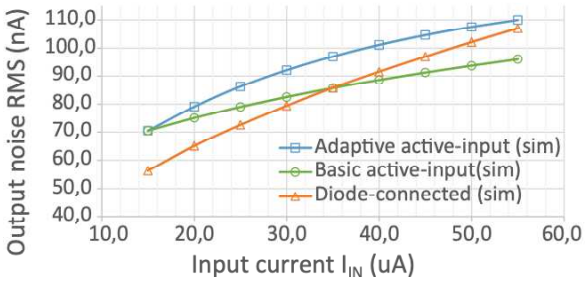


Figure 7. RMS value of output noise versus input currents. PSD integrated from 1 Hz to 20 MHz

Simulated $-3\,\mathrm{dB}$ bandwidth and total RMS output noise for the three compared types of current mirror, shown in Fig 6 and 7, correlates with the theoretical predictions. In our case study example, whereas the basic active-input exhibits a poorer speed than the equivalent diode-connected within the upper half input current range ($35\,\mu\mathrm{A}$ to $55\,\mu\mathrm{A}$), speed of the proposed adaptive active-input speed is kept higher all over the input range at solely the price of two additional MOS devices and an extra bias current. In addition, the proposed solution has negligible impact on noise and differences observed in Fig. 7 essentially relate to differences in system bandwidth values.

VI. Conclusion

This paper presents an enhanced version of the classic active-input current mirror. The efficiency of this solution has been theoretically proven with a generic small signal representation of the system, evaluated across the full input range. Transistor-level simulations on a case example realised with the $1.8\,\mathrm{V}$ AMS $0.18\,\mu\mathrm{m}$ technology confirm the theoretical assertions. The solution, based on an active biasing scheme for the feedback circuit, offers the advantages of the classic topology but ensure its speed performance of the classic active-input structure over a wider input current range. The proposed implementation has negligible noise contribution and minimal impact on power consumption and total area.

References

[1] P. R. Kinget, "Device mismatch and tradeoffs in the design of analog circuits," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 6, pp. 1212–1224, June 2005.

[2] L. N. Alves and R. L. Aguiar, "Frequency behavior of classical current mirrors [CMOS]," in *Electronics, Circuits and Systems, 2002. 9th International Conference on*, vol. 1, 2002, pp. 189–192 vol.1.

[3] T. Serrano and B. Linares-Barranco, "The active-input regulated-cascode current mirror," *IEEE transactions on circuits and systems - Fundamental theory and applications*, vol. 41, no. 6, January-June 1994.

[4] W. Ngamkham, M. N. van Dongen, and W. A. Serdijn, "Biphasic stimulator circuit for a wide range of electrode-tissue impedance dedicated to cochlear implants," in *2012 IEEE International Symposium on Circuits and Systems*, May 2012, pp. 1083–1086.

[5] S. Moazzeni and G. E. R. Cowan, "Application of active current mirrors to improve the speed of analog decoder circuits," *IEEE International Midwest Symposium on Circuits and Systems*, August 2009.

[6] M. Julien, S. Bernard, F. Soulier, V. Kerzérho, and G. Cathébras, "Formal analysis of bandwidth enhancement for high-performance active-input current mirror," in *2017 12th International Conference on Design Technology of Integrated Systems In Nanoscale Era (DTIS)*, April 2017, pp. 1–6.