Electromagnetic Fault Injection: How Faults Occur
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Electromagnetic Fault Injection: how faults occur?

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Introduction

• Context :

• Objectives :
  ➢ Modelling : impact of an EMFI on IC supply voltage
  ➢ SPICE simulation : impact of an EMFI on IC operation
  ➢ Experimental validation
Modelling: Impact of an EMFI on IC supply voltage

Spice Simulation: impact of EMFI on IC operation

Experimental Validation
Modelling: Impact of an EMFI on IC

- EM Induction: hypothesis?

- EMFI induces parasitic currents mostly in the power and ground networks.

- Metal wires from the power/ground networks form many loops.

- Interconnect logic wires don’t form loops.

- EM induction induces currents variation on closed loops.

- Probe IC
Modelling: Impact of an EMFI on IC

- Impact of EMFI on supply voltage.

\[ m_{gnd} = k_{gnd} \sqrt{L_{probe} \times L_{gnd}} \]
\[ m_{vdd} = k_{vdd} \sqrt{L_{probe} \times L_{vdd}} \]

Coupling Probe/Vdd grid  Supply Grid VDD

Coupling Probe/Gnd grid  Supply grid GND
Modelling: Impact of an EMFI on IC

- Impact of EMFI on supply voltage.

\[ m_{vdd} = m_{gnd} \]

**Swing** = \( V_{dd} - Gnd \)

\[ m_{vdd} \neq m_{gnd} \]

Swing is negative for few ns!
Modelling: Impact of an EMFI on IC supply voltage

Spice Simulation: Impact of EMFI on IC operation

Experimental Validation
Modelling: Impact of an EMFI on IC

- Testbench Simulation

\[ Swing = V_{dd} - Gnd \]

![Swing Diagram]

\[ Swing_{width} \]

![Testbench Circuit Diagram]

![Waveform Graphs]
Modelling: Impact of an EMFI on IC

- Logic simulation: Swing amplitude impact on IC operation

Fault criterion $F$:

\[ F = \frac{(\text{CK2Q})_{\text{ref}}}{(\text{CK2Q})_{\text{inj}}} \]

- $F = 1$ Normal Operation
- $0 < F < 1$ Delay
- $F = 0$ Sampling Fault
Modelling: Impact of an EMFI on IC

- Sampling Fault explanation

Normal Operation

Q = ‘1’
Modelling: Impact of an EMFI on IC

- Sampling Fault explanation

\[Q = '0'\]
Modelling: Impact of an EMFI on IC

• Sampling Fault explanation

![Diagram showing the impact of an EMFI on IC with a sampling fault at Q = '0'.]
- Modelling: Impact of an EMFI on IC supply voltage
- Spice Simulation: impact of EMFI on IC operation
- Experimental Validation
EMFI experimental validation

- **Effect of $F_{CLK}$ variations**
  - Target: AES 128bits.
  - EM pulse sweeps, for few periods, with a pulse delay step of 100ps.
  - 50 EMFI shots are performed at each sweep to determine fault probability $P_f$ ($0 < P_f < 1$).
  - As expected Sampling Fault Windows appear with a period equal to that of the IC.
  - Their width are independent of the frequency.

![Diagram of EMFI experimental validation](image)
EMFI experimental validation

- **Effect of $V_{\text{pulse}}$ variations**
  - Determine the evolution of the Sampling Fault Window width in function of $V_{\text{pulse}}$ variations.
  - The width of Sampling Fault Windows increases with $V_{\text{pulse}}$. 

![Graph 1](image1.png)

![Graph 2](image2.png)
**EMFI experimental validation**

- **Effect of PW variations**

  - Determine the evolution of the Sampling Fault Window width in function of PW variations.
  - The Pulse Width does not affect much the sampling fault window.
Conclusion

• Conclusion
 ➢ Modelling simulations show that EMFI induces a voltage **bounces or drops** on **power networks Vdd and GND**. That could induce a **Swing drop**.
 ➢ Sampling Fault occurs when **EM Field** is applied during IC operation around rising CLK edge. In **simulation** and **experimentally**.

• Perspective
 ➢ More accurate **coupling model**.
 ➢ Experimental validation and parallel on **one register** only.
Thank you

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Modelling: Impact of an EMFI on IC

- Logic simulation: Swing amplitude impact on IC operation

Fault criterion $F$:

$$F = \frac{(CK2Q)_{\text{ref}}}{(CK2Q)_{\text{inj}}}$$

$(CK2Q)_{\text{inj}} \geq (CK2Q)_{\text{ref}}$

- $F = 1$ Normal Operation
- $0 < F < 1$ Delay
- $F = 0$ Sampling Fault

![Graph showing normal operation and sampling fault](image_url)
Modelling: Impact of an EMFI on IC

- Sampling Fault explanation
Modelling : Impact of an EMFI on IC

Sampling Fault explanation

V1 is disrupted during the D recovery

If CLK edge occurs during V1 alteration : wrong value is sampled and stored in Master loop.