



Electromagnetic Fault Injection : How Faults Occur

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Fault Diagnosis and
Tolerance in Cryptography



Fault Diagnosis and Tolerance in Cryptography 2019

Electromagnetic Fault Injection : how faults occur ?



Authors : **Mathieu DUMONT** [1,2] , **Philippe MAURINE** [2], **Mathieu LISART** [1]

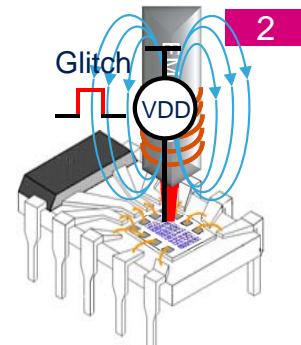
[1] STMicroelectronics, Rousset, France

[2] LIRMM, University of Montpellier, Montpellier, France

Introduction

- Context :

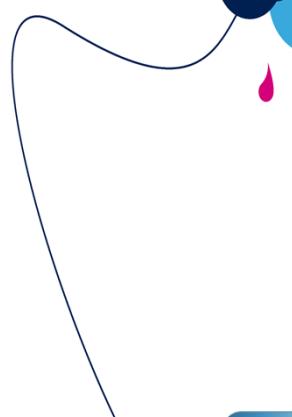
- Attack by Fault injection : Glitch attack, Laser attack, **Electromagnetic Fault injection (EMFI)**.
- EMFI Fault model : Timing Fault (2012) by A.Dehbaoui ; **Sampling fault** (2016) S.Ordas.



- Objectives :

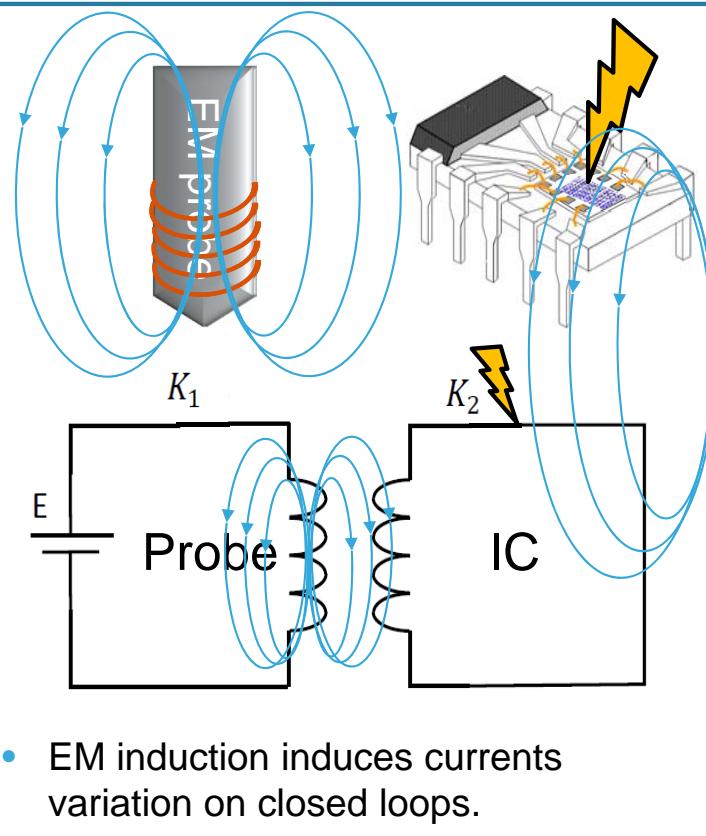
- Modelling : impact of an EMFI on IC supply voltage
- SPICE simulation : impact of an EMFI on IC operation
- Experimental validation

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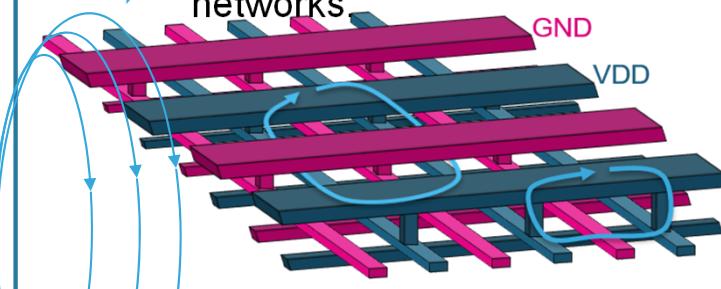


Modelling: Impact of an EMFI on IC

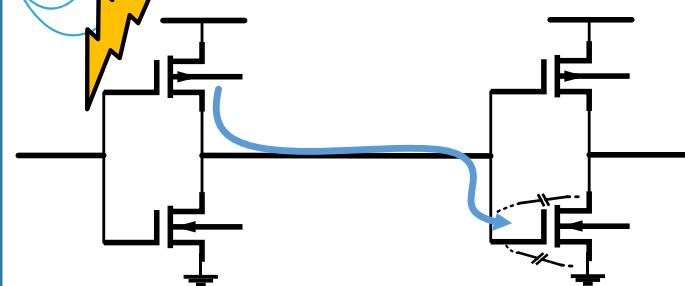
- EM Induction: hypothesis ?



- Metal wires from the power/ground networks form many loops!



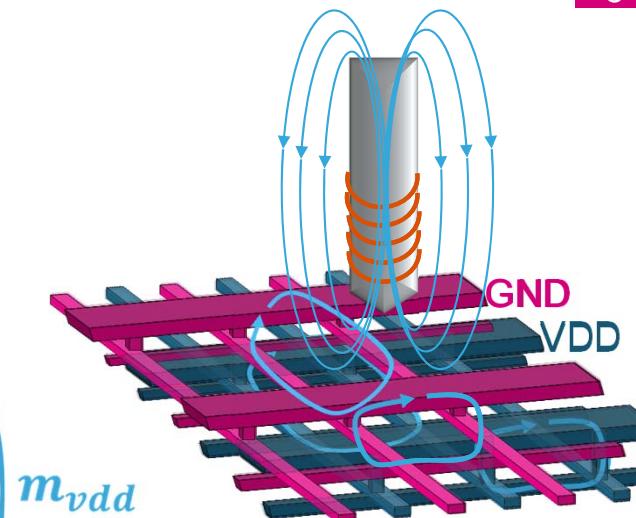
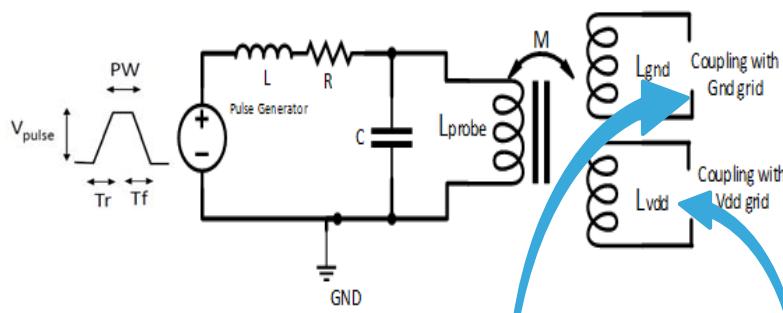
- Interconnect logic wires don't form loops.



Modelling: Impact of an EMFI on IC

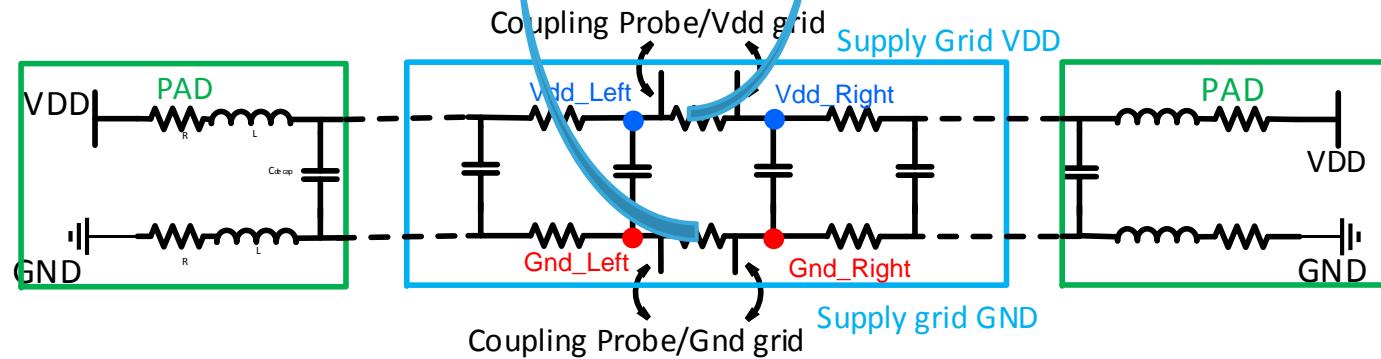
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- Impact of EMFI on supply voltage.



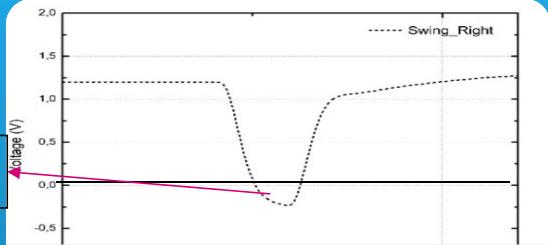
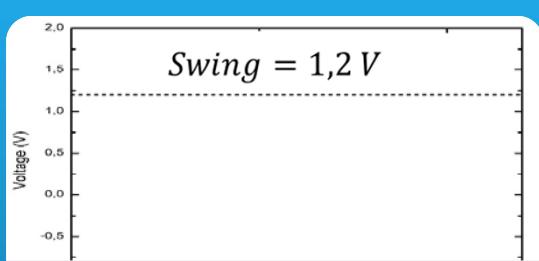
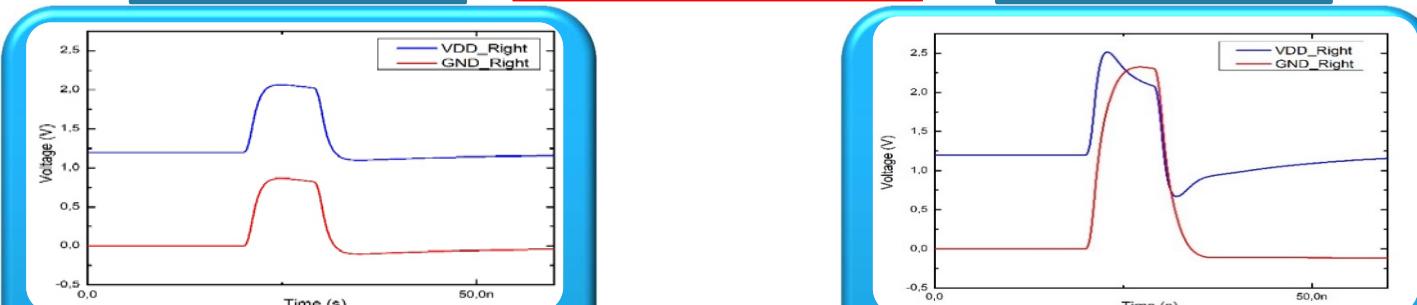
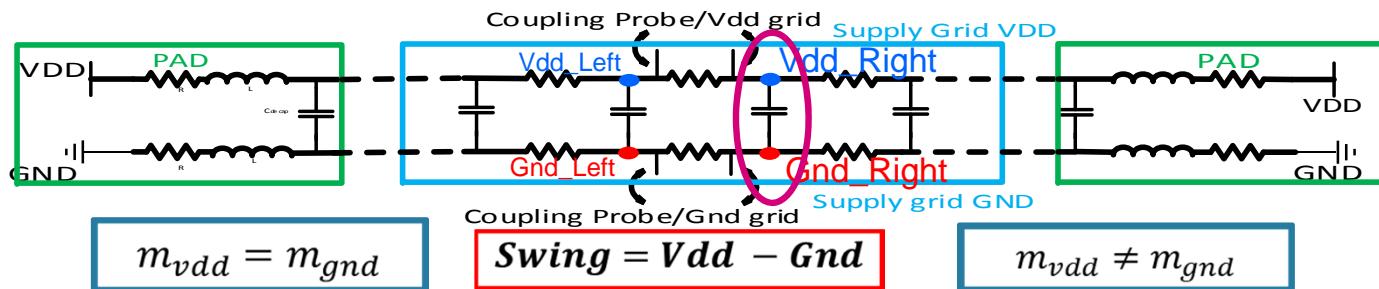
$$m_{gnd} = k_{gnd} \sqrt{L_{probe} \times L_{gnd}}$$

$$m_{vdd} = k_{vdd} \sqrt{L_{probe} \times L_{vdd}}$$

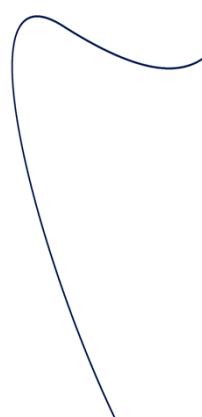


Modelling: Impact of an EMFI on IC

- Impact of EMFI on supply voltage.

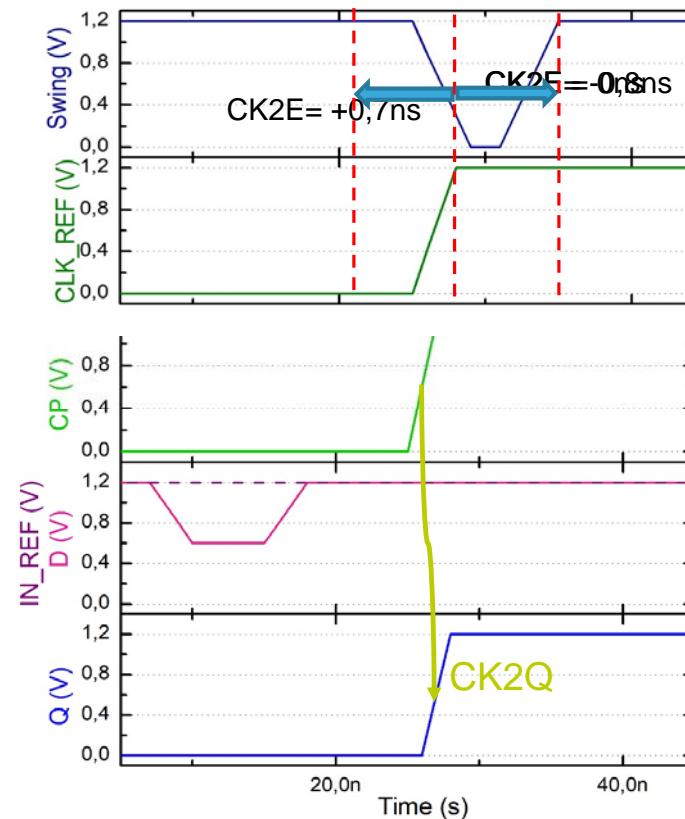
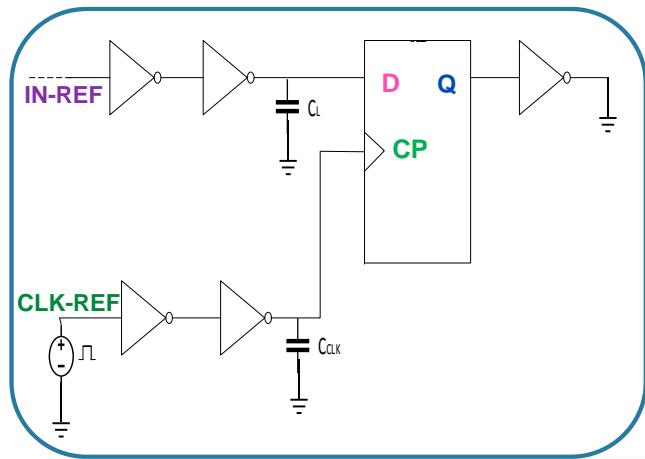
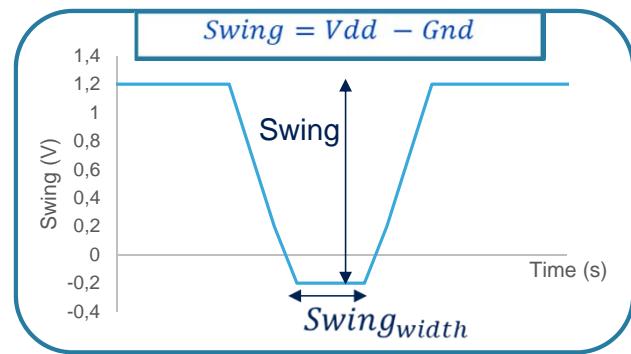


- Modelling: Impact of an EMFI on IC supply voltage
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Modelling: Impact of an EMFI on IC

- Testbench Simulation



Modelling: Impact of an EMFI on IC

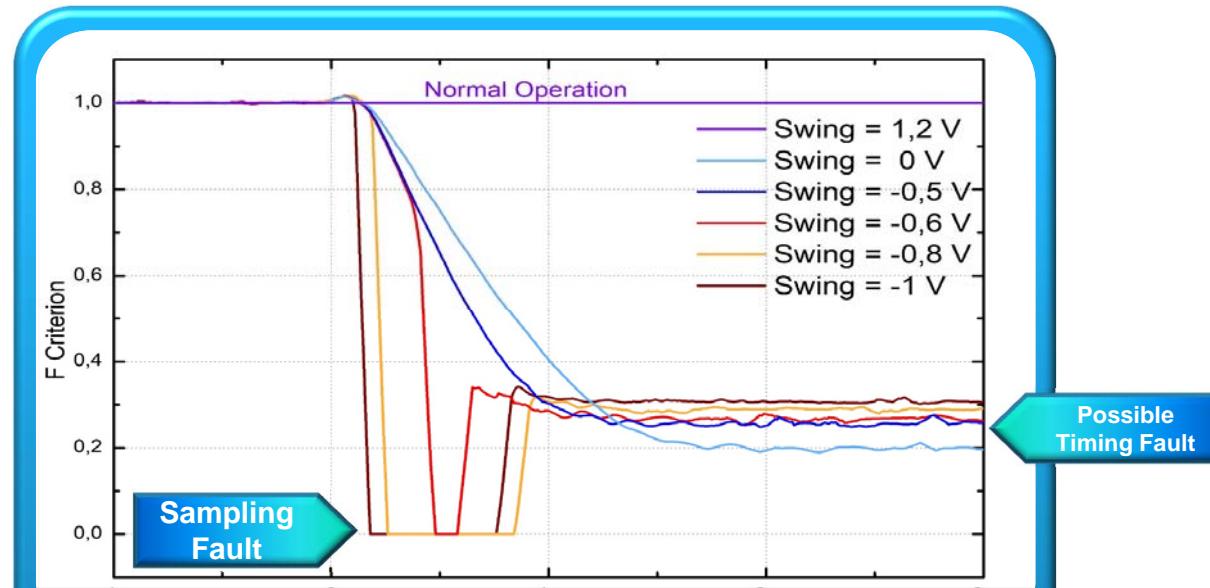
- Logic simulation: Swing amplitude impact on IC operation

Fault criterion F :

$$F = \frac{(CK2Q)_{ref}}{(CK2Q)_{inj}}$$

- $F = 1$ Normal Operation
- $0 < F < 1$ Delay
- $F = 0$ Sampling Fault

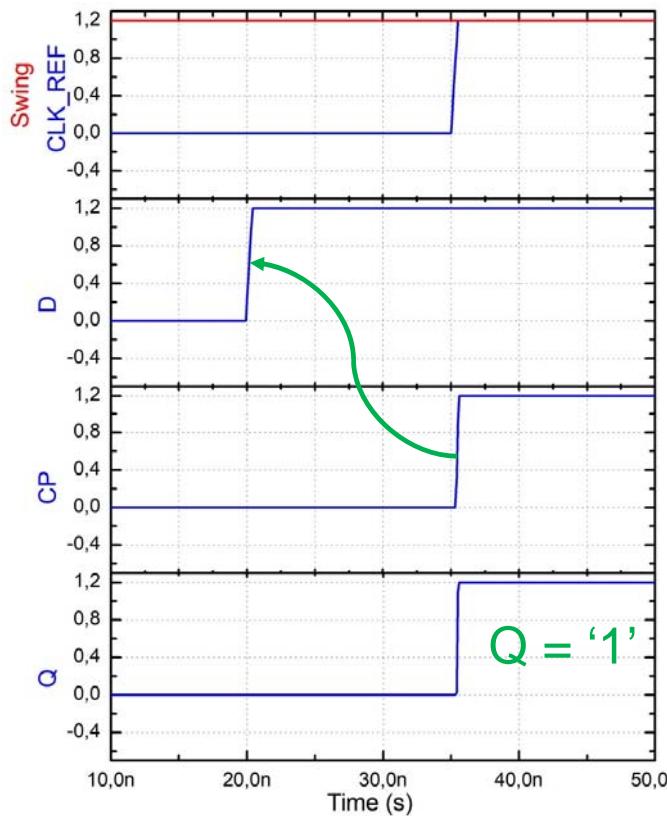
$$(CK2Q)_{inj} \geq (CK2Q)_{ref}$$



Modelling: Impact of an EMFI on IC

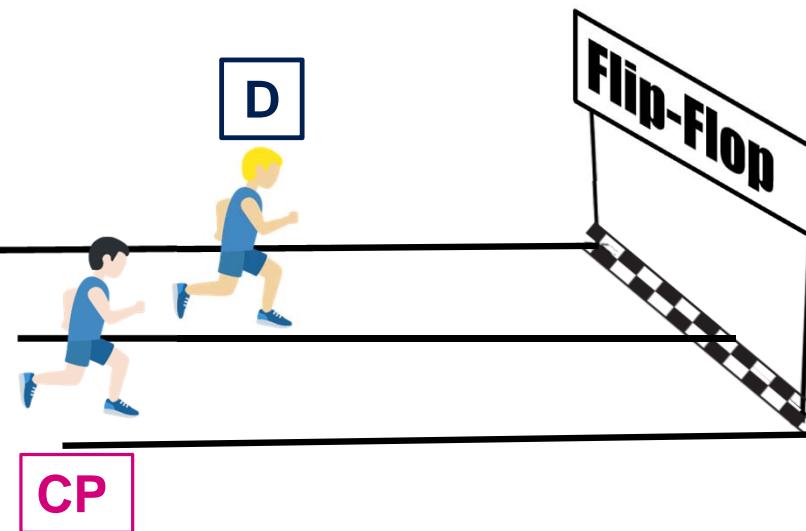
10

- Sampling Fault explanation



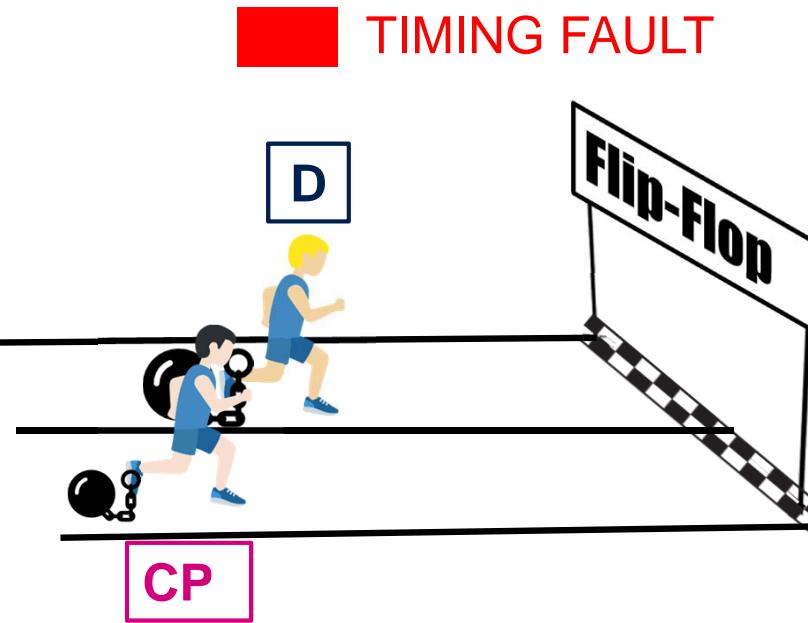
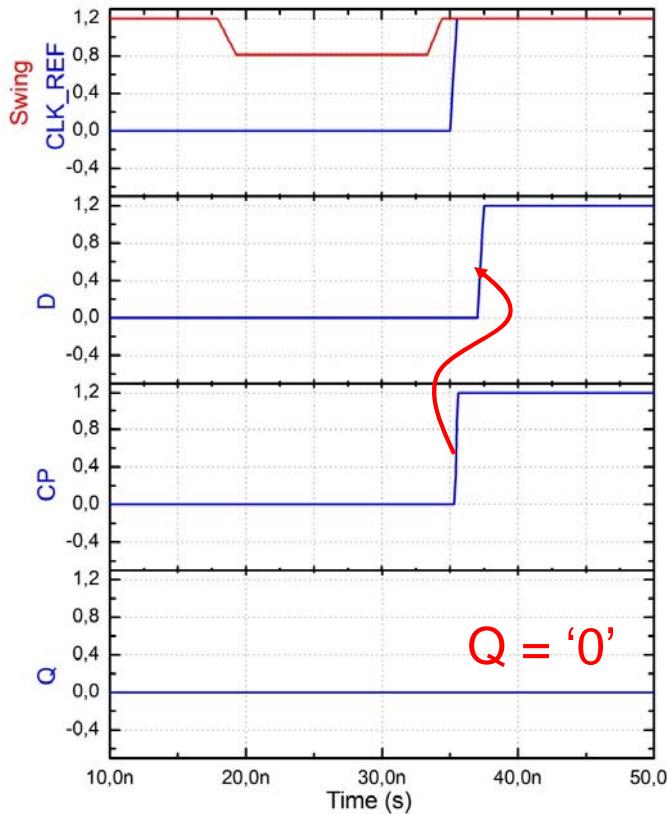
Normal Operation

NO FAULT



Modelling: Impact of an EMFI on IC

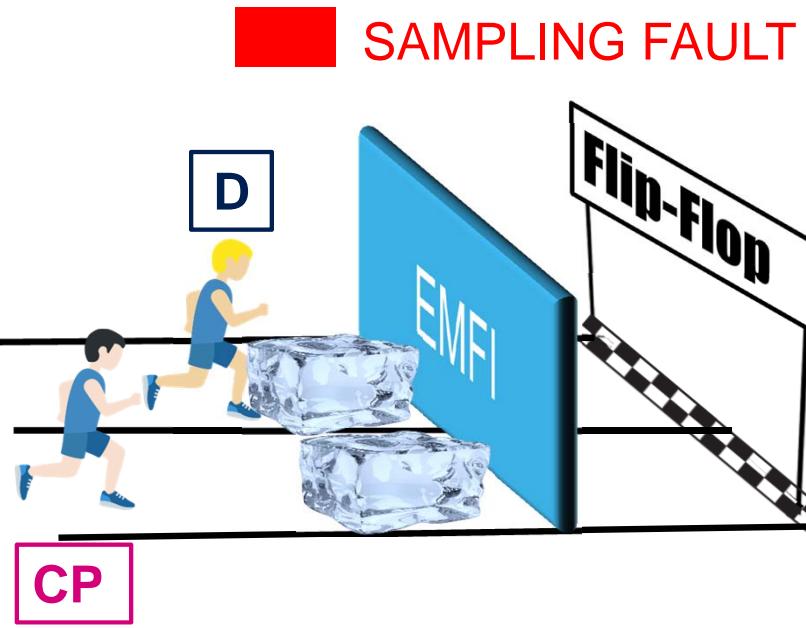
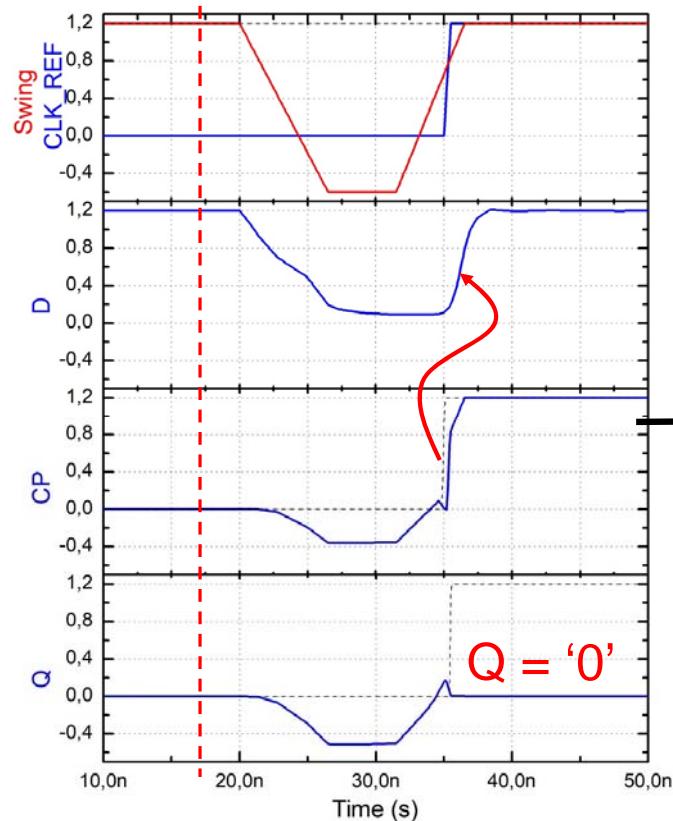
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Modelling: Impact of an EMFI on IC

12

- Sampling Fault explanation



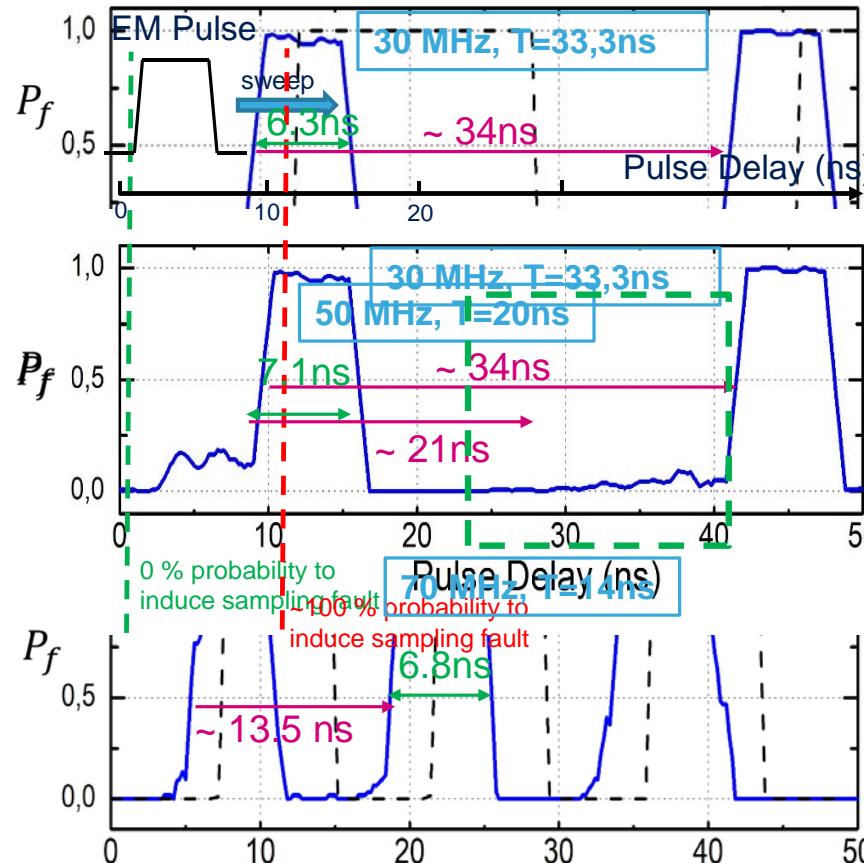
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EMFI experimental validation

- Effect of F_{CLK} variations

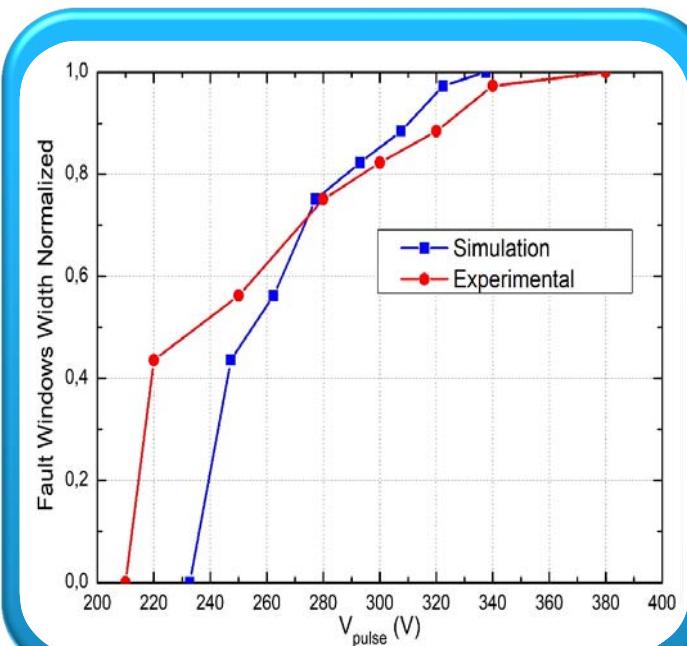
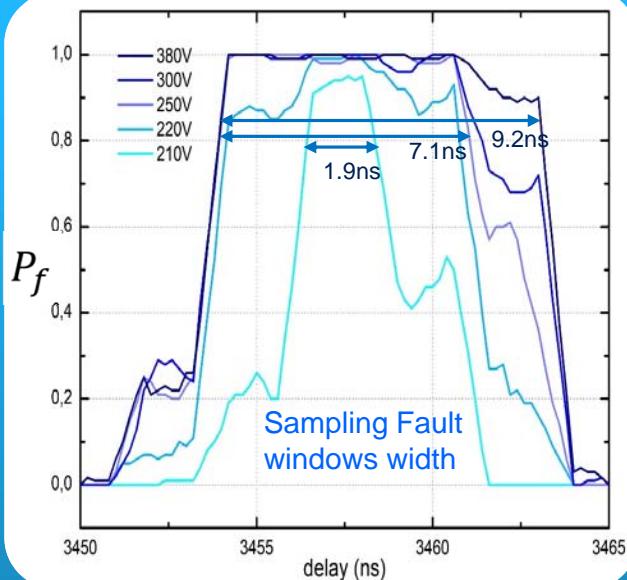
- Target : AES 128bits.
- EM pulse sweeps, for few periods, with a pulse delay step of 100ps.
- 50 EMFI shots are performed at each sweep to determine **fault probability P_f** ($0 < P_f < 1$).
- As expected **Sampling Fault Windows** appear with a period equal to that of the IC.
- Their width are **independent** of the frequency.



EMFI experimental validation

- Effect of V_{pulse} variations

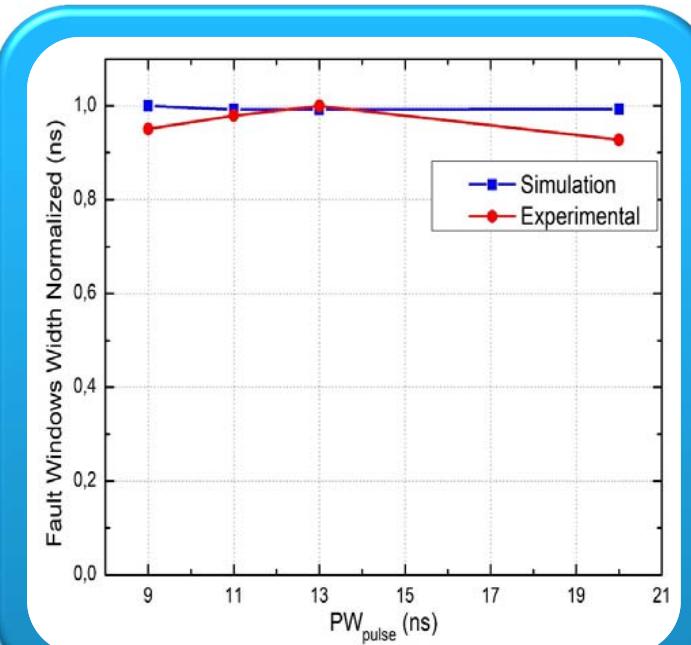
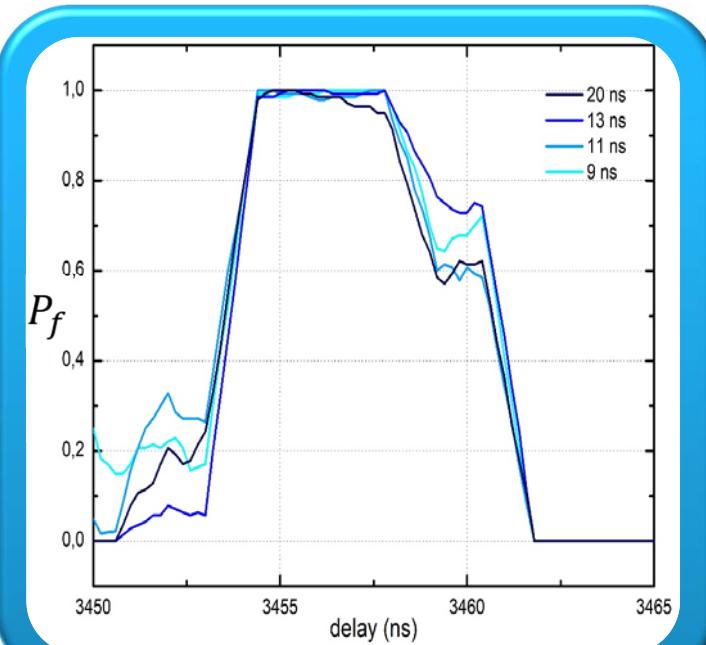
- Determine the evolution of the Sampling Fault Window width in function of V_{pulse} variations.
- The width of Sampling Fault Windows increases with V_{pulse} .



EMFI experimental validation

- Effect of PW variations

- Determine the evolution of the Sampling Fault Window width in function of PW variations.
- The Pulse Width does not affect much the sampling fault window.



Conclusion

17

- Conclusion

- Modelling simulations show that EMFI induces a voltage **bounces or drops** on power networks **Vdd and GND**. That could induce a **Swing drop**.
- Sampling Fault occurs when **EM Field** is applied during IC operation around rising CLK edge. In **simulation and experimentally**.



- Perspective

- More accurate **coupling model**.
- Experimental validation and parallel on **one register** only.



Thank you



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Modelling: Impact of an EMFI on IC

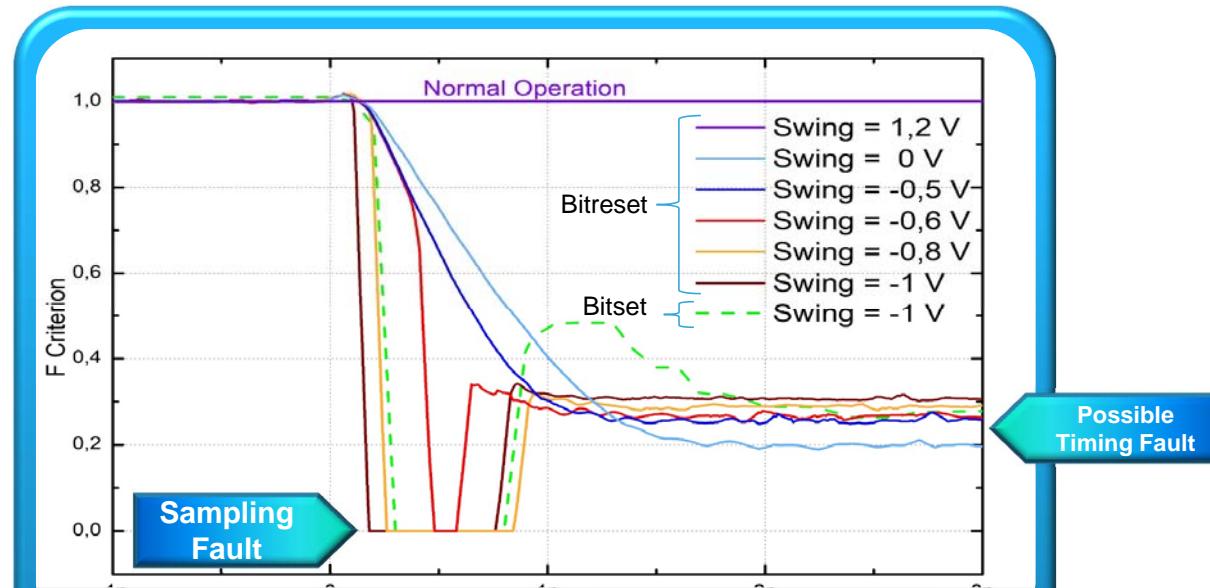
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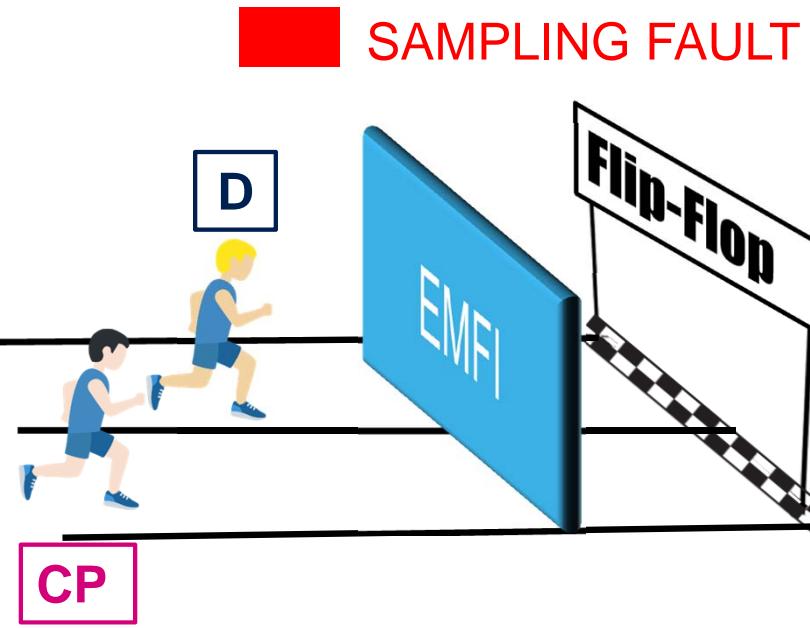
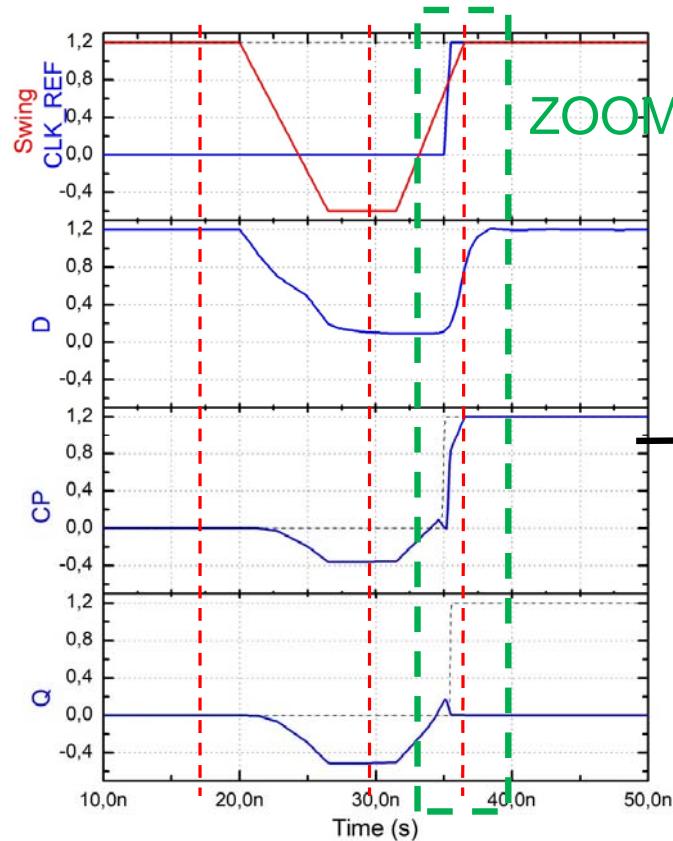
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Modelling : Impact of an EMFI on IC

20

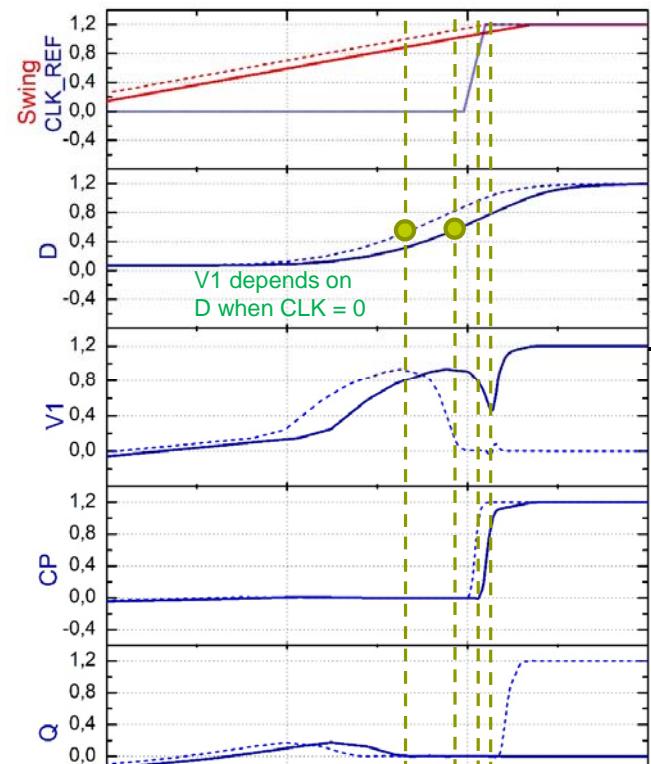
- Sampling Fault explanation



Modelling : Impact of an EMFI on IC

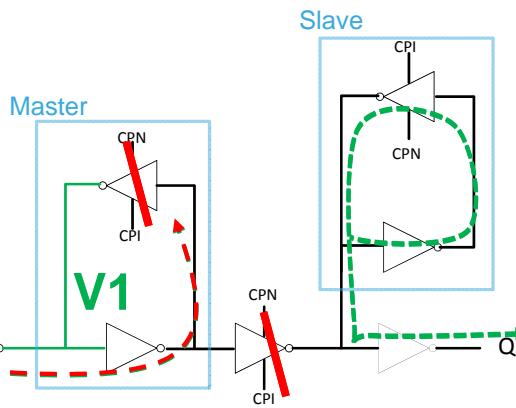
- Sampling Fault explanation

..... : $CK2Swing = 0 \text{ ns}$; No Fault
— : $CK2Swing = 0,3 \text{ ns}$; Sampling Fault



$CLK = 0$

V1 is disrupted during the D recovery



$CLK = 1$

If CLK edge occurs during V1 alteration : wrong value is sampled and stored in Master loop.

