Electromagnetic Fault Injection: How Faults Occur
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Electromagnetic Fault Injection: how faults occur?

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Introduction

• Context:

• Objectives:
  - Modelling: impact of an EMFI on IC supply voltage
  - SPICE simulation: impact of an EMFI on IC operation
  - Experimental validation
Modelling: Impact of an EMFI on IC supply voltage

Spice Simulation: impact of EMFI on IC operation

Experimental Validation
Modelling: Impact of an EMFI on IC

- **EM Induction: hypothesis?**

- **Metal wires from the power/ground networks form many loops.**

- **Interconnect logic wires don’t form loops.**

- **EMFI induces parasitic currents mostly in the power and ground networks.**

- EM induction induces currents variation on closed loops.
Modelling: Impact of an EMFI on IC

- Impact of EMFI on supply voltage.

\[
m_{\text{gnd}} = k_{\text{gnd}} \sqrt{L_{\text{probe}} \times L_{\text{gnd}}} \\
m_{\text{vdd}} = k_{\text{vdd}} \sqrt{L_{\text{probe}} \times L_{\text{vdd}}}
\]
Modelling: Impact of an EMFI on IC

- Impact of EMFI on supply voltage.

\[ m_{vdd} = m_{gnd} \]

**Swing = Vdd - Gnd**

\[ m_{vdd} \neq m_{gnd} \]

Swing is negative for few ns!
- Modelling: Impact of an EMFI on IC supply voltage
- Spice Simulation: impact of EMFI on IC operation
- Experimental Validation
Modelling: Impact of an EMFI on IC

- **Testbench Simulation**

![Diagram of testbench simulation](image)

**Swing = Vdd - Gnd**

**Swing**

**Swing\_width**

![Waveforms](image)

**CLK-REF**

**CLK**

**CP**

**Q**

**D**

**IN-REF**

**CLK-REF**

**IN\_REF**

**CLK**

**Q**

**D**

**CK2E = +0.7ns**

**CK2E = 0ns**

**CK2Q**

**Time (s)**

20.0n

40.0n
Modelling: Impact of an EMFI on IC

- Logic simulation: Swing amplitude impact on IC operation

Fault criterion F:

\[ F = \frac{(CK2Q)_{\text{ref}}}{(CK2Q)_{\text{inj}}} \]

- \( F = 1 \) Normal Operation
- \( 0 < F < 1 \) Delay
- \( F = 0 \) Sampling Fault
Modelling: Impact of an EMFI on IC

- Sampling Fault explanation

Normal Operation

Q = '1'

NO FAULT

Flip-Flop
Modelling: Impact of an EMFI on IC

- Sampling Fault explanation
Modelling: Impact of an EMFI on IC

- Sampling Fault explanation

![Graph showing sampling fault explanation with Q = '0' and EMFI impact on IC]
- Modelling: Impact of an EMFI on IC supply voltage
- Spice Simulation: impact of EMFI on IC operation
- Experimental Validation
EMFI experimental validation

- **Effect of $F_{CLK}$ variations**
  - Target: AES 128bits.
  - EM pulse sweeps, for few periods, with a pulse delay step of 100ps.
  - 50 EMFI shots are performed at each sweep to determine fault probability $P_f$ ($0 < P_f < 1$).
  - As expected, Sampling Fault Windows appear with a period equal to that of the IC.
  - Their width are independent of the frequency.
EMFI experimental validation

Effect of $V_{\text{pulse}}$ variations
- Determine the evolution of the Sampling Fault Window width in function of $V_{\text{pulse}}$ variations.
- The width of Sampling Fault Windows increases with $V_{\text{pulse}}$. 

![Graph](image-url)
EMFI experimental validation

- **Effect of PW variations**
  - Determine the evolution of the *Sampling Fault Window width* in function of *PW variations*.
  - The Pulse Width does not affect much the sampling fault window.
• Conclusion
  ➢ Modelling simulations show that EMFI induces a voltage **bounces or drops** on power networks **Vdd and GND**. That could induce a **Swing drop**.
  ➢ Sampling Fault occurs when **EM Field** is applied during IC operation around rising CLK edge. In **simulation** and **experimentally**.

• Perspective
  ➢ More accurate **coupling model**.
  ➢ Experimental validation and parallel on **one register** only.
Thank you

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Modelling: Impact of an EMFI on IC

- Logic simulation: Swing amplitude impact on IC operation

Fault criterion $F$:

\[
F = \frac{(CK2Q)_{ref}}{(CK2Q)_{inj}}
\]

- $F = 1$ Normal Operation
- $0 < F < 1$ Delay
- $F = 0$ Sampling Fault

![Diagram showing F criterion for different swing levels]
Modelling: Impact of an EMFI on IC

- Sampling Fault explanation
Modelling: Impact of an EMFI on IC

- Sampling Fault explanation

- V1 is disrupted during the D recovery

- If CLK edge occurs during V1 alteration: wrong value is sampled and stored in Master loop.