Self-Robust Non-Volatile C-element for Single Event Upset Enhanced Tolerance

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Abstract

For embedded systems in harsh environments, a radiation robust circuit design is still an open challenge. As circuits become more and more complex and CMOS processes get denser and smaller, their immunity towards particle strikes decreases drastically. Due to its proven resistance to radiation effects and its inherent non-volatility, Spin-Transfer-Torque-based Magnetic Tunnel Junction (STT-MTJ) is considered as a serious promising candidate for high reliability electronic. The first radiation hardened STT-MTJ based Non-Volatile C-element is presented in this paper. This hybrid VLSI structure addresses the problem of the non-volatile error occurrence by avoiding MTJs radiation induced magnetization reversal.

1. Introduction

Solar wind and flare, cosmic radiation and Van Allen Belt are some of the main sources of particles flux (protons, electrons, alpha particles...) in space, involving energy ranging from hundreds of KeV to millions of MeV. Since shielding technique shown important limitations and transistor scaling leads to a relevant impact of soft error even in terrestrial environment [5] a radiation-hard IC design becomes a real challenge. Physically, the interaction of such particles with the active region of CMOS ends up in numerous undesirable events that could cause a failure or even destroy the transistor. A Single Event Transient (SET) is an unwanted current pick, due to the accumulation of electron-hole pairs separated and collected near the reverse biased junction of the device. When the collection of this charge overcomes the maximum value that can be tolerated from a memory node without resulting in a bit-flip (Q_{critic}), a Single Event Upset occurs (SEU). A Multi Event Upset (MEU) could occur in case that several close nodes have affected simultaneously from the radiations. However, if the voltage pulse induced by the strikes does not exceed the breakdown voltage of the transistors, the failures are classified as non-disruptive since they can be corrected by reprogramming the circuit into its previous logic state. In the last decade, the evidence of the intrinsically MTJ robustness to radiation effects leads them to be subject of robust design investigation. Indeed, some design of hybrid latches have been proposed in [1], [6] and [3] as well as a magnetic radiation hard unit has introduced in [2] and [4]. However, when integrated in CMOS circuit, MTJ could be affected by radiation-induced errors, namely a bit- flip of the stored information, precisely because of the surrounding peripheral circuits. Hence, specific hardening technique for MTJ must be investigated since they are still vulnerable to radiations. Dealing with this issue has become more and more urgent as, in the last years, the evolution of MTJ-based technologies allows smaller and smaller writing currents, making easier for a SEU to induce on the writing/reading transistors a charge transfer, resulting in a magnetic orientation reversal. In this paper, the first radiation hardened Non-Volatile C-element is presented with the aim to take advantage of the error filtering capability of the C-element and at the same time of the intrinsic MTJ robustness to radiation, with a special regard to the avoidance of non volatile errors.

2. Proposed Solution

C-element is a state holding circuit, which is transparent when all its inputs are equal, and holds the previous output otherwise. Due to the use of MTJ, this unit combines together the capability to block a mismatch propagation and to store in the same unit the correct bit.
The MTJ nano-pillar structure, consists of a thin insulating barrier sandwiched between two ferromagnetic layers: a reference layer with a fixed magnetization and a storage layer with a switchable magnetization. Depending on the mutual magnetic orientation of the two layers

(parallel or anti-parallel) the resistance changes being either low-state or high-state allowing the storage of bit ”0” or ”1” respectively. In the NV C-element implementation MTJs are used to store the output state and its complement while CMOS part takes part of the combinational part. In between the various C-element implementations the Single Inverter Latch (SIL) C-element results to be the most soft-error resilient due the lowest number of sensitive nodes with respect to the total. The first innovation we propose is to make the C-element non volatile: two MTJs and five transistors are employed for this purpose, as depicted in Fig. 1. The circuit level implementation consists of pull up transistors (P1, P2) pull-down transistors (N1, N2) inverter (P4, N4) and weak inverter (P3, N3). Read operation (involving N5, N6, N7 and P5) is achieved by equalizing the voltage of the output node and of its complement, (Az signal) hence sensing the value of the MTJs resistance (Rd signal). A second novelty consists in adding transistors N9 and N10 to avoid/reduce the occurence of non volatile errors.

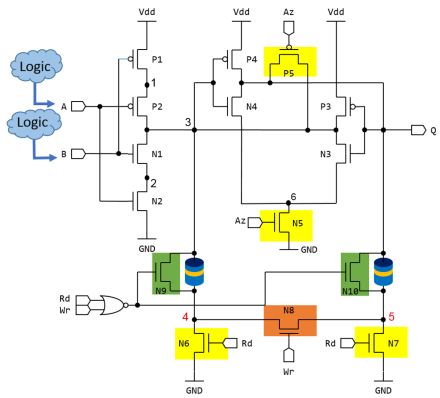

Figure 1. Proposed radiation tolerant Non Volatile implementation of the C-element. The numbers in the circuit represent the sensitive nodes.

SEUs were injected into the sensitive nodes of the circuit using a double exponential current pulse as depicted in Fig. 2. Error simulations shown that a charge of 100 fC in node 4 and/or in node 5 is already sufficient to reverse the storage layer magnetic orientation if N9 and N10 are removed. On the contrary, with the insertion of these two NMOS in parallel to each MTJ, a resistive partition path for the current pulse induced by the particle is obtained. Hence, provided that $R_{\text{on}} << R_{\text{p}}$, the quantity of current flowing into the MTJs will not be enough to induce their switching.
Simulation results summarized in Table II show that the insertion of the two NMOS in parallel to the MTJs increases the circuit robustness to non-volatile errors up to 3 times with respect to the solution without the shunt path. As highlighted in Fig. 3, Q regains quickly ($\sim$ 1ns) its original value and the values stored in the MTJs are not affected at all.

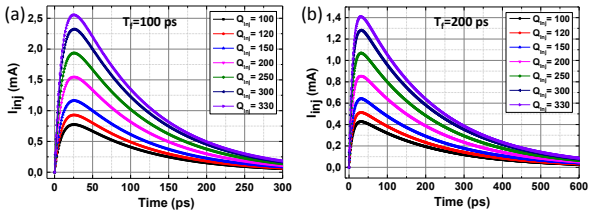

Figure 2. Transient current pulse waveforms of the radiation particle strikes corresponding to different values of the simulated injected charge for a fixed τ_{r}= 10 ps.

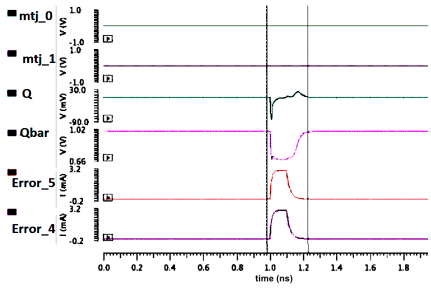

Figure 3. Transient simulation waveforms of the SEU tolerant proposed non-volatile C-element when Q_{inj}=300 fC in node 4 and 5.

3. Conclusion

In this paper, an STT-MTJ based C- element with enhanced SEU tolerance capability has been proposed. Error injections in sensitive nodes of the circuit attested that only two nodes could lead to non-volatile errors and thus to SEU. A circuit level solution has been proposed and tested through simulations to avoid/ lessened their occurence. Concerning the CMOS part the radiation hardening achievement has to deal with trade-off involving transistor width and speed, in particular as Vdd is scaled down.

References

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