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Evaluation of embedded STT-MRAM for Ultra Low Power applications

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Abstract

The complexity of embedded devices increases as today's applications request always more services. However, the power consumption of SoC has significantly increased due to the high-density integration and the high leakage power of current CMOS transistors. To address these issues, emerging technologies are considered. Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) is seen as a promising alternative solution to traditional memories thanks to its negligible leakage current, high density, and non-volatility. Considering low-power applications with duty-cycled behaviours, we evaluate STT-MRAM as a replacement for both embedded Flash and SRAM.

1. Introduction

Nowadays, embedded systems are widely used in various application requiring space deployment, thanks to their flexibility and low implementation cost compared to wired solutions [11]. However, many of these applications set high constraints for designers and developers in terms of performance and energy consumption. While the complexity of embedded devices is continuously increasing, the power consumption of systems-on-chip is a challenge for battery-powered applications. Having long autonomy for such devices becomes a real need. The energy consumption of an Ultra-Low Power (ULP) microcontroller can be optimised at multiple levels. A lot of ULP applications have a periodic behaviour, alternating between run and sleep phases (“duty-cycle” operation mode, Fig. 1 (a)). The time spent in each phase depends on the application specifications and selected solutions. Even though sleep modes help to reduce the power consumption of a microcontroller, some energy is still lost during sleep phases. As a workaround, it is possible to power down a microcontroller during sleep phases (Fig. 1 (b)), but for traditional architectures the system state is then lost, forcing a system reboot. Another solution is to insert Non-Volatile Logic (NVL) inside the architecture to make it able to store its state before a shut down, and restore it after wake-up (normally-off computing, Fig. 1 (c)). State recovery by using NVL is faster and more energy efficient

than a full restart [1], but this solution adds an overhead in terms of area and makes the go-to-sleep phase time longer. This method also requires some energy to store the system state and restore it at wake-up. Comparing the traditional microcontroller with the normally-off solution, there is a trade-off between the energy lost in sleep phase (Fig. 1 (a)) and the backup energy overhead (Fig. 1 (c)).

Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) is seen as a promising alternative solution to traditional memories thanks to its negligible leakage current, high density, and non-volatility. In comparison to Flash and FeRAM, STT-MRAM offers lower access latencies, higher retention and density ([9, 1]). By combining the 28-nm FD-SOI technology for CMOS and STT-MRAM solution for the memory system, we investigate the different architectural solutions to improve the energy efficiency, reliability, and performances of systems-on-chip for ULP applications.

2. Design evaluation

Characterization of new design and comparison with existing ones are necessary to evaluate the potential gains bring by new architectures and technologies. Moreover, they have to be done at application level to justify the use of these innovations and the investments required for their manufacturing and deployment. However, in embedded applications, especially for Internet of Things end-node devices, ULP SoCs have to interact with their environment. Modelling a complete SoC and the peripheral components, their interaction and low-power policies, can be very complex in terms of development and benchmarking.

Many works present physical implementations with dedicated architectures ([8]) and using new technologies and power management techniques (example with non-volatile logic and non-volatile RAM: [5]). If it is possible to integrate them in an application for accurate evaluation, they are prototypes mostly used for validation, not flexible enough for design space exploration. Simulation is one of the solutions for sensor node evaluation that is flexible and affordable to perform this investigation at various level. However, there is a trade-off between accuracy and simulation speed: the more accurate we want to be, the slower the simulation will be and so at every level, from the SoC evaluation [3] to the radio model [4]. Moreover,

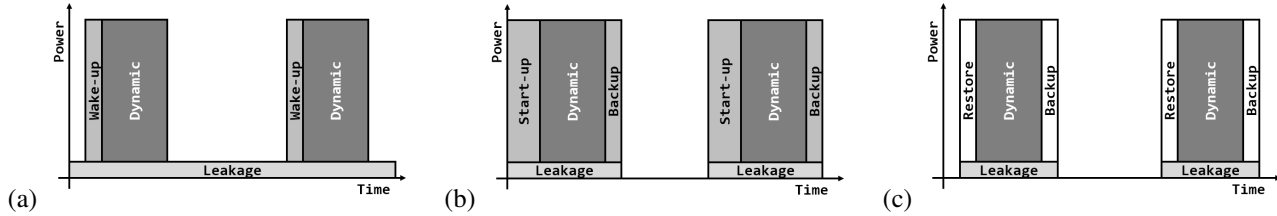


Figure 1. Duty-cycle operation: (a) Sleep mode (b) Power down mode (c) Normally-off computing

some models are not exempt from bugs and/or not accurate enough because of abstractions, simplifications and underestimated effects, especially for wireless communications [6, 7].

Power emulation using FPGA acceleration [2] is a solution between the flexibility of simulation tools and the accuracy and speed of a physical SoC. With FPGA prototyping, every signal of the implemented design is reachable like for RTL simulation. Performance and power estimation can be done by using monitoring tools with adapted models. As ULP SoCs usually run at low frequencies, it is possible to perform an evaluation with real-time execution, so the integration of an FPGA-based system inside an already deployed sensors networks is also possible for application level evaluation.

We have developed an FPGA-based platform for new designs evaluation [10], on which it is possible to reproduce the behaviour of STT-MRAM based solutions and so to investigate its integration inside ULP SoC taking account of the application context. With adapted power models, we can perform energy consumption estimation at real time thanks to dedicated monitoring tools.

3. Conclusion

MRAM is seen as a promising solution to replace traditional memory technologies to improve performances and reduce the energy consumption of ULP SoC for low power embedded applications. However, evaluations at application level are needed to evaluate and optimize the integration of STT-MRAM inside low-power microcontrollers. We have developed and use an FPGA-based platform to perform real-time cycle accurate evaluation. This platform, which can be interfaced with commercial or custom peripheral components, makes possible evaluations taking account of the application context.

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