

## Physical design and optimisation methods for TSV-based 3D and monolithic 3D integration

Aida Todri-Sanial

## ▶ To cite this version:

Aida Todri-Sanial. Physical design and optimisation methods for TSV-based 3D and monolithic 3D integration. ESSDERC-ESSCIRC 2019 - 15th Workshop on Heterogeneous Integration of Nanomaterials and Innovative Devices, Sep 2019, Krakow, Poland. pp.217-220. lirmm-02387999

## HAL Id: lirmm-02387999 https://hal-lirmm.ccsd.cnrs.fr/lirmm-02387999

Submitted on 22 Dec 2019

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers. L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés. Aida Todri-Sanial, LIRMM, University of Montpellier, CNRS Montpellier, France Email: <u>todri@lirmm.fr</u>

This talk aims to unveil how to effectively and optimally design 3D circuits covering aspects from 3D stacking to monolithic integration. As first, an overview of physical design challenges with respect to conventional 2D circuits will be provided, followed by an in-depth look into the power and thermal integrity challenges and solutions. More specifically, design challenges related to power, signal and clock distribution will be covered and also present some of the current solutions. Secondly, an overview of the reliability concerns for 3D circuits and their mitigation techniques will be presented. The talk will conclude with current challenges and future directions for 3D physical design.

## **References:**

- 1. A. Todri-Sanial and C.S Tan, "Physical Design for 3D Integrated Circuit," CRC PRESS 2015, ISBN: 9781498710367.
- 2. A. Todri-Sanial, "Overview of Physical Design Issues for 3D ICs," book chapter in *Physical Design for 3D ICs*, Edited by A. Todri-Sanial and Ch. S. Tan, CRC PRESS 2015, ISBN: 9781498710367.
- 3. A. Todri-Sanial, "Design Methodology for 3D Power Delivery Networks," book chapter in *Physical Design for 3D ICs*, Edited by A. Todri-Sanial and Ch. S. Tan, CRC PRESS 2015, ISBN: 9781498710367.
- 4. Y-L. Zhao, J-L. Yang, W-Sh. Zhao A. Todri-Sanial, Y. Cheng, "Power Supply Noise Aware Task Scheduling on Homogeneous 3D MPSoCs Considering the Thermal Constraint," in *Journal of Computer Science and Technology* 33(5): 1-17, September 2018, doi: 10.1007/s11330-015-0000-0.
- A. Todri-Sanial and Y. Cheng, "A Study of 3-D Power Delivery Networks with Multiple Clock Domains," in *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol. 24, no. 11, pp. 3218-3231, Nov. 2016. doi: 10.1109/TVLSI.2016.2549275
- Y. Cheng, A. Todri-Sanial, J. Yang and W. Zhao, "Alleviating Through-Silicon-Via Electromigration for 3-D Integrated Circuits Taking Advantage of Self-Healing Effect," in *IEEE Transactions on Very Large-Scale Integration* (VLSI) Systems, vol. 24, no. 11, pp. 3310-3322, Nov. 2016. doi: 10.1109/TVLSI.2016.2543260.
- A. Todri-Sanial, S. Kundu, P. Girard, A. Bosio, L. Dilillo, A. Virazel, "Globally Constrained Locally Optimized 3-D Power Delivery Networks," in *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol.22, no.10, pp.2131-2144, 2014, doi: 10.1109/TVLSI.2013.2283800.
- 8. A. Todri, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, "Uncorrelated Power Supply Noise and Ground Bounce Consideration for Pattern Generation," in *IEEE Transactions on Very Large-Scale Integration* (*VLSI*) *Systems*, vol.21, no.5, pp.958-970, 2013, doi: 10.1109/TVLSI.2012.2197427.
- 9. A. Todri, S. Kundu, P. Girard, A. Bosio, L. Dilillo, A. Virazel, "A Study of Tapered 3D TSVs for Power and Thermal Integrity," in *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol.21, no.2, pp.306 319, 2013, doi: 10.1109/TVLSI.2012.2187081.
- 10. A. Todri, M. Marek-Sadowska, "Reliability Analysis and Optimization for Power Gated ICs with Multiple Power Gating Configurations," in *IEEE Transactions on Very Large-Scale Integration Systems*, vol.19, no.3, pp.457-468, 2011, doi: 10.1109/TVLSI.2009.2036267.
- 11. A. Todri, M. Marek-Sadowska, "Power Delivery for Multi-Core Systems," in *IEEE Transactions on Very Large-Scale Integration Systems*, vol.19, no.12, pp.2243-2255, 2011, doi: 10.1109/TVLSI.2010.2080694.
- A. Koneru, A. Todri-Sanial and K. Chakrabarty, "Reliable Power Delivery and Analysis of Power-Supply Noise During Testing in Monolithic 3D ICs," 2019 IEEE 37th VLSI Test Symposium (VTS), Monterey, CA, USA, 2019, pp. 1-6. doi: 10.1109/VTS.2019.8758650
- 13. A. Koneru, A. Todri-Sanial and K. Chakrabarty, "Power-Supply Noise Analysis for Monolithic 3D ICs Using Electrical and Thermal Co-Simulation," *2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Bordeaux, 2018, pp. 217-220. doi: 10.1109/ICECS.2018.8617951