Importance of Interconnects: A Technology-System-Level Design Perspective

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(Invited paper)

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***Abstract*—**Current technology-design optimization methodology focuses first on front-end devices and logic gates and then addresses back-end interconnects. But, such approach is no longer feasible for sub-nanometer technologies. Here, we present a circuit-level study where both devices and interconnects are co-optimized to improve energy efficiency. We investigate advanced CMOS technology with 7 nm FinFET devices, and Cu interconnects with various aspect ratios from 3, 5 to 10. Further, we explore the advantages of carbon nanotube (CNT) based circuits with CNT field-effect devices and interconnects. CNT technology can achieve better energy-delay-product with co-exploring front- and back-end co-optimization and paving the way for an intelligent circuit-/system-level design and technology co-optimization.

I. Introduction

We are on the verge of the 4th Industrial Revolution era [1] which is characterized by a variety of new technologies intertwining both physical and cyber worlds. We will witness a more significant usage of semiconductor devices as the number of connected devices continues to grow exponentially and reaching 125 billion by 2030 [2]. Therefore, modern integrated circuits will continue to become more complex and transistor count will increase considerably. The recent semiconductor node with the highest transistor density is TSMC's 5-nanometer node with 171.3 million transistors per square millimeter [3].

Despite the technological advancements, several key challenges arise due to the unprecedented connectivity and data generated from connected devices. One key challenge is achieving fast performance and ultra-low power consumption. To address this challenge, the semiconductor industry has made several breakthroughs in terms of faster and higher density transistors. But, interconnects have somewhat been overlooked. Conventional copper (Cu) interconnects suffer from high resistivity due to surface scattering and grain boundary effects from scaling. Continued scaling of inter- connect aspect ratios have led to an increase in interconnect parasitics, contacts and vias resulting in excess voltage drop, which have limited transistor performance. Thus, as transistor performance improved with scaling, interconnects suffered, which overall restrained the advantages gained through scaling of FinFET devices [4]. As the industry is preparing for 7 nm node production and looking ahead into 5 and 3 nm nodes, several challenges arise due to interconnects, which requires re-thinking of interconnect topologies/materials and technology-physical design optimization approach.

II. Importance of Interconnects

We perform circuit-level simulation on a simple benchmark of ring oscillator where a single stage is illustrated in Fig.1a. We investigate both front-end devices and back-end interconnects with two technologies: 1) advanced CMOS technology of 7 nm FinFET devices and Cu interconnects, and 2) carbon nanotube (CNT) based technology field-effect transistor (CNTFETs), and multi-wall CNT (MWCNT) interconnects.

A. Benchmark with FinFET and Cu Interconnects

We use the ASAP7 library, which is a 7 nm FinFET predictive process design kit [5]. We apply the original FinFET model with TT (regular) mode and vary the number of fins. We use the Predictive Technology Model (PTM) [6] and obtain the resistance and capacitance analytical formula and a resistivity value fitting of 11.4 μΩ-cm for 7 nm Cu line width. We perform circuit-level simulations with 7 nm FinFET devices and vary the number of fins from 3, 5 to 10. For each fin number case study, we investigate interconnects by representing them as ideal interconnects (no parasitics), and Cu interconnects with different aspect ratios (AR) as 3, 5 and 10. We compute delay, power and energy-delay-product (EDP) and compare for each case study. Detailed values are summarized in Table I and Fig. 2. Overall, we observe interconnects play an important role in circuit delay, power and EDP. For example, for FinFET devices with three fins, Cu interconnects with AR=3 increase circuit power and delay up to 232% and 128%, respectively compared to ideal Cu lines. While both power and delay improve with increasing Cu interconnect aspect ratios, nevertheless it is challenging from integration perspective to process such high aspect ratios. Similarly, increasing the number of fins improves both power and delay, suggesting the need for physical design and technology to trade-off between Cu line AR and device fin number.

B. Benchmark with CNTFETs and CNT Interconnects

CNTFET inverter structure is based on [7] and MWCNT interconnect (Fig.1b) are based on [8-9]. The layout design for CNT benchmark is in Fig. 3. We use the VS-CNTFET (Virtual-Source Model for Carbon Nanotube FETs) device model developed by [10]. Device model parameters are based on the user manual suggestions such as 11.7 nm and 12,9 nm for the gate and contact lengths respectively, and single wall CNT (SWCNT) diameter of 1.2 nm. Device parameters are optimized for CNTFET gate delay based on the 2023 node of the IRDS projections [11] (i.e., $L_{Gatepitch}$ = 28.1 nm, L_{M1} = 25.2

nm and L_{pitch} = 31.1 nm) for 5 nm technology node. We vary the gate width *W* and tube-to-tube spacing *s* to alter the number of SWCNTs in the FET channel. MWCNT interconnects are introduced at gate-level, and we employ the model of pristine and doped MWCNTs. MWCNT interconnect doping concentration is represented by CNT Fermi-level shift E_f which increases electron density of state (DOS), thus introducing additional conducting channels and further enhancing CNT interconnect conductivity [9]. We consider end-contacts between CNTFET device and MWCNT interconnect with various values to present different metal materials [12-16]. It is important to note that the layout design for CNT benchmark is optimized for CNT interconnects to allow long interconnects and fewer contacts (Fig.3).

In Fig. 4(a), EDP is plotted with ideal interconnects (no parasitics) where EDP increases with *s* and decreases with *W*. As *s* gets larger (or fewer SWCNTs in the FET channel), it improves power consumption by reducing the drive current which also worsens the delay. In Fig. 4(b), EDP results are shown for 7 nm diameter pristine MWCNT interconnects. Comparing with ideal interconnects (Fig. 4(a)), circuit-level EDP for $W = 1\ \mu m$ has drastically increased. We introduce doping on MWCNTs for improving interconnect performance and power. EDPs with heavily doped MWCNTs are shown in Fig. 4(c) and it gets close to EDP of ideal interconnect (Fig. 4(a)). Interconnect performance improves with doping and devices become again dominant for circuit-level performance. In Fig. 4(d), we present EDP improvement with different doping concentrations. For example, EDP improves by 90% and 75% with light (E_f = 0.1 eV) and heavy (E_f = 0.3 eV) doping compared to pristine interconnects for CNTFET width, $W = 1\ \mu m$ and small tube spacing.

C. Comparison

We compare benchmarks with CNT and advanced CMOS technologies. For a fair comparison, we set CNTFET gate width as $W = 213\ nm$, comparable to a tri-gate 3 fin FinFET where effective channel width $3W_{eff} = 3 \times (2H_{fin} + T_{fin}) = 213\ nm$ [10]. In Fig. 5(a), we show benchmark comparisons with ideal interconnects in terms of delay and power consumption. We observe that the FinFET benchmark has better power consumption, whereas the CNT benchmark has a better performance when the CNT spacing $s < 9\ nm$ (or ~25 SWCNTs in the CNTFET). In Fig. 5(b), we show delay and power consumption with pristine interconnects. We consider doped MWCNTs with E_f = 0.3 eV and Cu interconnects of aspect ratio 5. We remark that CNT benchmark has better circuit performance than advanced CMOS benchmark when CNTFET spacing $s < 23\ nm$ (or ~9 SWCNTs inside CNTFET). Contrarily, power consumption improves when $s > 23\ nm$. In Fig. 5(c), we show the EDP of CNT benchmark and find a trade-off point for delay and power when CNTFET has spacing of $s \sim 9\ nm$ with doped MWCNT interconnects. We also find that for $s \leq 7\ nm$ and doped MWCNT interconnects, the CNT EDP is better than the EDP of the benchmark with FinFET and Cu interconnect with aspect ratio 10.

These simulations further motivate to investigate technology and system-level co-optimization for power, performance and energy efficiency as an alternative method to explore their physical design and premise of novel devices and interconnect materials. They also highlight the critical role of interconnects and the prospect of carbon nanotube interconnects for advanced sub-nanometer nodes.

III. Conclusions

Back-end timing closure for on-chip interconnects has now become a significant obstacle for designers who are migrating to smaller semiconductor geometries and FinFET transistors. It is essential to dedicate a higher priority to the interconnects earlier in the design stages, such that interconnects are optimized for functionality, placement, performance, latency, power, and area before the front-end design migrates to the physical back end of the process. Maybe there should also be a paradigm shift in how we approach technology and physical design optimization. First focusing on optimizing front-end devices and logic gates, and then addressing BEOL interconnects is no longer feasible for sub-nanometer nodes. However, a more system-level approach can be relevant where both interconnects, and circuits (logic gates to IP) are optimized simultaneously while considering interconnects. This work also provides compelling insights into the benefits and cost of carbon nanotube-based circuits and interconnects as a viable technology to improve circuit energy efficiency.

Acknowledgment

This work has received funding from the EU Horizon 2020 CONNECT project under grant agreement No 688612.

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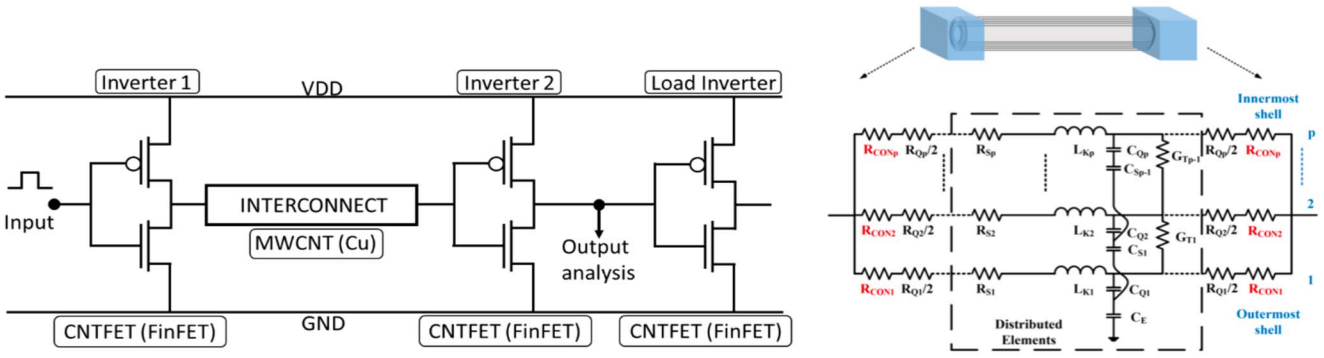


Fig. 1. (a) Illustration of small section of ring oscillator benchmark to demonstrate the circuit-level schematic which is implemented with 1) CNTFET devices and MWCNT interconnects between inverter gates, and 2) 7 nm FinFET devices with Cu interconnects with various aspect ratios. (b) MWCNT interconnect electrical compact model [9].

Table 1. Advanced CMOS technology: 7nm FinFET devices with Cu interconnects.

Cu Aspect Ratio (A/R)	3 Fins			5 Fins			10 Fins		
	Delay (ps)	Power (uW)	EDP (fJ·ps)	Delay (ps)	Power (uW)	EDP (fJ·ps)	Delay (ps)	Power (uW)	EDP (fJ·ps)
Ideal Interconnect	12.08	0.50	0.08	12.08	0.84	0.12	12.08	1.68	0.25
A/R = 3	27.49	1.66	1.25	22.36	1.98	0.99	17.73	2.85	0.90
A/R = 5	22.35	1.16	0.58	18.77	1.47	0.52	15.22	2.31	0.53
A/R = 10	15.95	0.78	0.20	15.11	1.12	0.26	13.50	1.95	0.36

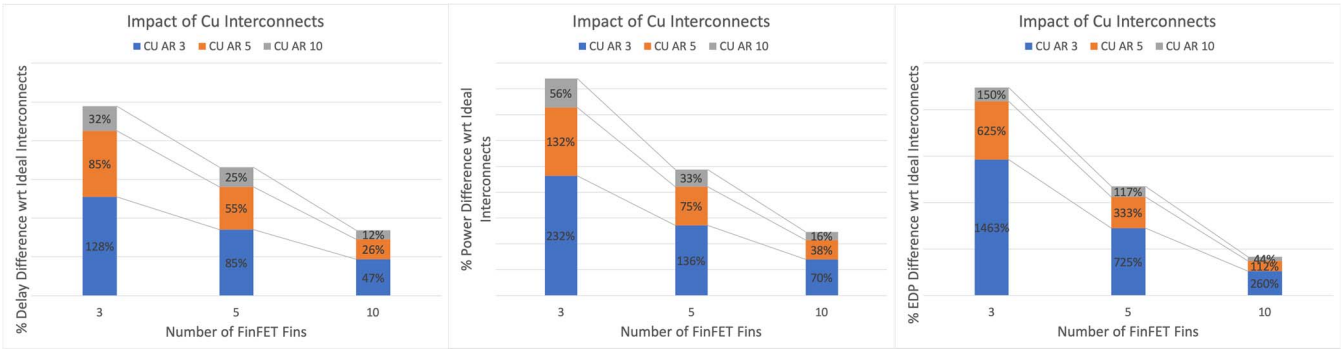


Fig. 2. Impacts of Cu interconnects on circuit-level overall delay, power and EDP for different interconnect aspect ratios and FinFET devices with number of fins for 3, 5, and 10.

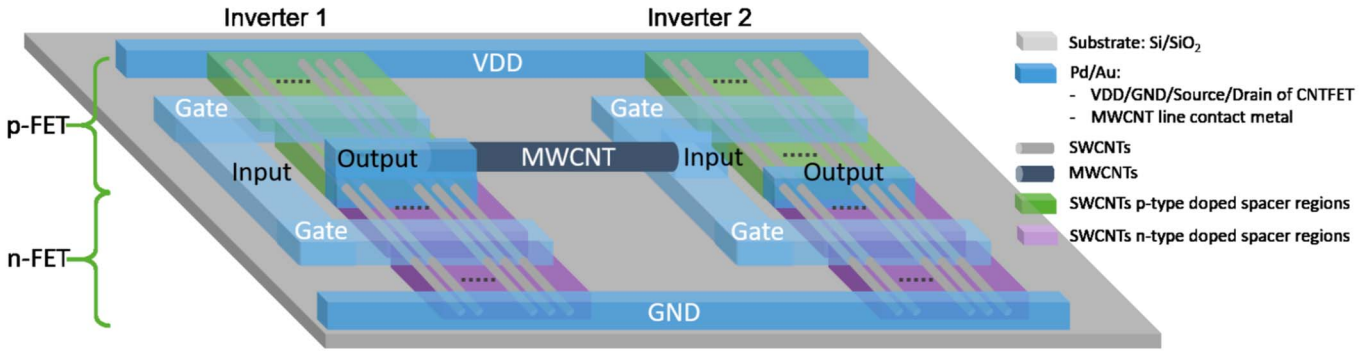
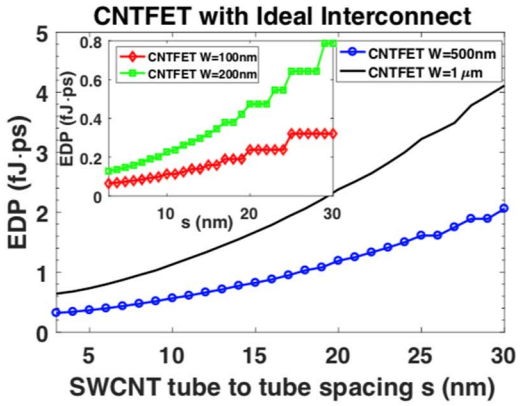
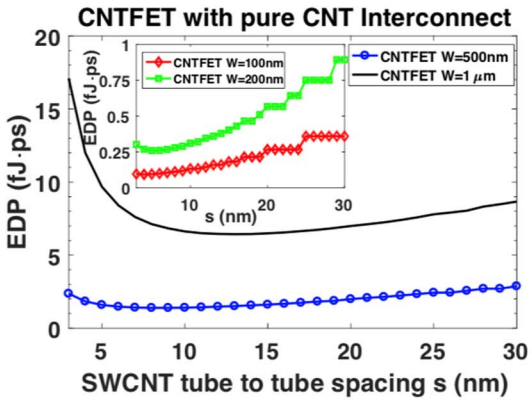


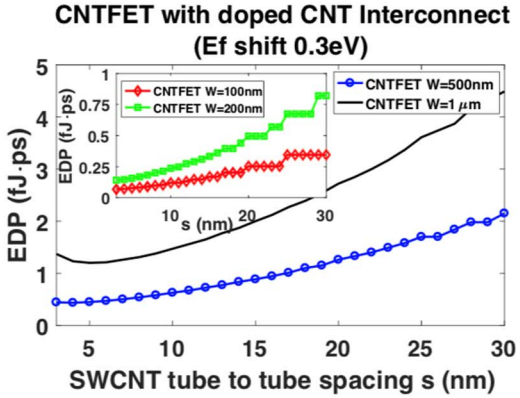
Fig. 3. Illustration of carbon nanotube-based benchmark. Carbon nanotube field-effect transistors (CNTFETs) connected with multi-wall CNT (MWCNT) interconnects to create a ring oscillator benchmark.



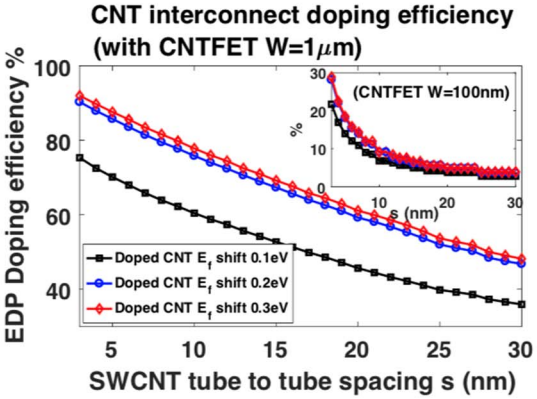
(a) EDP of CNTFET devices with ideal interconnects.



(b) EDP of CNTFET devices with pristine MWCNT interconnects.

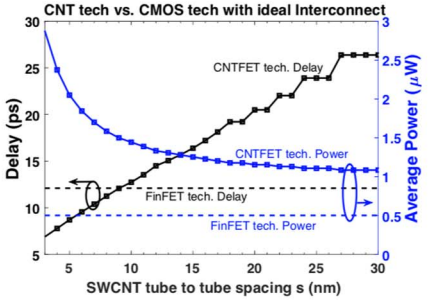


(c) EDP of CNTFET devices with doped MWCNT interconnects.

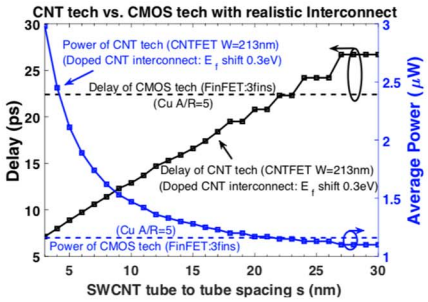


(d) EDP improvement with various MWCNT doping concentrations and CNTFET devices with $W = 1\mu m$ (and $W = 100$ nm for inset figure).

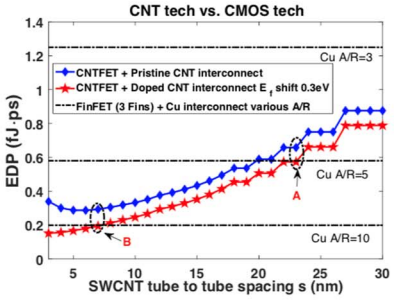
Fig. 4. (a)-(d) are resuls for CNT-based benchmark. (a) represents energy delay product (EDP) as varying CNTFET width (W) and tube-to-tube spacing (s) with ideal interconnects (no parasitics). (b) shows EDP variations when including pristine MWCNT interconnect between logic gates. (c) shows EDP variation with doped MWCNT interconnects (Ef shifts 0.3eV) under different W and s. (d) illustrates the overall EDP improvement by introducing different doping concentrations on MWCNT interconnects.



(a) Delay and power comparisons for CNT and advanced CMOS benchmarks with ideal interconnects.



(b) Delay and power comparisons for CNT and advanced CMOS benchmarks with real interconnects.



(c) EDP comparisons between CNT and advanced CMOS benchmarks with different interconnects.

Fig. 5. Cross (a)-(c) are simulation analysis to compare CNT and advanced CMOS technologies. (a) and (b) represent circuit delay and power consumption for devices (CNTFET and FinFET) with ideal and realistic (doped MWCNT and Cu) interconnects, respectively. (c) shows the energy delay product (EDP) for CNT and advanced CMOS technologies with different interconnect configurations. Pristine and heavily doped MWCNT interconnects are included for CNTFET devices; whereas for FinFET devices, Cu interconnects with various aspect ratio (A/R) are considered.