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A Novel Low-Cost TMR-Without-Voter Based HIS-Insensitive and MNU-Tolerant Latch Design for Space Applications

Aibin Yan, Zhelong Xu, Kang Yang, Jie Cui, Zhengfeng Huang, Patrick Girard, *Fellow, IEEE*, Xiaoqing Wen, *Fellow, IEEE*

Abstract—**With the CMOS technology scaling down, radiation induced multiple-node-upsets (MNUs) that include double-node-upsets and triple-node-upsets (TNUs) are becoming more and more an issue in storage cells used for applications constrained by their environment, such as aerospace applications confronted to radiations. This paper presents a novel triple-modular-redundancy (TMR)-without-voter based high-impedance-state (HIS)-insensitive and MNU-tolerant latch design, namely TMHIMNT, to ensure both high reliability and low cost. The TMHIMNT latch mainly comprises triple clock-gating based dual-interlocked-storage-cells (DICEs) and four inverters. Through three internal inverters, the values stored in DICEs converge to a common node feeding an output-level inverter, enabling the TMHIMNT latch to tolerate any possible MNU. Simulation results demonstrate the MNU tolerance of the proposed TMHIMNT latch. Due to the disuse of C-elements, the proposed TMHIMNT latch is insensitive to the HIS, making the latch more reliable for aerospace applications. Moreover, compared with the**

state-of-the-art TNU hardened latch (TNUHL), due to the use of a high-speed path, clock-gating technologies, and fewer transistors, the proposed TMHIMNT latch can achieve 98% delay, 17% power, and 29% area reductions, respectively.

Index Terms—**Radiation hardening, latch design, multiple-node-upset, high-impedance-state**

I. INTRODUCTION

With the rapid advancement of CMOS technologies, modern integrated circuits are becoming increasingly vulnerable to reliability issues caused by soft errors. Soft errors are transient errors that are mainly caused by the striking of neutrons, protons, heavy ions, alpha particles, electrons, and so on [1-2]. In nano-scale CMOS technologies, a striking particle can invalidly change the logic state of a single node in a storage cell, resulting in a *single event upset* (*SEU*), i.e., a *single node upset* (*SNU*). However, in highly-integrated nano-scale CMOS technologies, due to charge sharing, a high-energy striking-particle can simultaneously change the logic states of double or even triple adjacent nodes, resulting in a *multiple-node-upset* (*MNU*) that includes *double-node-upset* (*DNU*) and *triple-node-upset* (*TNU*) [3-5]. It is obvious that radiation hardening only targeting SNUs is no longer sufficient for safety-critical aerospace applications that require high reliability. Therefore, it is crucial to design integrated circuits that are MNU tolerant to achieve high reliability.

Using the *radiation-hardening-by-design* (*RHBD*) approach, many hardened storage cells have been proposed [3-22]. Among these cells, some are hardened for *static ran-*

dom access memories (*SRAMs*) [6-8], some are hardened for flip-flops [9-10], and all the others are hardened for latches. Among these hardened latches, many designs mainly target SNUs [11-15]. Using techniques such as *dual-modular redundancy* (*DMR*) and *triple-modular redundancy* (*TMR*), these designs can robustly retain values protected against SNUs. However, the fine-featured and highly-integrated devices in advanced nano-scale technologies can allow a single-event charge to simultaneously affect multiple nodes and cause an MNU. To tolerate MNUs for latches in safety-critical aerospace applications, an efficient way is still to employ the RHBD technique using spatial redundancies such as multiple-modular redundancy and *double-level error-interception* (*DLEI*) as in [3-5, 16-22]. However, these state-of-the-art latches still suffer from some problems such as: (1) they cannot provide complete TNU tolerance [11-21] since there is at least one counterexample that the latch will output an invalid value if triple nodes suffer from a TNU; (2) a TMR-voter, delay element, and/or redundant devices have to be used for some latches, leading to large overhead in terms of transmission delay, power dissipation, and silicon area; and (3) they are sensitive to the *high-impedance state* (*HIS*) due to the use of a *C-element* (*CE*) as a voter [3-5, 12, 22]. Although a keeper connected to the output of the CE can avoid sensitivities to the HIS, it leads to extra overhead.

In this paper, based on the TMR-without-voter technique, a novel low-cost HIS-insensitive and MNU-tolerant latch design, namely TMHIMNT, is proposed. The latch mainly comprises triple *clock-gating* (*CG*) based *Dual-Interlocked-storage-Cells* (*DICEs*) [23] and four inverters. Through three internal inverters, the values kept in these SNU-self-recoverable DICEs converge to the input of an output-level inverter and the

input cannot retain a completely flipped value, enabling the latch to tolerate any possible SNU, DNU, and TNU. Simulation results demonstrate the complete node-upset tolerance of the proposed TMHIMNT latch. Due to the use of a high-speed path, CG technologies, and fewer transistors, the proposed TMHIMNT latch is low-cost especially in terms of power dissipation and silicon area, compared with the state-of-the-art TNU tolerant latches. Moreover, the proposed latch does not use C-elements, thus it is insensitive to the HIS, making the latch more reliable for aerospace applications that require both high reliability and cost-effectiveness.

The contribution of this paper can be summarized as follows. (1) The TMR-without-voter technique is firstly proposed to reduce overhead. (2) Based on the TMR-without-voter technique, using triple DICEs and four inverters, a novel TNU-tolerant latch design is proposed, featuring low cost compared with the state-of-the-art MNU-tolerant latches. (3) Without using CEs, the proposed latch is insensitive to the HIS, leading to very high reliability.

The rest of the paper is organized as follows. Section II reviews typical SNU, DNU, and/or TNU hardened latch designs. Section III describes the implementation, normal working principles, and fault toleration verifications for the proposed latch design. Section IV provides the comparison and evaluation results for overheads. Section V concludes the paper.

II. TYPICAL LATCH DESIGNS

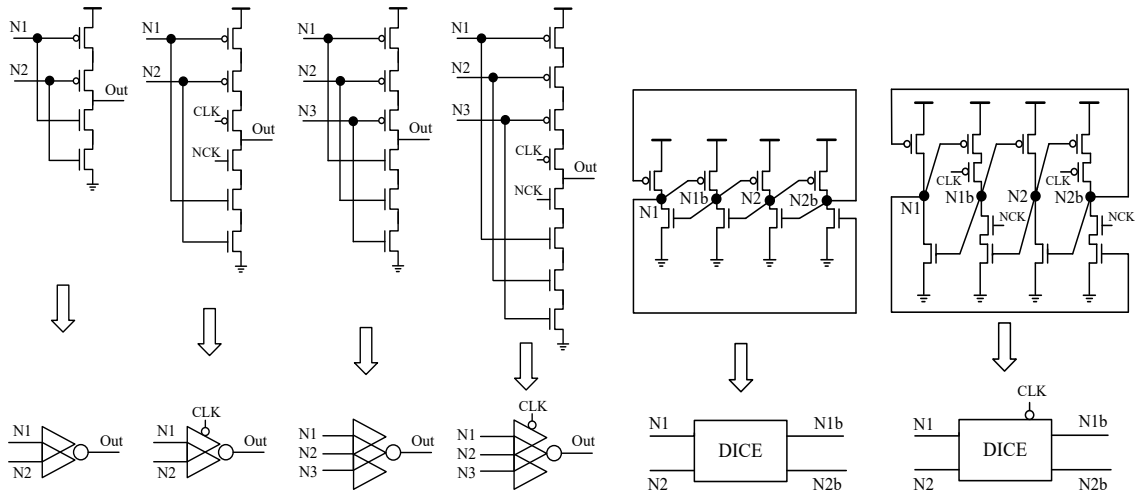
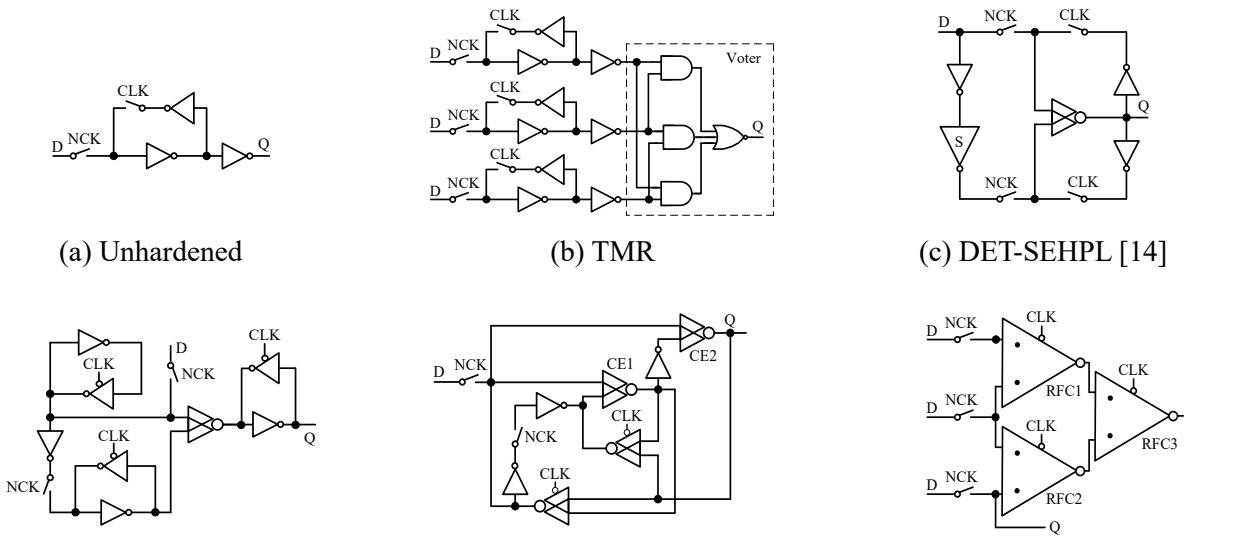


Fig. 1. Schematics of the widely used components in typical radiation-hardened latch designs. (a) 2-input C-element. (b) Clock-gating based 2-input C-element. (c) 3-input C-element. (d) Clock-gating based 3-input C-element. (e) Dual-interlocked-storage-cell (DICE). (f) Clock-gating based DICE.

In typical radiation-hardened latch designs, CEs and DICEs are extensively used. Fig. 1 shows the schematics of these widely used components. Fig. 1-(a) and (c) show the 2-input and 3-input CEs and it is easy to create a 4-input one. A CE behaves as an inverter if all its inputs have the same value and its output can retain the previous correct value for a period of time if its inputs become different. However, if its inputs become different for an extended period of time, its output will float to an undetermined value, i.e., it enters into the HIS. Fig. 1-(b) and (d) show the CG-based CEs that are controllable by the *system clock* (*CLK*) and the *negative system clock* (*NCK*) signals. Fig. 1-(e) shows the DICE. A DICE can self-recover from any possible SNU [23]; however, it cannot provide self-recoverability from partial DNUs in the worst case. Fig. 1-(f) shows

the CG-based DICE. Fig. 2 shows the schematics of typical latch designs, where the switches are *transmission gates* (*TGs*). For clock-signal connections to a TG, we take the left TG next to input D in Fig. 2-(a) as an example. Since it is marked with NCK, the gate terminal of the PMOS transistor is connected to NCK and the gate terminal of the NMOS transistor is connected to CLK. This rule is applicable to all latches in this paper.



(a) Unhardened (b) TMR (c) DET-SEHPL [14]

(d) LSEH [15] (e) HRUT [16] (f) DNURL [17]

(g) THLTCH [18] (h) DICE4TNU [5] (i) TNUHL [3]

Fig. 2. Schematics of typical latch designs.

Fig.2-(a) shows the unhardened latch. It simply uses two inverters to create a feed-back loop to keep values and thus it cannot effectively tolerate SNUs. Moreover, it is insensitive to the HIS as it does not use C-elements. Fig.2-(b) shows the TMR latch. It

employs triple unhardened latches with a voter to tolerate SNUs only. The voter consists of three 2-input AND gates and one 3-input OR gate, totally leading to 18 transistors; however, the unhardened latch has 10 transistors only. This motivates us to propose a novel TMR-without-voter technique to reduce overhead. Fig.2-(c) shows the DET-SEHPL latch [14]. The latch uses a delay element marked with S to make the inputs of the CE in the latch have different delays from D, thus possibly masking a transient error at single-inputs of the CE. However, the latch cannot tolerate SNUs, especially for Q, since an SNU at Q can feed back to the inputs of the CE, leading to a retained invalid value. Fig.2-(d) shows the LSEH latch [15]. Based on the DMR, the latch mainly uses two unhardened latches feeding a CE to tolerate SNUs. Since the inputs of the CE have different delays from D, the CE can mask a transient error in single-inputs of the CE. The keeper connected to the output of the CE can avoid sensitivities to the HIS. However, it cannot tolerate MNUs. Fig.2-(e) shows the HRUT latch [16]. Similarly, since the inputs of CE1/CE2 have different delays from D, the CEs can mask transient errors. Moreover, the latch feeds back Q to its internal nodes to tolerate SNUs. However, it cannot tolerate MNUs.

Fig.2-(f) shows the DNURL latch [17]. The latch uses triple interlocked SNU-self-recoverable RFC cells [13] to achieve complete DNU-self-recoverability. However, it cannot effectively tolerate TNUs. Fig.2-(g) shows the THLTCH latch [18]. The latch employs a delay element marked with τ to create delay-differential of CE-inputs to mask transient errors in some CE-single-inputs and uses nine interlocked CEs to tolerate DNUs. However, it cannot effectively tolerate TNUs. Fig.2-(h) shows the DICE4TNU latch [5]. The latch uses four interlocked DICEs feeding a 4-input CE to tolerate TNUs.

However, it is sensitive to the HIS. This is because any DICE cannot self-recover from a DNU in the worst case, which can make the inputs of the C-element different for an extended period of time. Fig.2-(i) shows the TNUHL latch [3]. The latch uses five inter-locked 4-input CEs to create feedback loops to retain values. Based on the DLEI, the loops feed two 3-input CEs that feed one 2-input CE to tolerate TNUs. However, it is also sensitive to the HIS and has a very large area. This motivates us to propose a novel HIS-insensitive TNU-tolerant latch with low-cost that will be introduced in the next section.

III. PROPOSED TMHIMNT LATCH DESIGN

A. Latch Schematic and Working Principles

Based on the TMR-without-voter technique, Fig. 3 shows the schematic of the proposed novel low-cost HIS-insensitive and MNU-tolerant latch design, namely TMHIMNT. The latch comprises triple clock-gating based SNU-self-recoverable DICEs (DICE1, DICE2, and DICE3) to store values, three inverters (Inv1, Inv2, and Inv3) to make DICEs converge to a common node (this is our proposed TMR-without-voter technique), a CG-based output-level inverter (Inv4) to output the stored values, and seven TGs to initialize the values of nodes. N1 through N6, N1b through N6b, and Qb are the internal nodes. D, Q, CLK, and NCK are the input, output, system clock signal, and negative system clock signal, respectively.

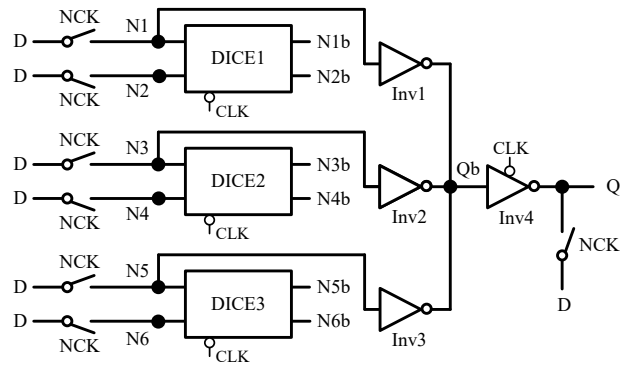


Fig. 3. Proposed TMHIMNT latch design.

When CLK is high and NCK is low, the latch works in transparent mode. In this mode, the transistors in TGs are ON. Thus, N1 through N6 and Q have the same value from D, and Qb can be determined by N1, N3, and N5 through Inv1, Inv2, and Inv3. To reduce power dissipation, CG techniques are used in DICEs to avoid the formation of feedback loops so as to reduce current competition. Thus, N1b through N6b have no values and cannot feed N1 through N6. Note that, Q cannot be determined by Qb through Inv4, since the output of Inv4 is blocked through CG techniques. In other words, to reduce delay, Q can only be determined by D through a TG. In summary, the proposed latch can be properly initialized, and Q can receive the values from D.

When CLK is low and NCK is high, the latch works in hold mode. In this mode, the transistors in TGs are OFF, and the clock-controlled transistors in DICEs and Inv4 are ON. Thus, the values of N1 through N6 can feed N1b through N6b, and the values of N1b through N6b can feed N1 through N6, forming many feedback loops to retain correct values in DICEs. The stored values in DICEs can feed Qb through Inv1, Inv2, and Inv3, and the value of Qb can feed Q through Inv4. Thus, the stored values in the latch

can output to Q. In summary, the proposed latch can properly store values, and can output stored values through Q.

Here, the SNU, DNU, and TNU tolerance principles in hold mode of the proposed latch are introduced. For SNUs, since DICE1, DICE2, and DICE3 are SNU-self-recoverable [23], it is obvious that, N1 through N6, and N1b through N6b can self-recover from SNUs, respectively. When Qb or Q suffers from an SNU, since the stored values in DICEs are correct, the value of Qb can be refreshed through Inv1, Inv2, and Inv3, and eventually Q is still correct. In summary, the proposed latch is SNU-tolerant. For DNUs, since any node-pair can be affected by a DNU, there are totally four indicative cases described in the following.

Case D1: Only one DICE is affected by a DNU. In this case, the DICEs are equivalent for DNU tolerance. Thus, only one DICE needs to be considered. Here, we only consider DICE1 for illustration. Let λ denote the node-distance of two adjacent nodes in a DICE. Since the nodes in a DICE are symmetrically constructed as shown in Fig. 1, possible node-distances in a DICE are only λ and 2λ. Thus, the representative node-pairs are only <N1,N1b> and <N1,N2> of DICE1. Their node-distances are λ and 2λ, respectively, and all other node-pairs in DICE1 are equivalent to the above pairs. Through an extensive investigation, it can be found that DICEs can partially self-recover from a DNU. For example, node-pair <N1,N1b> as shown in Fig. 1-(e)/(f) can self-recover from a DNU when N1 = 1, but cannot self-recover from a DNU when N1 = 0.

Let us consider the case where <N1,N1b> of the latch is affected by a DNU. If N1 = 1, <N1,N1b> can self-recover from the DNU. Then, the values kept in DICE1 will still

be correct. Therefore, the values of all nodes in the latch can still be correct. In other words, the latch can tolerate this DNU if N1 = 1. If N1 = 0, <N1,N1b> cannot self-recover from the DNU. Thus, the values kept in DICE1 will be totally wrong and a wrong value will feed Qb through Inv1. Moreover, the values kept in DICE2 and DICE3 are correct and a correct value will feed Qb through Inv2 and Inv3, respectively. Thus, this will lead to an undetermined value (but not the HIS) for Qb. However, the value of Qb will be eventually close to the correct value due to current competition. Therefore, this value will be strengthened/reversed to be a correct value through Inv4, resulting in the output of a correct value on Q. In other words, the latch can still tolerate this DNU if N1 = 0. Therefore, the latch can tolerate the DNU at node-pair <N1,N1b>. Similarly, in the case where <N1,N2> of the latch is affected by a DNU, the latch can still tolerate the DNU. Therefore, the latch can tolerate DNUs for Case D1.

Case D2: Two DICEs are simultaneously affected by a DNU. Obvisouly, the representative node-pair is only <N1,N3>. **Case D3**: One DICE along with Qb or Q are affected by a DNU. Obviously, the representative node-pairs are <N1,Qb> and <N1,Q>. **Case D4**: No DICE is affected by a DNU. Obviously, the representative node-pair is only <Qb,Q>. In these cases, since DICEs are SNU-self-recoverable, all values kept in DICEs will be eventually correct. Then, the error (if any) at Qb can be firstly removed by DICEs through inverters and Q can be its original correct value. In other words, the values of all nodes in the latch can still be correct. Therefore, the latch can tolerate DNUs for Cases D2, D3, and D4. Through the above discussions, it can be found that the latch is DNU-tolerant. For TNUs, since any triple-node can be affected by a TNU, there are totally six indicative cases described in the following.

Case T1: Two nodes in one DICE along with Qb or Q are affected by a TNU. This case is similar to Case D1, but Qb or Q is also affected. Similarly, we only need to consider DICE1 for illustration. Therefore, the representative triple-nodes are only <N1,N1b,Qb>, <N1,N2,Qb>, <N1,N1b,Q>, and <N1,N2,Q>.

Let us consider the case where <N1,N1b,Qb> of the latch is affected by a TNU. If N1 = 1, <N1,N1b> can self-recover. Then, the values kept in DICE1 will still be correct. Thus, the error at Qb will be removed by DICEs through inverters, and the values of all nodes in the latch will still be correct. In other words, the latch can tolerate this TNU if N1 = 1. If N1 = 0, <N1,N1b> cannot self-recover. Thus, the values kept in DICE1 will be totally wrong and a wrong value will feed Qb through Inv1. However, the values kept in DICE2 and DICE3 are correct and a correct value will feed Qb through Inv2 and Inv3, respectively. Thus, this will lead to an undetermined value (but not the HIS) for Qb.

It is obvious that at the point when Qb is also affected due to the TNU, there will be four values converging to Qb, i.e., the first is the wrong value outputting through Inv1, the second is the wrong value coming from the direct particle-striking of the TNU, the third and the fourth are the correct values outputting through Inv2 and Inv3. However, the second wrong value coming from the direct particle-striking of the TNU will not be kept for an extended period of time. This means that, as time passes, the value of Qb will still be jointly determined through Inv1, Inv2, and Inv3, and eventually Qb is still close to the correct value due to current competition. Therefore, this value will be strengthened/reversed to be a correct value through Inv4, resulting in the output of a correct value on Q. In other words, the latch can still tolerate this TNU if N1 = 0. There-

fore, the latch can tolerate the TNU at triple-node <N1,N1b,Qb>. Similarly, in the case where <N1,N2,Qb> of the latch is affected by a TNU, the latch can still tolerate this TNU.

Let us consider the case where <N1,N1b,Q> or <N1,N2,Q> of the latch is affected by a TNU. As described in Case D1, the value of Qb will be correct or eventually close to the correct value due to current competition, making Inv4 output a correct value on Q. Therefore, the error at Q will be removed by Qb, making the latch output a correct value. In other words, the latch can tolerate this TNU. Therefore, the latch can tolerate TNUs for Case T1.

Case T2: Triple nodes in one DICE are affected by a TNU. We still consider DICE1 for illustration. Obviously, all nodes in DICE1 will be flipped, and the representative triple-node is only <N1,N1b,N2>. However, similarly to Case T1, the value of Qb will be eventually close to the correct value due to current competition. Thus, this value will be strengthened/reversed to be a correct value through Inv4, resulting in the output of a correct value on Q, i.e., the latch can tolerate the TNU. Therefore, the latch can tolerate TNUs for Case T2.

Case T3: Double nodes in one DICE and one node in another DICE are simultaneously affected by a TNU. Obviously, the representative triple-nodes are <N1,N1b,N3> and <N1,N2,N3>. Since one node in another DICE can self-recover, the TNU can downgrade to a DNU. As discussed in Case D1, the latch can tolerate DNUs at <N1,N1b> and <N1,N2>. In other words, the latch can tolerate the TNU. Therefore, the latch can tolerate TNUs for Case T3.

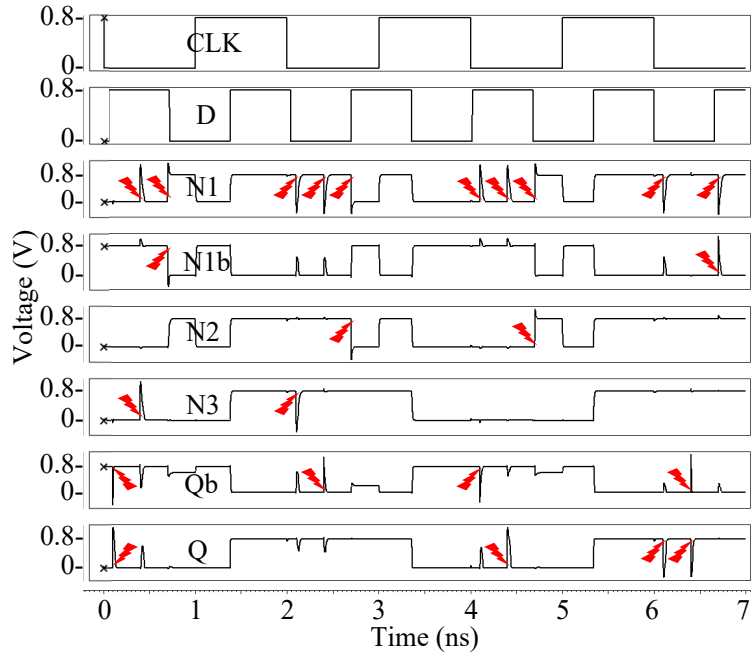


Fig. 4. Simulation results of the key SNU and DNU injections for the proposed TMHIMNT latch design.

Case T4: One node in every DICE is simultaneously affected by a TNU. Obvious, the representative triple-node is only <N1,N3,N5>. **Case T5**: One node in one DICE along with Qb and Q are simultaneously affected by a TNU. Obviously, the representative triple-node is only <N1,Qb,Q>. **Case T6**: Single nodes in two DICEs along with Qb or Q are simultaneously affected by a TNU. Obviously, the representative triple-nodes are only <N1,N3,Qb> and <N1,N3,Q>. In these cases, since DICEs are SNU-self-recoverable, all values kept in DICEs will be eventually correct. Then, the error (if any) at Qb can be firstly removed by DICEs through inverters and Q can be its original correct value. In other words, the values of all nodes in the latch can still be correct. Therefore, the latch can tolerate TNUs for Cases T4, T5, and T6. Clearly, the above dis-

cussions validate that the latch is SNU, DNU, and TNU tolerant. Moreover, the latch does not use C-elements to avoid the HIS-sensitivities, making the latch more reliable for aerospace applications.

B. Simulation Results

The TMHIMNT latch was implemented in the 22 nm CMOS technology and extensive simulations using Synopsys HSPICE were performed. The simulation parameters were described, i.e., the supply voltage was set to 0.8V, the working temperature was set to the room temperature, the PMOS transistors had the ratio W/L = 90/22nm, and the NMOS transistors had the ratio W/L = 45/22nm. Note that, the lighting marks in Figs. 4, 5, and 6 denote the injected node-upset-errors.

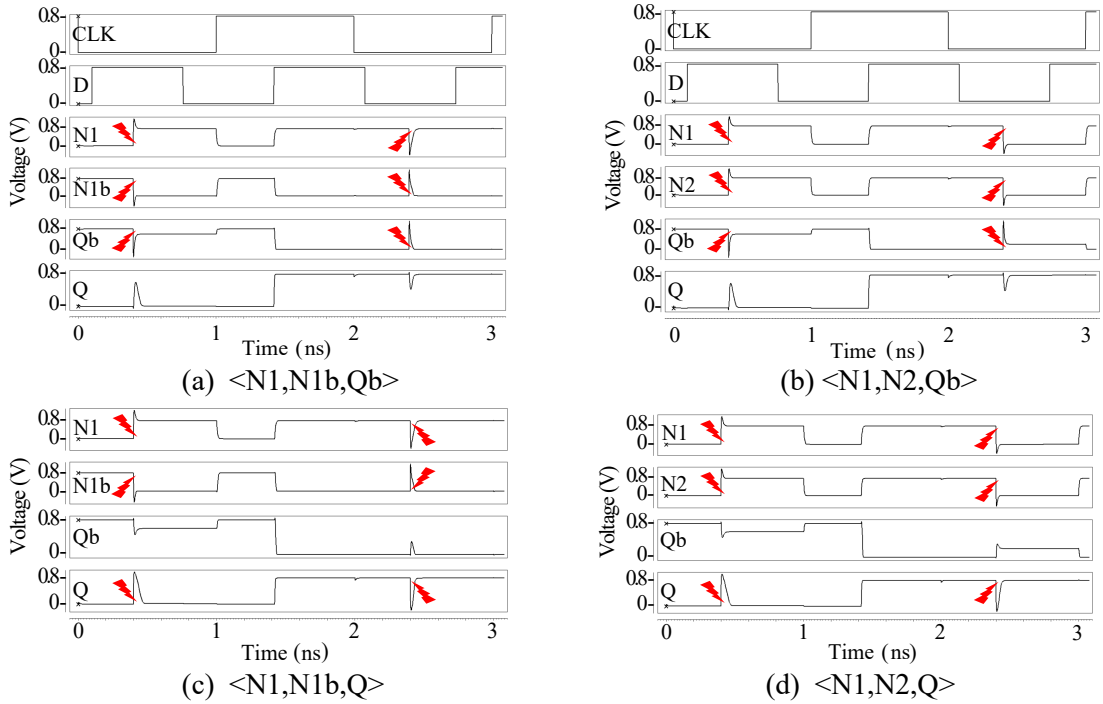


Fig. 5. Simulation results of the key TNU injections for Case T1 of the proposed TMHIMNT latch design.

Fig. 4 shows simulation results of the key DNU injections for the proposed latch. SNU injections are simple but omitted for the brevity of the paper. In Fig. 4, during 0ns to 1ns and during 4ns to 5ns, when Q = 0, a DNU was injected to key node-pairs <Qb,Q>, <N1,N3>, <N1,N1b>, <N1,Qb>, <N1,Q>, <N1,N2>, respectively. During 2ns to 3ns and during 6ns to 7ns, when Q = 1, a DNU was injected to the same key node-pairs <N1,N3>, <N1,Qb>, <N1,N2>, <N1,Q>, <Qb,Q>, <N1,N1b>, respectively. It can be seen that, the latch can tolerate or even self-recover from these DNUs. In summary, the latch can tolerate or even self-recover from DNUs.

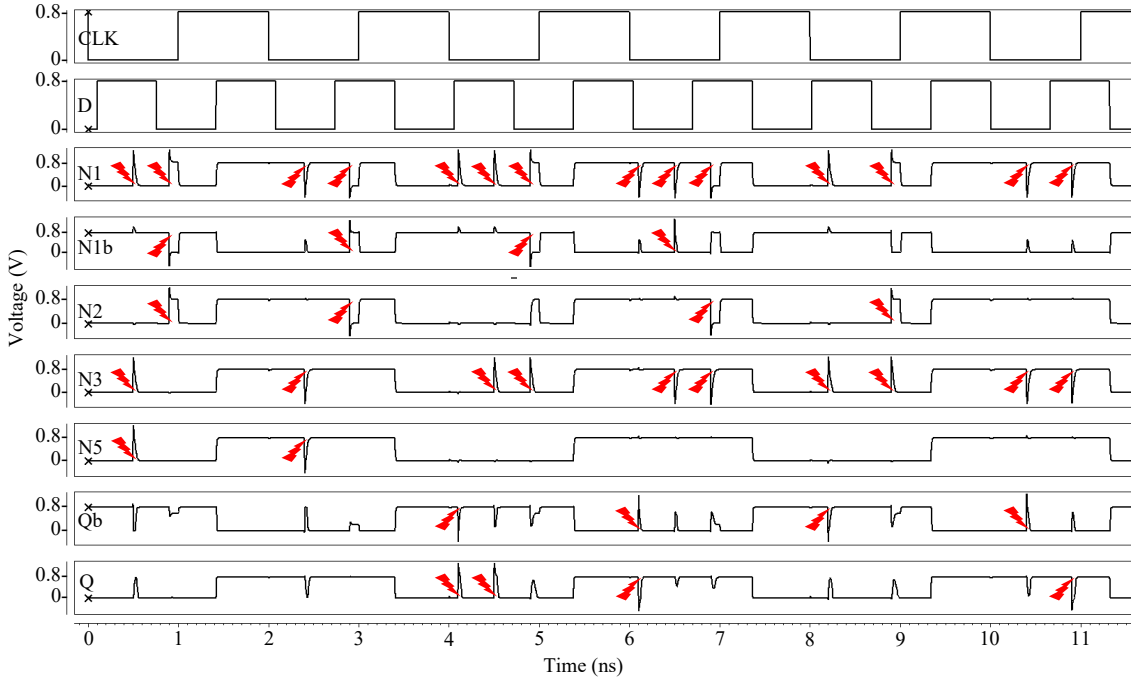


Fig. 6. Simulation results of the other key TNU injections for the proposed TMHIMNT latch design.

Fig. 5 shows simulation results of the key TNU injections for Case T1 of the proposed latch. In Fig. 5-(a), during 0ns to 1ns, when Q = 0, a TNU was injected to key

triple-node <N1,N1b,Qb>. It can be seen that, the wrong value of Qb coming from the direct particle-striking of the TNU cannot be kept for an extended period of time. As time passes, the value of Qb was still close to its correct value. Therefore, Q was eventually still correct. Moreover, during 2ns to 3ns, when Q = 1, a TNU was injected to the same key triple-node. It can be seen that the latch can self-recover from this TNU. In other words, the latch can tolerate the TNU at <N1,N1b,Qb>. Similarly, it can be seen from Fig. 5-(b), (c), and (d) that the latch can tolerate the TNU at <N1,N2,Qb>, <N1,N1b,Q>, and <N1,N2,Q>, respectively. Note that, the signals of CLK and D in Fig. 5-(c) and (d) are the same as those in Fig. 5-(a) and (b), but they are omitted for the brevity of the paper.

Fig. 6 shows simulation results of the other key TNU injections for the proposed latch. In Fig. 6, during 0ns to 1ns, 4ns to 5ns, and 8ns to 9ns, when Q = 0, a TNU was injected to key nodes <N1,N3,N5>, <N1,N1b,N2>, <N1,Qb,Q>, <N1,N3,Q>, <N1,N1b,N3>, <N1,N3,Qb>, and <N1,N2,N3>, respectively. During 2ns to 3ns, 6ns to 7ns, and 10ns to 11ns, when Q = 1, a TNU was injected to the same key nodes, i.e., <N1,N3,N5>, <N1,N1b,N2>, <N1,Qb,Q>, <N1,N1b,N3>, <N1,N2,N3>, <N1,N3,Qb>, and <N1,N3,Q>, respectively. It can be seen that, the latch can tolerate or even self-recover from these TNUs. In summary, the latch can tolerate or even self-recover from these TNUs.

As described above, simulation results have demonstrated the DNU and TNU tolerance of the proposed TMHIMNT latch. In these simulations, we used a controllable double-exponential current source model to perform all kinds of node-upset injections as in [25] to simulate striking-particles. The time constants of the rise and fall periods of

the injected current pulses were set to 0.1 and 3 ps, respectively.

IV. COMPARISONS AND EVALUATIONS

To make fair comparisons, the typical latch designs reviewed in Section II were also implemented with the same parameters listed in Section III.B. Detailed reliability and overhead comparison results are shown in Table I, with respect to SNU, DNU, and/or TNU tolerance, HIS insensitivity, overhead about D to Q delay (i.e., the average of rise and fall delays from D to Q), average power dissipation (dynamic and static), and silicon area (measured with the same method as in [4]).

TABLE I
RELIABILITY AND OVERHEAD COMPARISONS AMONG THE SNU, DNU, AND/OR TNU UNHARDENED/HARDENED LATCHES

No.	Latch	Ref.	SNU Tolerant	DNU Tolerant	TNU Tolerant	HIS Insensitive	Delay (ps)	10^{-4}×Area (nm^2)	Power (μW)
1	Unhardened	-	×	×	×	√	12.36	1.49	0.37
2	TMR	-	√	×	×	√	35.79	4.46	1.52
3	DET-SEHPL	[14]	×	×	×	√	46.90	3.56	0.64
4	LSEH	[15]	√	×	×	√	61.23	4.16	1.20
5	HRUT	[16]	√	×	×	√	70.40	6.24	0.54
6	DNURL	[17]	√	√	×	√	3.12	9.80	1.18
7	THLTCH	[18]	√	√	×	√	12.38	9.50	1.58
8	DICE4TNU	[5]	√	√	√	×	1.63	9.21	2.20
9	TNUHL	[3]	√	√	√	×	95.79	12.47	1.46
10	TMHIMNT	Proposed	√	√	√	√	1.63	8.91	1.21

For reliability comparisons, it can be seen from Table I that, the unhardened latch cannot effectively tolerate SNUs, let alone MNUs that include DNUs and TNUs. However, it is insensitive to the HIS since it does not use C-elements. The TMR latch cannot tolerate MNUs since it cannot output correct values if the multiple modules to be voted

have kept errors. Similarly, the latch is insensitive to the HIS. The DET-SEHPL latch cannot tolerate SNUs, let alone MNUs, since its output can be easily flipped by an SNU causing an invalidly retained value. Moreover, although it uses a C-element, it is insensitive to the HIS since the inputs of the C-element cannot be different for an extended period of time due to the special feedback loops in the latch. The LSEH latch cannot tolerate MNUs since it cannot output correct values if the C-element-voted double modules have kept errors. Moreover, it is insensitive to the HIS due to the use of a keeper connecting to its output. The HRUT latch cannot tolerate MNUs since it cannot output correct values when an input-and-output node-pair of its C-element is affected. Moreover, it is insensitive to the HIS since the inputs of any C-element cannot be different for an extended period of time.

The DNURL latch cannot tolerate TNUs since the three common nodes among RFCs can be flipped, causing invalidly retained values. Similarly, it is also insensitive to the HIS. The THLTCH latch has the same features compared with the DNURL latch. The DICE4TNU latch can tolerate MNUs. However, it is sensitive to the HIS since the inputs of its C-element can be different for an extended period of time especially when a TNU affects a DICE. The TNUHL latch has the same features as the DICE4TNU latch. The proposed TMHIMNT latch can tolerate MNUs, and it is insensitive to the HIS since it does not use C-elements. Therefore, the proposed TMHIMNT latch is more reliable than all the above compared MNU-tolerant latches.

For overhead comparisons, we first discuss the delay. ***(Delay Comparisons)*** It can be seen from Table I that, the DNURL and DICE4TNU latches as well as the proposed TMHIMNT latch have a small delay since any of them uses a high-speed path, i.e., only

a transmission gate connecting D and Q is used to reduce D to Q delay in transparent mode. The reason why the DICE4TNU latch and the proposed TMHIMNT latch have the smallest delay is that they have to load fewer transistors when working in transparent mode. The TNUHL latch has the largest delay mainly due to the use of many transistors from D to Q. Next, we discuss the area. **(*Area Comparisons*)** It can be seen from Table I that, the unhardened latch has the smallest area, since it has the smallest amount of transistors. The TNUHL latch has the largest area, mainly due to the use of many transistors. The 2nd to 5th latches in Table I have a smaller area since they are mainly hardened to be robust against SNUs. The other hardened latches have a larger area since they are mainly hardened to be robust against MNUs. Generally, an MNU tolerant latch has to introduce a larger area. However, due to the use of fewer transistors, the area of the proposed TMHIMNT latch is the smallest compared with the other MNU-tolerant latches, which demonstrates the low-cost area overhead of the proposed latch. Finally, we discuss the power. **(*Power Comparisons*)** It can be seen from Table I that, the unhardened latch has the lowest power dissipation, since it has the smallest amount of transistors and there is no active feedback loop in transparent mode. The DET-SEHPL and HRUT latches have smaller power dissipation mainly due to their smaller area and/or used clock-gating technologies. The DICE4TNU latch has the largest power dissipation, since too many feedback loops can be constructed even in transparent mode, leading to too much current competition and power dissipation. The THLTCH and TNUHL latches have larger power dissipation mainly due to their larger area. Generally, a latch that has a small area and/or uses clock-gating technologies to reduce current competition has lower power dissipation. Therefore, the proposed latch has low power

dissipation compared with the MNU-tolerant latches. In summary, the above discussions demonstrates that the proposed TMHIMNT latch is low-cost compared with the MNU-tolerant latches.

To make quantitative comparisons, the *percentages of reduced costs* (*PRCs*) of the proposed TMHIMNT latch compared with the latches in Table I can be calculated. For example, any delay-PRC for a compared latch can be calculated with "$100\%\times(Delay_{compared} - Delay_{proposed}) / Delay_{compared}$". Here, $Delay_{compared}$ denotes the delay of a compared latch and $Delay_{proposed}$ denotes the delay of a proposed latch. Therefore, power PRCs and area PRCs for compared latches can be calculated similarly. However, here we only discuss the PRCs for the TNU tolerant latches for the brevity of the paper.

For the delay, compared with the 8^{th} and 9^{th} TNU tolerant latches in Table I, the PRCs are 0.00% and 98.30%, respectively. Here 0.00% means that the proposed latch has an identical delay compared with the DICE4TNU latch. However, compared with the TNUHL latch, the proposed latch can reduce the delay by 98.30%. For the area, the PRCs are 3.26% and 28.55%, respectively. This means that, compared with the DICE4TNU and TNUHL latches, the proposed latch can reduce 3.26% and 28.55% area, respectively. For the power, the PRCs are 45.00% and 17.12%, respectively. This means that, compared with the DICE4TNU and TNUHL latches, the proposed latch can reduce 45.00% and 17.12% power, respectively. In summary, the above discussions demonstrate that the proposed TMHIMNT latch is low-cost compared with the TNU-tolerant latches.

V. CONCLUSIONS

In the advanced nano-scale CMOS technologies, aggressive shrinking of transistor feature sizes makes integrated circuits such as SRAMs, flip-flops, and latches more likely to experience MNUs that include DNUs and TNUs. Existing latches suffer from severe problems such as non-tolerance to MNUs, large overhead, and/or sensitivity to the HIS. In this paper, based on the proposed TMR-without-voter technique, a novel low-cost HIS-insensitive and MNU-tolerant latch design has been proposed. Through three inverters, the values kept in triple DICEs converge to a common node feeding an output-level inverter, so that the latch can tolerate MNUs. Using the TMR-without-voter technique, a high-speed transmission path, clock-gating technologies, and fewer transistors, the proposed latch is cost-effective. Simulation results have demonstrated the robustness and cost-effectiveness of the proposed latch. Moreover, unlike the state-of-the-art MNU-tolerant latches that use an output-level C-element as a voter, the proposed latch is insensitive to the HIS as it does not use C-elements, making the latch more reliable to be applied to aerospace applications.

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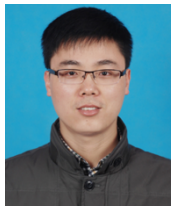

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