Design and Technology-level Optimization Challenges for Carbon Nanotube Circuits

Aida Todri-Sanial

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This talk aims to give an in-depth look into the process, growth, characterization, modeling, and simulation of carbon nanotube as the back-end of line material for both local and global on-chip interconnects. The talk is organized into two parts. The first part provides an in-depth overview of the process and growth of carbon nanotubes and their resistance measurements [1-2, 11-12]. In the second part, the talk is dedicated to investigating carbon nanotubes for digital logic cells such as interconnects for signal, power and ground interconnect material [7-10,18-22]. Due to the low-temperature growth, carbon nanotubes inherit a lot of defects that worsen its electrical resistance and ballistics transport. We investigate the doping of CNTs and show both experimental and simulations results of doped CNTs and their improved resistance [3-6, 13-15, 17]. We compare the performance, power and area metrics of digital logics cells with conventional copper and carbon nanotube interconnects (undoped and doped) to highlight the advantages and limitations of carbon nanotube BEOL interconnects. This talk gives an overview of our group research results achieved in the EU H2020 CONNECT project.

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2020 International Workshop on

Advanced Electronic Design Automation

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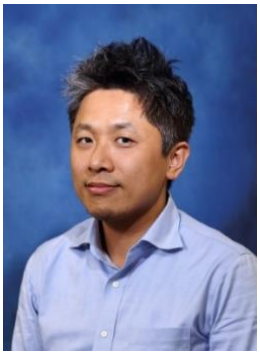
5. Speakers

	*Shaojun Wei* is the professor and PhD tutor at Tsinghua University, he is the head of Department of Microelectronics and Nanoelectronics and director of Institute of Microelectronics. He received a master's degree in engineering from the Department of Radio Electronics of Tsinghua University in 1984 and a Ph.D. in applied science from the Microelectronics Laboratory of Mons Institute of Technology in Belgium in 1991.He has won the second prize of National Science and Technology Progress Award; the second prize of National Technology Invention Award; the first prize of Technology Invention Award of the Ministry of Education; the first prize of Electronic Information Science and Technology Award of China Electronics Society. He is committed to the research of VLSI design methodology. The main research areas are: VLSI design methodology research, digital system high-level comprehensive technology research, embedded system design

	technology research and reconfigurable computing chip technology research. He has published more than 200 papers in the above fields, holds dozens of Chinese and American invention patents, published 3 monographs, and participated in the writing of many books. He is a member of the executive committee and TPC of many famous international conferences such as DAC, A-SSCC, HotChips, etc. He has been invited to give special lectures at famous international companies and international conferences.
	*Vazgen Sh. Melikyan* is professor at NPUA since 2001 and Director of Educational Department, Synopsys Armenia CJSC since 2004. He is Academician of Engineering Academy of RA and Corresponding Member of National Academy of Sciences of RA. He is also Honorary Professor of National Research University MIET since 2012 and European University. In 2016 Vazgen Melikyan has been awarded with Gold medal of the Ministry of Education and Science of Armenia for "the greatest contribution to the field of education and science", Gold Medal of Yerevan State University for significant contribution in the field of University Education and Science and the long-term fruitful cooperation with Yerevan State University, Gold Medal of the Russian-Armenian (Slavonic) University for many years of close cooperation, training highly qualified specialists in "Design and Technology of Electronic Means" specialization, Gold Medal of VivaCell-MTS for significant contribution in the field of Education and Science. He is the author of 11 monographs, more than 280 scientific and 135 methodical publications, had more than 150 reports in international conferences. 57 PhD dissertations have been realized and successfully defended under his supervision. His primary research interests include System level design and codesign, IP and platform based design, Electrical, logical and mixed-mode simulation and timing analysis, Power analysis and low power IC design, High speed IC design, Logic synthesis and circuit optimization, Signal integrity and design reliability analysis, Physical design and manufacturability.
	*Ricardo Reis* is a Professor at UFRGS since 1979. He is former member of the Microelectronics Committee of National Council for Scientific and Technological Development (CNPq). Former member of the Computer Science Committee of National Council for Scientific and Technological Development (CNPq), for two terms. He pulished more than 500 hundred papers in journals and conferences proceedings (like IEEE Design & Test, ACM TODAES, IEEE JSSC, ISCAS, SBCCI, PATMOS, VLSI-SoC, DAC, DATE, ICCD, CICC, ASP-DAC, LATW). He recevied many awards including Award as research of the year from the Fapergs, Silver Core award from IFIP, Research level 1A of the CNPq (Brazilian National

	Science Foundation). His primary research interests include Physical Design Automation and Methodologies, CAD tools, Circuits Tolerant to Radiation, VLSI Design Methodologies and Microelectronics Education.
	*Aida Todri-Sanial* received the B.S. degree in electrical engineering from Bradley University, IL in 2001, M.S. degree in electrical engineering from Long Beach State University, CA, in 2003 and a Ph.D. degree in electrical and computer engineering from the University of California Santa Barbara, in 2009. She received her French Habilitation (Habilitation a Diriger des Recherches) from the University of Montpellier in 2015. She obtained a post-graduate certificate in Entrepreneurship Programme for Women in Science, Technology and Engineering from the Judge Business School, University of Cambridge, UK in 2017. Her research interests focus on nanometer-scale issues in high-performance VLSI design with emphasis on power, thermal, signal integrity, and reliability issues as well as on circuits and systems for emerging technologies and nanomaterials. She has co-authored more than 100 publications on VLSI design area and emerging technologies.

	*Bei Yu* is currently an assistant professor in the Department of Computer Science and Engineering at the Chinese University of Hong Kong.He received a bachelor's degree in information and computer science from the University of Electronic Science and Technology of China in 2007 and a master's degree in computer science and technology from Tsinghua University in 2010,and a Ph.D. in electrical and computer engineering from the University of Texas in 2014.He has won the Best Paper Award from Integration, VLSI Journal in 2018, the Best Paper Award from ISPD in 2017, and the Best Paper Award from ICCAD in 2013.His current research interests include machine learning and deep learning and their applications in VLSI computer-aided design (CAD) and computer vision.He is the editor of the IEEE TC-CPS newsletter. He has also co-chaired the TPC of the ACM / IEEE CAD Machine Learning Symposium (MLCAD) 2019, the program committee for DAC, ICCAD, DATE, ASPDAC, ISPD.
	*Mohamed M. Sabry Aly* received the Ph.D. degree in electrical and computer engineering from the École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, in 2013.,He was a Post-doctoral Research Fellow with Stanford University, Stanford, CA, USA. He is currently an Assistant Professor with Nanyang Technological University, Singapore. He was a recipient of the Swiss National Science Foundation Early Post-doctoral Mobility Fellowship in 2013.His current research interests include the system-level design and optimization of computing systems enabled by emerging technologies. He was Technical Program committee member for ECRTS 2015,DATE 2015-2020,DAC 2017 and

	Technical Program committee track chair for ISLPED 2019,VLSIDS 2020.
	*Wenjian Yu* is now an associate professor at the school of computer science and technology, Tsinghua University. He received his B.S. and Ph.D. degrees in computer science and technology from Tsinghua University in 1999 and 2003 respectively. He has won the Lin Jiaqiao Applied Mathematics Award in 2001,the Microsoft Fellowship Award in 2002,the Tsinghua Excellent (Doctor) Graduate in 2003,the The 2nd Award of Natural Science Prize, Ministry of Education, China in 2006, the Excellent Young Scholar Award from the National Science Foundation of China in 2014, the Best Paper Award from the Design, Automation and Testing in Europe Conference in 2016. His research mainly focuses on physical modeling and simulation of integrated circuits, and a broad range of numerical algorithms, stochastic algorithms and their parallelization. He has authored/coauthored two books and over 150 papers in refereed journals and conferences.
	*Guojie Luo* is currently a long-term associate professor at Peking University's School of Information Science and Technology, and deputy director of the Energy-Efficient Computing and Application Center. He received a bachelor of science degree from the Department of Computer Science and Technology of Peking University in 2005, and a master and doctorate degree in computer science from the University of California, Los Angeles (UCLA) in 2008 and 2011, respectively. He has won the 2013 ACM/SIGDA Outstanding Doctoral Dissertation Award, the 2016 CCF-Intel Young Scholar Promotion Program Award, and the 2017 ASP-DAC Ten-Year Most Influential Thesis Award. His current research interests include electronic design automation, heterogeneous computing based on FPGAs and new devices, and medical image analysis algorithms. He has been a member of the technical committees of ICCAD 2014-2016, ISPD 2014-2016, ASP-DAC 2013-2015, NanoArch 2013-2014, and a reviewer of magazines such as IEEE TCAD, IEEE TVLSI, ACM TRETS, ACM JETC and so on.
	*Yibo Lin* is an assistant professor in the Department of Computer Science at Peking University. He recived the B.S. degree in Microelectronics from Shanghai Jiaotong University in 2013. Previously, he worked as a postdoctoral researcher at the University of Texas at Austin from 2018 to 2019. He recived the Ph.D. degree in Electrical and Computer Engineering from the University of Texas at Austin in 2018. His research interests include modeling and optimization of VLSI design automation, deep learning applications, emerging technology in VLSI CAD, hardware acceleration and hardware security. He is a recipient of the Best Paper Awards at DAC 2019, Integration, the VLSI Journal 2018, and SPIE Advanced Lithography Conference 2016. He has published 16 journal articles and 35 conference papers.

	*Carolina Metzler* is the Postdoc Fellow at UFRGS(Universidade Federal do Rio Grande do Sul) since 2014 and the Lead Application Engineer at Cadence since 2019. She recived the Computer Enginner Degree from PUCRS in 2009 and Ph.D degree in Microelectronic Systems recognized by the PGMicro from UFRGS in 2016. She is the IEEE Circuits and Systems Society member (Rio Grande do Sul Chapter). Her research interests focus on physical design, test and design for test, 3D integration and new technologies.
	*Yucheng Wang* is a 20+ year EDA veteran. He is not only the expert in static timing and statistical timing analysis, he also contributed broadly to the various aspects of Aprisa, including power analysis, clock tree synthesis and optimization and data base. Prior joining AtopTech, he was R&D manager with Avant! where he started the Astro project. Before that, he was the technical lead at Integrated Silicon System, he developed RC extraction, which became Star RC after merged with Avant!. He was a cofounder, VP of Timing Trchnology of AtopTech Inc. Dr Wang has 2 US patents related to EDA. He received BS and MS in Electrical Engineering from Fudan University, and PhD. In Electrical and Computer Engineering from Duke University. He is currently the CTO of Shenzhen Giga Design Automation.
	*Quan Chen* is currently an assistant professor. He obtained a PhD degree in electrical and electronic engineering from the University of Hong Kong in 2010. He was a postdoctoral fellow at the University of California, San Diego (UCSD) and a research assistant professor at the University of Hong Kong. He joined Southern University of Science and Technology in 2019 as an assistant professor at the Shenzhen-Hong Kong Microelectronics Institute. He was the winner of the Hong Kong Cyberport "Cyberport Incubation Program" and the winner of the University of Hong Kong Innovation and Technology Commission (ITC) "University Technology Entrepreneurship Support Program (TSSSU) in 2019. Dr. Chen's main research areas include ultra-large-scale circuit simulation and multiphysics analysis in the field of electronic design automation (EDA), and first-principles simulation of quantum mechanics of advanced nano-devices and materials, and he has many years of experience in technology transformation and commercialization.

	*Hongliang Lv* is the professor in the school of microelectronics at Xidian university, She currently is the IEEE member and the senior member of the Chinese Institute of Electronics. She obtained a PhD in microelectronics and solid electronics in 2001. She has published nearly forty academic papers in well-known domestic and foreign journals and international conferences, including more than twenty papers by the first author, and more than twenty papers retrieved by SCI, EI, and ISTP, especially in IEEE Trans. On Electron Device, Applied Physics A, Diomand and Related Material, Chinese Physics, Journal of Electronics, and Journal of Semiconductors. Her research interesting includes digital-analog hybrid integrated circuit design methodology. wide band gap semiconductor materials and devices, simulation of new VLSI semiconductor devices, ultra-high-speed semiconductor integrated circuits and RF integrated circuit design.
	*Jianli Chen* is currently a distinguished professor with the Center for Discrete Mathematics and Theoretical Computer Science, Fuzhou University. His research interests include optimization theory and applications, and optimization methods for VLSI physical design automation. In recent three years, Dr. Chen received Best Paper Award from DAC 2017, Best Paper Award Nomination and Best-in-track Paper from ICCAD 2018 and ICCAD 2019. He and his group was the recipient of the First Place Awards at the CAD Contest at ICCAD in 2017, 2018 and 2019, and the EDAthon in 2019, respectively. Dr. Chen also received the CCF Integrated Circuit Early Career Award, and the Distinguished Young Scholars Foundation of FuJian Province in 2018. He has served as TPCs for DAC, ICCAD, ASP-DAC, and so on. Since January 2018, he has served as a Design Automation Technical Committee of IEEE CEDA.
	*Yuanqing Cheng* got his Ph.D. degree from Institute of Comupting Technology, Chinese Academy of Sciences in 2012. Then, he spent one year at CNRS/LIRMM laboratory, Montpellier, France. At the end of 2013, he joined EE department of Beihang University as an assistant professor. During 2015 – 2016, he went to University of California, Santa Barbara, U.S. as a visiting scholar. His research topic includes low power and reliability design for 3D integerated circuits, low power and reliability design for emerging memory technologies, especially STT-MRAM and carbon nanotube devices. He has co-authored more than 40 peer-reivewed papers. He is a member of IEEE/ACM/IEICE/SIGDA/CEDA, a member of IFIP Working Group 10.5, a senior member of CCF (China Computing Federation), and is the TPC member of IEEE/ACM DATE conference, IEEE/ACM ISQED conference, IEEE PATMOS conference and IEEE ISVLSI conference.

6. Agenda

January 8, 2020		
14:00--18:00	Conference Registration	
18:00--20:00	Welcome Dinner	
January 9, 2020		
Venue: Conference Room, 20 / F, Ziction Liberal Hotel		
Time	**Content**	**Speaker**
9:00-9:10	Opening speech	Yue Hao Xidan University
9:10-9:30	Appointment and issuance of foreign honorary professors at the 111 base	Yuming Zhang Xidain University
9:30-10:10		Shaojun Wei Tsinghua University
10:10-10:30	Tea break	
10:00-10:40	Gate-Level Simulation with Consideration of Destabilizing Factors	Vazgen Melikyan (NPUA/Synopsis)
10:40-11:20	Optimisation is a Keyword in IoT	Ricardo Reis (UFRGS)
11:20-12:00	Timing closure challenges at advanced process nodes	Yucheng Wang （SMiT）
12:00-14:00	Business lunch and seminar	Dean Yuming Zhang
14:00-14:30	Break	

January 9, 2020		
Venue: Room 221, East Building, Xidian University		
14:30-15:00	**The co-simulation and co-design methods in heterogeneous integration of III-Vs on Si platforms**	**Hongliang Lv Xidian University**
15: 00-15: 30	**VLSI Mask Optimization: From a Deep Learning Perspective/or Accelerating Deep Convolutional Network Inferences**	**Yu Bei Hong Kong University**
15:30-16:00	**Physical Design Automation for Logic Monolithic ICs: Challenges, Opportunities, and Strategies**	**Carolina Metzler （UFRGS /Cadence）**
16:00-16:30	**Tea break**	
16:30-17:00	**Capacitance Extraction and Power Grid Analysis Using Statistical and AI Methods**	**Wenjian Yu Tsinghua University**
17:00-17:30	**EDA technology for emerging electronic devices and circuits**	**Quan Chen Southern University of Science and Technology**
17:30-18:00	**Analytical Placement Methods for VLSI Circuit Designs**	**Jianli Chen Fuzhou University**
18:00~20:00	**Dinner**	

January 10, 2020		
Venue: Room 221, East Building, Xidian University		
Time	**Content**	**Speaker**
9:00-9:30	**Towards a cloud-native Infrastructure for Open-Source EDA**	**Guojie Luo Peking University**
9:30-10:00	**Machine Learning Based Integrated Circuits Back End Design and Acceleration**	**Yibo Lin Peking University**
10:00-10:30	**Tea break**	
10:30-11:00	**Design and Technology-level Optimization Challenges for Carbon Nanotube Circuits**	**Aida Todri-Sanial (CNRS)**
11:00-11:30	**Emerging Computing Systems: from system analysis to fabricated prototypes**	**Mohamed M. Sabry Aly NTU**
11:30-12:00	**Reliability and DFT of 3D Integrated Circuits**	**Yuanqing Cheng Beihang University**
12:00-12:10	**End of the meeting**	**Dean Yuming Zhang**
12:00-14:30	**Lunch break**	
14:30-18:00	**Visit and exchange**	**Within Xi'an**
18:00-20:00	**Dinner**	