Spin-Transfer Torque Magnetic Tunnel Junction for Single-Event Effects Mitigation in IC Design

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HAL Id: lirmm-02957089

https://hal-lirmm.ccsd.cnrs.fr/lirmm-02957089

Submitted on 9 Jun 2021

Spin-Transfer Torque Magnetic Tunnel Junction for Single Event Effects mitigation in IC design

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Abstract—**For embedded systems in harsh environments, a radiation robust circuit design is still an open challenge. As complementary metal oxide semiconductor (CMOS) processes get denser and smaller, their immunity towards particle strikes decreases drastically. Due to its radiation effects good tolerance and its inherent non-volatility, Spin-Transfer Torque Magnetic Tunnel Junction (STT-MTJ) is considered a promising candidate for high reliability electronics. Nevertheless, when integrated in CMOS circuit, these magnetic devices could be still affected by upsets. To decrease the probability of this occurrence, a radiation robust setup is used to calibrate a physics-based 20 nm MTJ compact model, integrated in a 28 nm Fully Depleted Silicon on Insulator Technology. Thus, a radiation hardening by design (RHBD) solution is presented, where a non-volatile sequential block enables one to mitigate the Single Event Effects (SEEs).**

Index Terms—**STT-MTJ, C-element, SEU, radiation hardening by design (RHBD)**

I. INTRODUCTION AND RELATED WORKS

Solar particle events (SPE), galactic cosmic rays (GCR) and trapped radiation are the major sources of particle flux in space, covering energy range from hundreds of keV to tens of GeV/amu [1], which can lead to Single Event Effects (SEEs) on electronic components. Among this class of effects, the single event that induces a change in the logic state of a memory cell (bit-flip) is called a Single Event Upset (SEU). However, if the voltage pulse induced by the particle strikes does not exceed the breakdown voltage of the transistors, the effect is classified as reversible (soft error) since it can be corrected by reprogramming the circuit into its previous logic state.

Nevertheless, since shielding technique effectiveness has shown important limitations [1] [2] and transistor scaling leads to a relevant impact of soft error even in terrestrial environment [3] designing a radiation-hard IC becomes a real challenge. Thus, several designs have been proposed mainly based on hardware and time redundancy. In [4] redundant feedback lines are used to mask the effects of SEUs. A similar idea is behind the use of SEU-tolerant flip-flop in [5] and the robust latch as proposed in [6]. Radiation hardening techniques

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are also presented in [7] [8] [9]. The main shortcomings of these solutions are the silicon area overhead and the inborn vulnerability of bulk technology to radiations. Due to the encouraging results on radiation effects tolerance [10], [11] in the last few years, STT-MRAM, belonging to the Non-Volatile (NV) Memory class, have been the object of RHBD investigations. For this purpose, latches have been proposed in [12], [13] and [14], as well as a magnetic radiation hard unit introduced in [15].

However, when integrated in a CMOS circuit, STT-MTJs exhibit the same weakness as the other NV memories in harsh environment, i.e. the surrounding peripheral circuits vulnerability. Hence, specific hardening techniques for STT-MTJs must be investigated since they could be affected by radiation-induced errors, due to the integrated CMOS logic. Dealing with this issue has become more and more urgent, as the evolution of MTJ-based technologies allows smaller and smaller writing currents. Indeed, in this scenario, it could be easier for a Single Event Transient (SET) to induce, on the writing/reading transistors, a charge transfer that results in a bit flip. Trying to handle these challenges, radiation-hardened peripheral circuit designs have been proposed in [16], [17] and [18]. The solution proposed in [18] has a radiation hardening capability below 100 fC while showing a negligible performance degradation and low area overhead.

This work combines FDSOI 28 nm, attested to be 6 times more resilient than bulk to heavy-ion induced SEU[19], [20] with STT-MTJs to propose a logic-in-memory circuit able to mitigate the impact of SEEs in an asynchronous micro-pipeline. Moreover, a preliminary investigation on radiation tolerance is done by studying the impact of STT-MTJ's parameters on the overall magnetic device robustness. The compact-model is then calibrated and used to design the radiation tolerant CMOS-STT circuit.

The paper has the following organization: the proposed solution is presented in Section II, robustness evaluation and radiation hardening enhancement are proposed in Section III, Section IV suggests a suitable application scenario and Section V concludes this paper.

II. PROPOSED SOLUTION

A. Detection behaviour

RHBD strategies are commonly used to limit the propagation of an error in a circuit. One of the most widely used solution is the implementation of Dual Modular Redundancy (DMR) combined with C-elements (namely the Muller logic gate [21]), as illustrated in Fig. 1 a.
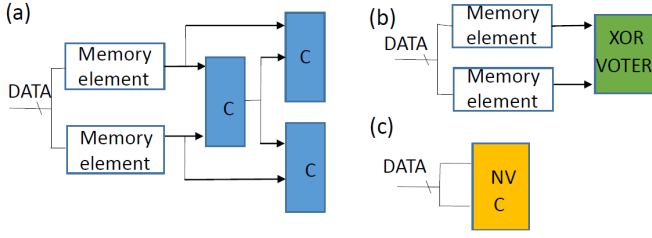
Fig. 1. Simplified radiation hardening solutions in [5] [6] (a), [14] [15] (b) and the one proposed in this paper (c).

The C-element is a state holding circuit, which is transparent when all its inputs are equal, and holds the previous output otherwise, as reported in Table I [21].

Another approach consists in combining memory elements and an XOR that compares data values, at each stage of the DMR, to check if any mismatch has occurred (Fig. 1 b). Both of previous approaches need an external memory element and a circuit able to highlight a mismatch (the XOR or the Muller gate).

On the contrary in this study, the use of STT-MTJs integrates both the memory element and the Muller cell into a single circuit. The proposed circuit receives as input the data path and its duplication as illustrated by Fig. 1 c. It blocks a mismatch propagation (second and third lines of Table I) or, allows, the correct bit propagation (first and fourth lines of Table I). In the context of a multi-stage asynchronous micro-pipeline, it also allows one to restore the correct bit from previous stages. This behaviour is ensured by the C-element that stores the right value inside two STT-MTJs, thanks to a proper control of the Write signal.

TABLE I
TRUTH TABLE OF THE 2-INPUT C-ELEMENT

Input A	Input B	Output
0	0	0
0	1	Previous output
1	0	Previous output
1	1	1

B. Non-Volatile C-element implementation

The MTJ nano-pillar consists of a thin insulating barrier (MgO) sandwiched between two ferromagnetic layers: a reference layer (RL) with a fixed magnetization and a free layer (FL) with a switchable magnetization. Depending on the mutual orientation of these two layers (parallel or anti-parallel) the resistance changes being either low state (R_p) or high state (R_{ap}). Bit "0" or "1" are consequently stored. In STT-MTJ this relies on Spin-Transfer Torque phenomenon and it is made possible by letting a polarized current pass through the magnetic nano-structure. We will call NV error the soft error in the STT-MTJ due to an SEU. STT-MTJ ca be easily integrated into CMOS back-end of line process (BEOL).

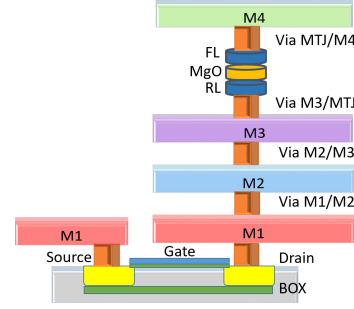Typically, they are inserted after Metal 3 or Metal 4 as depicted in Fig. 2.

Fig. 2. Simplified view of the hybrid magnetic-CMOS process.

In the proposed circuit, MTJs are used to store the output state and its complement while the CMOS part takes charge of the combinational operations. Among the various Muller cell implementations, the Single Inverter Latch (SIL) C-element has been chosen, since it was already demonstrated to be the most soft-error resilient [22].

At first, we propose to make the C-element non-volatile: two MTJs and five transistors are used for this purpose, as depicted in Fig. 3. The circuit level implementation consists of pull-up transistors (P1, P2), pull-down transistors (N1, N2), an inverter (P4, N4) and a weak inverter (P3, N3). Read operations (involving N5, N6, N7 and P5) are achieved by equalizing the voltage of the output node (Q) and node 3 by means of Az signal. Hence, sensing the value of the MTJs resistance (Rd signal) exploiting the Tunnel Magnetoresistance (TMR) effect [23].

$$TMR = \frac{R_{ap} - R_p}{R_p} \qquad (1)$$

To perform a write operation, a bipolar current pulse is generated by driving the gate signal of N8 to logic level high. This current pulse must have the right amplitude and width to switch the orientation of the MTJ's free layer, namely it has to be above the minimum switching required current (critical current, I_c):

$$I_c = \alpha \frac{\gamma e}{\mu_B g}(\mu_0 M_s)H_k V = 2\alpha \frac{\gamma e}{\mu_B g}E \qquad (2)$$

Where α is the Gilbert damping factor, γ is the gyromagnetic factor, e is the electron charge, μ_B is the Bohr magneton constant, g is the spin polarization efficiency, $\mu_0 M_s$ is the saturation field of the free layer, H_k is the anisotropy field, V is the volume of the free layer, and E is the barrier energy [24]. A second novelty consists in adding transistors N9 and N10 to avoid, or at least reduce, the occurrence of non-volatile errors, as it will be detailed in the next section.

Design and simulation results presented in this paper were run with Spectre Electrical Simulator, under Cadence Analog Design Environment platform, using the 28 nm FD-SOI technology PDK from STMicroelectronics. The Supply Voltage was fixed at 1 V. Concerning the STT-MTJ cells,
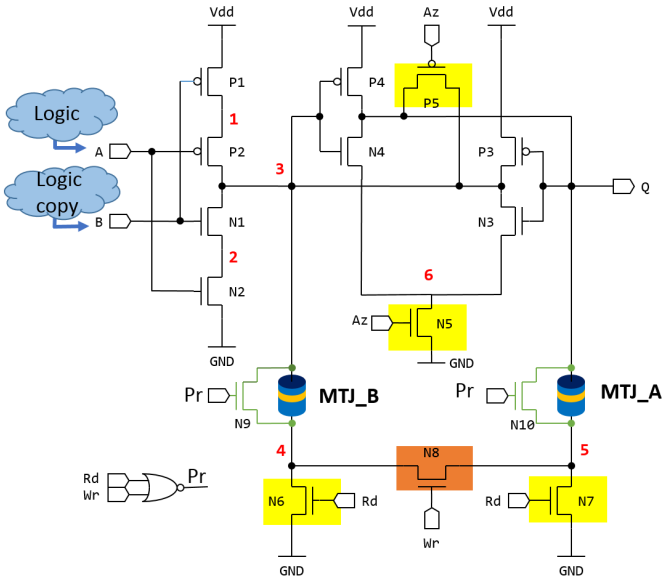
Fig. 3. Proposed radiation tolerant Non-Volatile implementation of the C-element. The numbers in the circuit represent the sensitive nodes.

a physics-based 40 nm perpendicular MTJ compact model described in Verilog A has been used [25]. This model originates from the framework of Julliers' model, Brinkman's model and Simmon's model with an analytical approach and along with some important approximations. In fact, the MTJ switching thresholds are derived from linearization of Landau-Lifshitz-Gilbert (LLG) equation around the stability points. The conductance of the MTJ varies with the bias voltage applied across the device and with temperature. Moreover, as a basic assumption, the magnetization of each FM layer is considered uniform. Monte Carlo simulations at different corners have been run to validate the functional operations of the cell against process, voltage and temperature (PVT) variations for the CMOS part, and resistance-area product, critical current and TMR variations for the MTJ components. Table II shows the default STT parameters in the considered MTJ compact model.

TABLE II
DEFAULT STT PARAMETERS IN THE P-MTJ COMPACT MODEL

Parameter	Description	Value
Area	MTJ surface	20 nm × 20 nm
TMR(0)	TMR with 0 V_{bias}	1.5
E_{bd}	Breakdown electric field	0.8 V/nm
R_p	Parallel resistance	1 kΩ
RA	Resistance area product	1.5 Ωμm²
Ic0	Minimum switching current	50 μA
t_{ox}	Oxide thickness	0.8 nm
P	Polarization of the free layer	0.65

III. ROBUSTNESS ANALYSIS

A. Error model

For the heavy-ion induced events, the deposited charge Q can vary from a few to a few hundreds of femto Coulombs. SETs were injected into the sensitive nodes of the circuit, using a double exponential current pulse, a well-known way to model the electrical impact of particle strikes [26] [27]. The injected current is expressed by the following equation:

$$I_{inj}(t) = \frac{Q_{inj}}{\tau_f - \tau_r} \times \left(e^{\frac{-t}{\tau_f}} - e^{\frac{-t}{\tau_r}} \right) \tag{3}$$

Where Q_{inj} is the amount of collected charge and τ_f and τ_r are, the fall and rise time constants respectively.

B. Critical charge: considerations on MOSFET parameters dependence

The injected charge depends on the timing parameters of the current pulse according to Equation 3. In general, the accumulated charge increases linearly with the increase of the current pulse width. Moreover, the transient current can be enhanced by bipolar amplification due to the parasitic source-body-drain structure. Using the 28 nm FD-SOI technology, we achieved immunity to this phenomenon; as a drawback, aggressive scaling increases the probability of multiple nodes to be affected by one particle strike [28]. In this analysis we injected a double exponential current pulse with a fixed τ_r = 10 ps and a value of τ_f = 120 ps. The dependency of Q_{crit} on transistors width and length has to be taken into account for a robust transistor sizing. Actually, a rigorous definition of critical charge in logic circuit with active feedback is [29]:

$$Q_{crit} = Q_{node} + I_{P,ON} \times \omega_{pulse}$$
$$= C_{node} Vdd + I_{P,ON} \times \omega_{pulse} \tag{4}$$

Where C_{node}, proportional to the product between gate length (L) and width (W), is the capacitance of the considered node and $I_{P,ON}$, proportional to the transistor aspect ratio ($\frac{W}{L}$), is the stabilization current of the pull-up transistors. Thence, the larger the current pulse, the higher the contribution of $I_{P,ON}$. For the chosen τ_f, increasing the transistor width up to 10 times the minimum size allows to increase Q_{crit} by almost a factor of 10.

Low threshold voltage transistors were employed to guarantee a fast stabilization of the node charge and, therefore, to enhance the advantage of the quenching phenomena in 28 nm FD-SOI, which, by means of the electron-hole recombination, results in a faster decay of the transient.

C. Errors injection

The STT compact model was calibrated with the parameter's values listed in Table II. Errors were injected into the sensitive nodes of the proposed circuit (numbered from 1 to 6 in Fig. 3). Simulation results can be summarized as follows:

- SET at node 1 or node 2 will not affect the output of the C-element; only a simultaneous hit of both will inevitably affect the output computation.

- Since Az signal is normally high, a strike at node 6 could lead to a transient disturbance only during sensing operation (N5 off). Using wider windows of activation for both Az and Rd signals reduces the probability for this event to affect the read operation. An enhancement of the MTJ reading reliability could also be achieved with higher TMR as detailed in paragraph D.
- A hit at node 3, the most critical node of the volatile part, leads directly to a transient on the output. Even so, as detailed in Fig. 4, Q quickly recovers its value in a time, referred to the recovery time, ranging from 250 ns to 350 ns for an injected charge varying from 100 fC to 330 fC, respectively.
- Both node 4 and node 5 are the most critical for the NV-part. In order to test their behaviour when an SET occurs, the protection transistors N9 and N10 have been disconnected in this first step. A charge of 100 fC has been injected on the drain of the read/write off transistors. As a result, a current above the critical value flows through the MTJ, reversing its memory state. Therefore, this SET induced a non-volatile SEU, compromising the stored data reliability. Then, we keep increasing the injected charge to evaluate how the output node, Q, is affected. Actually, the occurrence of NV errors in MTJs and SEEs on the output node are quite independent. Still up to Q_{inj} = 240 fC in node 4, the output of the circuit, Q, quickly recovers from the SET, so that the non-volatile error occurs even if the output of the circuit is correct (Fig. 5). Despite this, it is not acceptable to maintain an incorrect stored data in the memory part of the circuit. The same amount of charge, injected at node 5, results in a NV error and also in a SEU on Q node (Fig. 6): this is easily understandable since the affected node is closer to node Q than node 4. In both transient simulations, the current induced in the MTJ in parallel state (storing the bit "0") is higher with respect to the current induced in the antiparallel state, precisely because of the lower value of its resistance. This is noticeable in Fig. 5 by observing the transient current peak on MTJ's free layer. This should not be confused with the fact that, the switching energy is lower for AP→P than for P→AP, as it is well known from Spin Transfer Torque theory [30].

D. Radiation hardening enhancement

Since current peaks induced on the drain are usually intense and narrow [31], two different strategies are pursued: on the one hand, minimizing the probability of a NV upset induced by the strike, $P(t_{strike})$, by making it more difficult to upset the FL; on the other hand, reducing as much as possible the current, induced by an upset, flowing though the MTJs. The latter is achieved by activating, during the standby window (i.e. when neither a write nor a read operation have to be performed), two transistors, providing a shunt path for the current, which will act as a protection for the stored data.

1) Impact of MTJ parameters on radiation hardening:
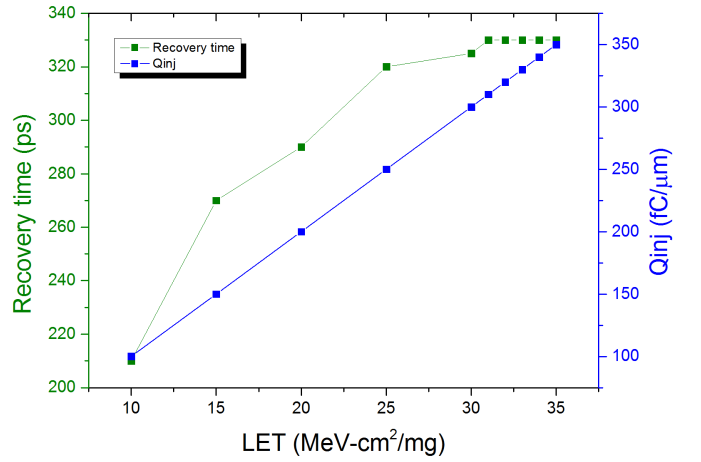- Resistance-area product (RA):

Fig. 4. Recovery time at node 3 after a particle strike with different linear energy transfer (LET) values.
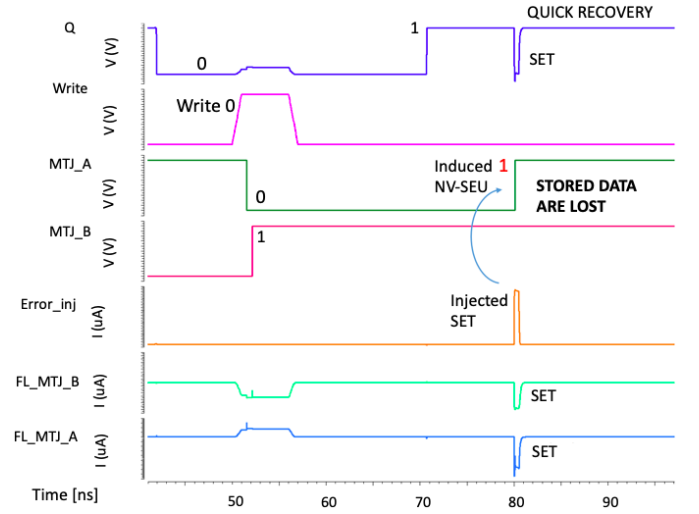

Fig. 5. Transient simulation waveforms of the Non-Volatile C-element when Q_{inj} = 240 fC in node 4.

According to [30], the switching probability during a sub-critical current pulse is given by:

$$P(t_{strike}) = 1 - exp(-\frac{t_{strike}}{\tau_{switch}}) \qquad (5)$$

Where t_{strike} is the duration of the current induced by the upset, and τ_{switch} is the mean time needed to switch the MTJ's free layer orientation. Immediately following from Equation 5, a way to minimize the $P(t_{strike})$ is to increase τ_{switch}. This could be done by increasing the RA parameter [32], [33] and evaluating the impact on the other STT-metrics:

$$RA \propto exp(-\frac{4\pi t_{ox}\sqrt{2m\phi}}{h}) \qquad (6)$$

Where h is the Planck constant, ϕ the barrier potential height and m the effective mass of the electron. At first, it
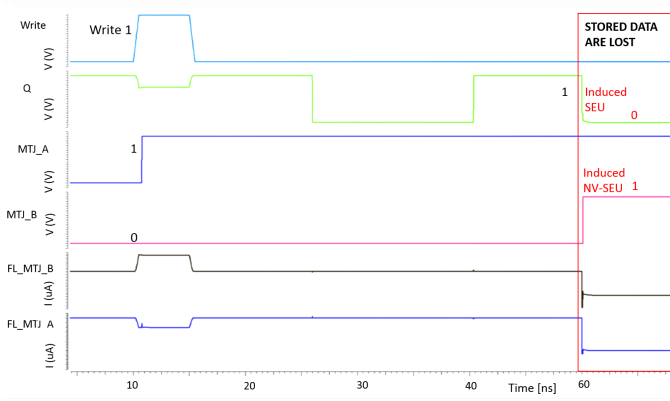
Fig. 6. Transient simulation waveforms of the Non-Volatile C-element when Q_{inj} = 240 fC in node 5.

should be noticed that the increase of RA is exponentially related to the increase of oxide thickness. The role of the tunnel barrier thickness is crucial to enhance radiation tolerance: the thicker t_{ox}, the higher the breakdown energy of the MgO, thus the more robust to radiations the MTJ. Nevertheless, a particular attention must be given to the growing of t_{ox}, which makes it more difficult to upset but also increases the resistance of the magnetic device. Clearly, this could lead to the failure of standard writing operations. Moreover, due to the limited length of spin relaxation, the MgO thickness has to be thin enough to ensure the electron tunnelling possibility [33]. In addition, the reliability of reading operations has to be increased. For this reason, the increase of RA has a good impact because it leads to a linear increment of the TMR. This relation was proven experimentally and is valid in the region below RA values of 10 $\Omega\mu m^2$.

- Thickness (volume) of the free layer:
Following Equation 2, this parameter is directly involved in the critical current definition. By increasing the free layer volume (or thickness since a constant MTJ diameter is considered), more current would be needed to switch the magnetization of the FL, thus critical current increases. As a result, $P(t_{strike})$ is lowered; as a drawback, the write energy is increased.

Increasing the free layer volume leads to higher thermal stability, as described by Equation 7. This has a beneficial effect on the retention time and on the radiation tolerance, since data stored are less sensitive to the thermal and energy fluctuations [30].

$$\Delta = \frac{E}{K_B T} \qquad (7)$$

In Equation 7 the energy barrier E, proportional to free layer volume, has been already defined in Equation 2 and $K_B T$ is the thermal activation energy at the operating temperature, with K_B the Boltzmann constant and T the temperature.

- Size:

In this analysis, the MTJ's area is kept constant with the aim to investigate the radiation tolerance of scaled MTJ integrated in a 28 nm FD-SOI technology. Thus, a radius of 20 nm is kept constant in this design.

Table III summarizes the effect of the considered parameters on $P(t_{strike})$ and the write energy. Interestingly enough, these last two metrics have opposite trends, suggesting that high MTJ robustness and low write energy cannot be achieved at the same time. Since the proposed circuit was conceived in such a way that a reduced number of write operations have to be accomplished, this penalty has less impact than in the other proposed design [14]. In conclusion, by taking into account these observations, a new setup, suitable for radiation hardening purpose, is used to calibrate the STT model, as detailed in Table IV.

TABLE III
IMPACT OF RA INCREMENT ON MTJ RADIATION ROBUSTNESS FOR MTJ RADIUS = 20 NM

Symbol	Parameter	$P_{MTJ_{upset}}$	Write energy
R_p ⇑	Parallel resistance	⇓	⇑
τ_{switch} ⇑	Mean time for MTJ switch	⇓	⇑
TMR ⇑	Tunnel Magnetoresistance Ratio	⇓	-
$E_{barrier}$ ⇑	Oxide barrier energy	⇓	⇑
t_{ox} ⇑	Oxide thickness	⇕	⇑
Δ ⇑	Thermal stability factor	⇓	-
V ⇑	Volume of the free layer	⇓	⇑

TABLE IV
ROBUST SETUP FOR STT PARAMETERS IN THE P-MTJ COMPACT MODEL

Parameter	Description	Value
Area	MTJ surface	20 nm × 20 nm
TMR(0)	TMR with 0 V_{bias}	2.0
E_{bd}	Breakdown electric field	0.8 V/nm
R_p	Parallel resistance	6.8 kΩ
RA	Resistance area product	8.5 $\Omega\mu m^2$
Ic0	Minimum switching current	67 μA
t_{ox}	Oxide thickness	1.1 nm
P	Polarization of the free layer	0.71

2) Impact of the shunt path on radiation hardening: As an alternative, a less resistive path is created by the insertion of two NMOS (N9, N10) in parallel to each MTJ. The key idea is to obtain a resistive shunt path for the current pulse induced by particle strikes. Hence, provided that $R_{on} \ll R_p$, the quantity of current flowing through the MTJs will not be enough to

induce their switching. The R_{on} of the NMOS transistor in linear region will vary as:

$$R_{on} = \frac{1}{2K_n(V_{gs} - V_{dt})} \quad (8)$$

Where K_n is the electron mobility. Thus, a trade-off between large transistors and robust enhancement is mandatory. After a parametric analysis, a transistor aspect ratio between 8 and 10 has been chosen for the design, in spite of a slight area penalty.

Additionally, to ensure the validity of this solution, the gate signal of N9 and N10 has to be carefully controlled. A NOR gate between the *Read* and *Write* signals ensures that they do not interfere with the standard operations. It acts when N6, N7, N8 are off, so node 4 and node 5 represent exactly the drain of the off NMOS transistor.

Simulation results show that the insertion of the NMOS in parallel to each MTJ increases the circuit robustness to non-volatile errors up to 3 times with respect to the solution without the shunt path, and 1.5 to 3 times with respect to the designs in the state of the art [13], [14], [16], [15]. As highlighted in Fig. 7, after a Q_{inj} = 300 fC in node 4, the output Q quickly regains its original value (it takes around 1 ns in the worst case) and the information stored in the MTJs are not affected at all. Concerning the strike at node 5, the output Q will be reversed as in the non radiation-tolerant version. Nevertheless, since MTJs are not affected, the correct value can be restored as detailed in Section IV.
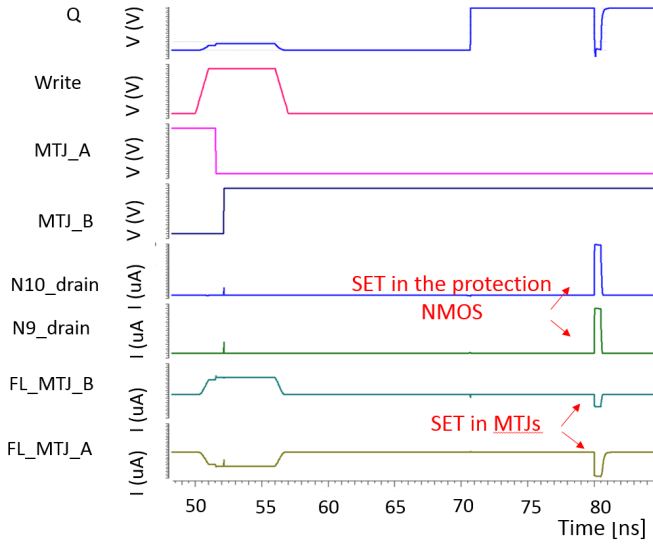

Fig. 7. Transient simulation waveforms of the radiation tolerant Non-Volatile C-element when Q_{inj} = 300 fC in node 4.

Fig. 8 summarizes the errors injection response in terms of recovery time (duration of the transient on the output of the circuit, Q) and current induced (intensity of the transient) in the parallel state MTJ, by varying the quantity of injected charge. The two NV C-elements, the basic version and the radiation-tolerant one, are then compared in the plot. Starting

from 250 fC, the current induced in the parallel state (worst case) of the MTJ is slightly above the critical current value (~2 μA). In spite of this, no bit flip occurs because the transferred energy is not enough to reverse the FL magnetization. This is valid up to ~308 fC when random switching is observed even in the presence of the protection transistors. The radiation-tolerant version of the circuit also leads to a faster recovery time of the output Q (25% faster). This can be explained with the charge recombination process in the inserted protection transistor. Unfortunately, this is not sufficient to cause an increase of the critical charge in node Q.
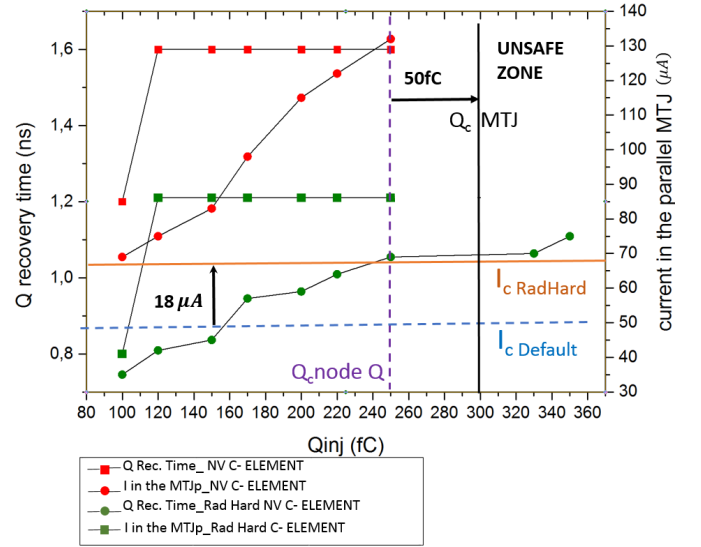

Fig. 8. Output recovery time and current peak induced in the parallel MTJ after an SET with different energy values. The radiation hardened version and the basic version are plotted.

We also have to consider that the circuit is still vulnerable to multi-node upset, as noticeable from Fig. 9. Indeed, if several nodes are affected at the same time the output of the N9-N10 control logic can be flipped. In this case, the shunt path would either not be activated (bit flip from "1" to "0"), or activated when it should not (bit flip from "0" to "1"). In this istance, reading or writing operation may be concerned. However, this occurance depends meanly on the amount of collected charge, which determines the SET expiration time and thus the vulnerability window.

Fig. 10 compares the radiation-tolerant version of the circuit, the basic one (taken as the baseline) and solution from [15] and [18]. It is interesting to notice that, as expected, the main penalty of the robust version is the mean write energy, estimated to be 187 fJ per write operation (mean writing time being 2.8 ns and I_{c0}~67 μA, at 1 V). This is due to changes in the MTJ setup in order to achieve higher radiation tolerance. The penalty due to a higher cost for a single write operation is softened by the reduced number of them, as will be further detailed in the next Section. Unlike the other solutions, memory elements and peripheral circuit being merged in the same circuit, area is not a critical metric for this circuit. On the contrary, delay is the major penalty.

This is not surprising since, among the existing C-element implementations, the SIL one is the most robust and the slowest. Moreover, an additional delay is added because of the insertion of transistors P5 and N5 in the proposed non-volatile version, since they have to disconnect (connect) the SIL part from (to) GND to allow the MTJ reading operations. However, the main advantage of the proposed solution is the capability of correcting errors due to SEEs along all the sensitive nodes in the C-element and to store, in the same cell, the correct data. The non-volatile errors radiation tolerance is shown to be up to 3 times higher than the other solutions.
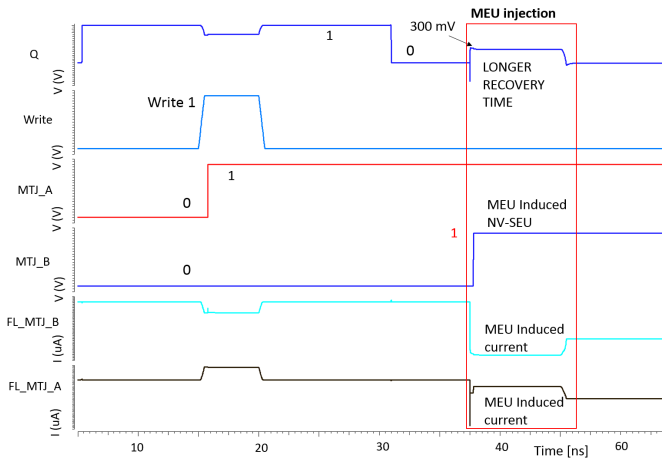

Fig. 9. Transient simulation waveforms of the radiation tolerant Non-Volatile C-element when Q_{inj} = 308 fC in node 4 ad 5.
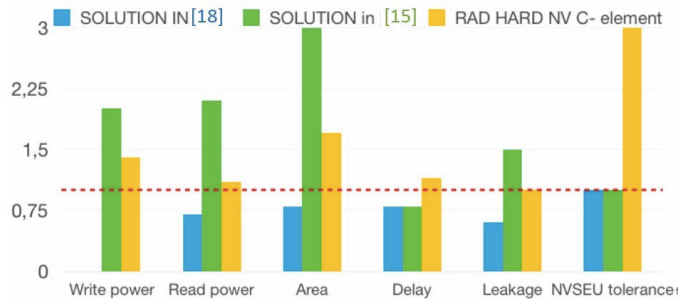

Fig. 10. Performances, area and robustness comparison between the proposed solution and the state of the art. The basic version of the NV C-element is assumed as the baseline (red dotted line). Data for solution in [18] refer only to the read circuit.

IV. ASYNCHRONOUS MICROPIPELINE

In this section, a possible radiation hardening scenario is suggested: the use of the proposed NV C-element in an asynchronous DMR micropipeline, as depicted in Fig. 11. A traditional asynchronous micropipeline is formed in stages. Each stage integrates a half buffer formed of several volatile C-elements. Thence, if the circuit is powered down, the data stored by the various half buffer are lost. The same will happen in case of a reset event. By using the cell presented in this

paper, the SEEs are mitigated while the immunity to power-off and resets is achieved without the need to duplicate the memory elements. Indeed, if a mismatch between the two data-paths occurs, the error propagation is blocked by the C-element. Write and read operations are handled by an XNOR and inserted in each stage. The write signal is only activated if the inputs of the C-element are equal. Otherwise, the read signal performs the reading of the bit stored in the previous stage, allowing the combinational block to carry out again its operations. Since write operations can occur only if data are correct, their reduced number mitigates the increase of write energy per bit. The output of the XNOR is also sent to an AND gate in charge to propagate the Acknowledgment signal along the return path, with the aim to confirm (output "1") or not (output "0") the readiness to receive new data, according to the 4 phases handshake protocol requirements.
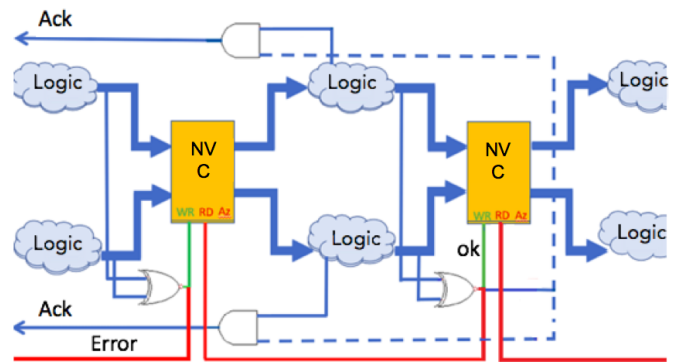

Fig. 11. SEEs mitigation in an asynchronous micro-pipeline hardened by means of the proposed Non-Volatile C-element.

V. CONCLUSIONS AND PERSPECTIVES

In this paper, we propose a STT-MTJ based C-element with enhanced single-event tolerance. Error injections in sensitive nodes attested that only two nodes of the circuit could lead to non-volatile errors and, thus, to SEU in the memory part of the circuit. A radiation-tolerant design has been proposed and tested through simulations to avoid, or at least decrease, soft errors in non-volatile magnetic elements. A specific STT-MTJ setup has been used for this purpose: STT values have been settled accordingly with the aim to decrease the MTJ's radiation-induced switching probability. An increase of write energy and delay are the drawbacks of this solution. To mitigate the first, a proper control of the write signal has been proposed. A suitable scenario for the presented VLSI cell is also mentioned: in the context of DMR micro-pipelined asynchronous circuit, the integration of the proposed circuit is convenient to block SEEs propagation, achieving SEU tolerance. As next step, a validation of the design behaviour under irradiation by means of TRADCARE engineering tool [34] is planned. Then, heavy-ion and proton test campaigns will be performed to confirm simulation results. There are also limits inherent to the FDSOI technology robustness: on the one hand, it is shown to be more tolerant to SEU [35];

on the other, it is more sensitive to Total Ionizing Dose (TID) if compared with bulk technology [36]. For future works, it should be interesting to evaluate a better trad-off between SEU mitigation and TID tolerance, for example investigating design based on PDSOI technology and STT-MTJ.

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