

Workshop on Artificial Intelligence 2020
Talk Abstract Submission

Title: Neuromorphic Computing based on Oscillatory Neural Networks

Speaker: Aida Todri-Sanial, LIRMM, University of Montpellier, CNRS, France

Abstract:

Neuro-inspired computing employs technologies that enable brain-inspired computing hardware for more efficient and adaptive intelligent systems. Mimicking the human brain and nervous system, these computing architectures are excellent candidates for solving complex and large-scale associative learning problems. In this talk, we will showcase a novel and alternative neuromorphic computing paradigm where information is encoded in the phase of coupled oscillating neurons or oscillatory neural networks. The VO₂ metal-insulator transition devices emulate biological neurons and 2D MoS₂ memristors emulate synapses.

Current research efforts on neuromorphic computing are mainly focused on the various hardware implementation of synapses using memristors such as resistive random access memory (RRAM) technology, spin-based and ferroelectrics. But, several challenges hinder current memristive neuromorphic hardware from going mainstream due to latency (delay in accessing the device and charging/discharging wires), and density of synapse matrix allowed by the manufacturing process. In the framework of EU H2020 NeurONN project, we implement and explore energy-efficient neuromorphic computing based on oscillatory neural networks (ONN) [1] using metal-insulator-transition (MIT) for emulating “*neurons*” and 2D material memristors for emulating “*synapses*” to achieve a truly neuro-inspired computing paradigm for enabling AI at the edge [2-4].

In ONN, the principle of operations is “oscillation phase” rather than the charge-time dependent switching to emulate biological neurons. By describing neurons as oscillators, one can limit their oscillation amplitudes to small values to limit power consumption, as interconnects would only vary their voltage swings to a limited range. On the other hand, more conventional Spiking Neural Networks (SNN) or non-spiking Artificial Neural Networks (ANN), must use full voltage swings to communicate and compute. Therefore, ONNs have an unprecedented efficient way of drastically reducing power consumption for the same system complexity. A comparison of the computing in “time” vs “phase” and the architecture with energy efficient components of NeurONN is illustrated in Figure 1.

In this talk, several ONN aspects will be covered from devices, architecture design to training algorithms in order to highlight the potential and novelty of ONN for energy efficient brain-inspired computing. The talk is in line with the innovative themes of the Workshop on AI 2020 on “Development of the foundation of AI”.

Acknowledgement:

This work is supported by the European Union’s Horizon 2020 research and innovation program, EU H2020 NEURONN (www.neuronn.eu) project under Grant No. 87150

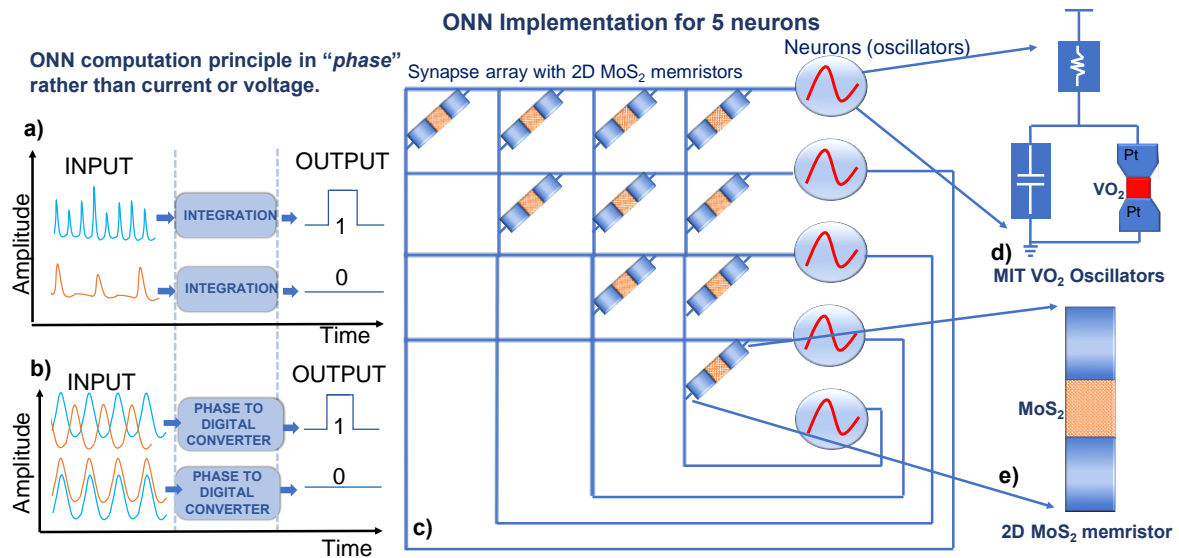


Figure 1. a) spiking neuron voltage amplitude used for encoding information such as in spiking neural networks. b) ONNs use a different paradigm by using *phase* to compute, rather than current or voltage. c) Illustration of ONN implementation with 5 oscillating neurons and resistive synaptic coupling, d) oscillating neuron is based on MIT VO₂ devices, and e) synapse weights with 2D memristor (MoS₂) devices. The fully-connected array uses only $n(n-1)/2$ memristors compared to n^2 as in other topologies such as SNN and ANN.

References:

- [1] E. M. Izhikevich, Computing with Oscillators, Neural Networks, 2000.
- [2] E. Corti, A. Khanna, K. Niang, J. Robertson, K. Moselund, B. Gotsmann, S. Datta, S. Karg, Time-Delay Encoded Image Recognition in a Network of Resistively Coupled VO₂ in Si Oscillators, Electron Device Letters, 2020.
- [3] E. Corti, B. Gotsmann, K. Moselund, A. Ionescu, J. Robertson, S. Karg, Scaled Resistively Coupled VO₂ Oscillators for Neuromorphic Computing, Solid State Electronics, 2020.
- [4] Th. Jackson, S. Pagliarini, L. Pileggi, An Oscillatory Neural Network with Programmable Resistive Synapses in 28nm CMOS, IEEE ICRC, pp.118-124, 2018.