Novel Quadruple-Node-Upset-Tolerant Latch Designs with Optimized Overhead for Reliable Computing in Harsh Radiation Environments

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Abstract—With the rapid advancement of CMOS technologies, nano-scale CMOS latches have become increasingly sensitive to multiple-node upset (MNU) errors caused by radiations. First, this paper proposes a novel latch design, namely QNUTL that can completely tolerate MNUs such as double-node upsets, triple-node upsets (TNUs), and even quadruple-node upsets (QNUs). The latch is mainly constructed from three dual-interlocked-storage-cells (DICEs) and a triple-level soft-error interceptive module (SIM) that consists of six 2-input C-elements. Due to the single-node-upset self-recoverability of DICEs and the soft-error interception of the SIM, the latch can completely tolerate any QNU. Next, by replacing the DICEs in the QNUTL latch by clock-gating (CG) based ones, a QNUTL-CG latch is proposed to significantly reduce power consumption. Simulation results demonstrate the MNU-tolerance of the proposed latches. Moreover, owing to the use of a high-speed transmission path, clock-gating, and a few transistors, the proposed QNUTL-CG latch has low overhead in terms of area, D-Q delay, CLK-Q delay, and setup time, compared with the state-of-the-art TNU-tolerant latch (TNUTL) which is not QNU-tolerant.

Index Terms—Latch design, fault tolerance, reliable computing, triple-node-upset, quadruple-node-upset

1 Introduction

CMOS technologies have scaled down to the deep nano-scale level, enabling high integration, low overhead, and high performance for integrated circuits and systems. However, with the aggressive reduction of transistor feature sizes, the sensitivity of CMOS devices to soft errors has significantly increased, which can result in data corruptions, execution failures, or even system crashes in the worst case. When radiative particles, such as protons and neutrons, collide with sensitive nodes of integrated circuits, they may generate additional charges causing erroneous transient pulses or node-upsets that are called soft errors [1-2]. Soft errors include *single-node upsets* (*SNUs*), *double-node upsets* (*DNUs*), *triple-node upsets* (*TNUs*), and even *quadruple-node upsets* (*QNUs*). Soft errors can severely affect the reliability of safety-critical applications, especially for those circuits and systems used in harsh radiative environments, e.g. aerospace [3]. Although the recently adopted FinFET technology can reduce the soft error rate at transistor or cell level [4], effective and scalable solutions for soft error tolerance are still needed.

In fact, a pool of very interesting papers, such as paper [5], shows that yes, FinFET technology can reduce the soft error rate at transistor or cell level, but they also show that *single-event upset* (*SEU*) rates and mitigation choices for FinFET-based circuits are strongly influenced by the supply voltage and the operating environment. In Fig. 3 of paper [5], we can see that the impact of supply voltage on the SEU cross-section is very high, and that with Vdd scaling, even a FinFET technology may become less stronger / robust when compared to a planar 20 or 28 nm technology (we do not intend to scale down Vdd for low power). This clearly shows the need to consider single but also multiple soft errors, and especially QNUs in latches and flip-flops.

To mitigate data corruptions, execution failures, or even system crashes caused by soft errors, many designs, such as memory cells [6-8], flip-flops [1, 9-11], and latches [2, 3, 12-26], have been proposed. This paper focuses on the design of latches. For unhardened designs, a striking-particle can cause state changes of single nodes that are called SNUs. Due to charge-sharing [27], a striking-particle can cause state changes of double-nodes that are called DNUs. Moreover, due to the drastic reduction of transistor feature sizes, a striking-particle can affect multiple-nodes simultaneously, thus causing *multiple-node upsets* (*MNUs*) that include TNUs and even QNUs. Although most of the existing latch designs are hardened against soft errors, they still suffer from severe problems.

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First, for SNU-tolerant latch designs [12-13], any of them has at least one node-pair that cannot effectively tolerate a DNU. Second, TNUs cannot be effectively tolerated by DNU-tolerant latch designs [14-15, 18-20]. Third, TNU-tolerant latch designs [1, 16-17] cannot effectively tolerate QNUs, despite a large area overhead.

To the best of our knowledge, so far there is no latch design that can provide complete QNU-tolerance. Reliability and area/delay/power overhead of latch designs are crucial for safety-critical applications. A latch may be switched off into standby mode to significantly reduce power dissipation. In this case, the hold mode duration of the latch may last for a long time. During this long duration, the latch may be impacted by a series of radiative particles in harsh environments, thus causing many accumulated errors, such as QNUs. Let us discuss this point in more details. Let us assume that a DNU recoverable latch is switched off into standby mode to significantly reduce power dissipation, and that the hold mode duration of the latch lasts for a long time. During this long duration, the latch may be impacted by a radiative particle and cause a TNU. In these conditions, the latch can no longer output a correct value and the error will be kept. During this long duration, the latch may be impacted by another radiative particle and cause an SNU. Since the latch is already affected by a TNU, it may no longer provide good DNU-recovery during the switched off duration, and thus the TNU and the SNU can be accumulated to form a QNU (and even the values of all nodes in the latch can be flipped).

Due to charge-sharing, a QNU can also be caused by one striking-particle, causing invalid value-retention in circuits and systems. Note that no research indicates the occurrence probability of charge-sharing induced QNU. However, if a circuit is highly integrated and fabricated with a very small technology node such as 7nm, it is likely that more transistors/nodes will be much closer to each other, thus causing severe increase of the probability of an event like that. Let us take *the TNU tolerate latch* (*TNUTL*) [3] as example. In hold mode, when the four inputs of a C-element are affected by a QNU, the latch will output a wrong value, i.e., the latch cannot tolerate the QNU. However, especially for safety-critical applications in harsh environments, if a latch can effectively tolerate any QNU, the latch can output the correct values, thus providing very high reliability for reliable computing.

New phenomena highlighted in [28] show that the aggressive reduction of transistor feature sizes can lead to *multiple-bit-upsets* (*MBUs*) that include *triple-bit upsets* (*TBUs*) and *quadruple-bit upsets* (*QBUs*). Fig. 1 shows single-bit upset (SBU), double-bit upset (DBU), and MBU percentages in different technology nodes for storage cells. It can be seen from Fig. 1 that MBUs are becoming a critical challenge as technology scales down. Therefore, in deep nano-scale technologies, MNUs, such as TNUs and QNUs, may also have an increasing percentage, especially for safety-critical applications in harsh environments, seriously affecting the reliability of latches.

It should be noted that providing an accurate and realistic calculation of the occurrence probability of a TNU/QNU is quite complex since many factors such as (1) technology data; (2) layout (to know effective area that may be affected by particles, spacing among adjacent nodes, etc.); (3) working conditions (hold mode duration, supply voltage, working temperature, etc.); (4) particle types (neutron, proton, α-particle, heavy ion, etc.); (5) particle properties (flux distribution, effective hit rate, linear energy transfer, hit angle, etc.); (6) particle correlations, etc., should be known.

The above issues motivate us to design highly reliable latches to tolerate MNUs, such as TNUs and QNUs, for reliable computing of safety-critical applications.

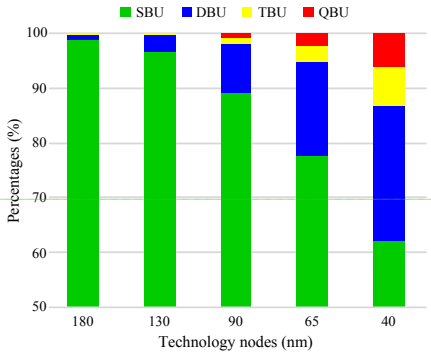

Fig. 1. Single-, double-, and multiple-bit-upset percentages in different technology nodes for storage cells [28].

In this paper, a novel *Quadruple-Node-Upset-Tolerant Latch* (*QNUTL*) design and its advanced version, namely QNUTL-CG, protected against MNUs are proposed. The QNUTL latch mainly consists of three independent *dual-interlocked-storage-cells* (*DICEs*) [29] and a triple-level *soft-error interceptive module* (*SIM*). Each DICE is constructed from four *input-split inverters* (*IINVs*), and two of its non-adjacent nodes are used as the inputs of the SIM. The SIM consists of six 2-input *C-elements* (*CEs*), and the outputs of the CEs in the first stage are used as the inputs of the CEs in the second stage, which is similar to the second stage versus the third stage. Each DICE can self-recover from any possible SNU, and the SIM can intercept errors in a triple-level manner. Therefore, the proposed QNUTL latch can effectively tolerate QNUs. Moreover, a high-speed path and a *clock-gating* (*CG*) technique are used in the QNUTL-CG latch to reduce overhead. Simulation results demonstrate the any-possible-QNU tolerance and moderate overhead of the proposed QNUTL/QNUTL-CG latch designs.

The rest of the paper is organized as follows. Section 2 introduces typical SNU, DNU, and/or TNU hardened latch designs. Section 3 describes the schematic, normal working principles, and fault-tolerance verifications for the proposed latch designs. Section 4 presents comprehensive evaluation and comparison results for the proposed and existing state-of-the-art latch designs. Section 5 concludes the paper.

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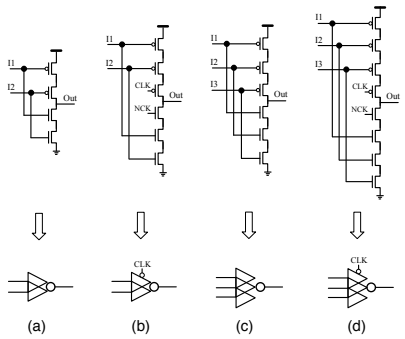

Fig. 2. Schematics of different C-elements. (a) 2-input, (b) Clock-gating based 2-input, (c) 3-input, and (d) Clock-gating based 3-input.

2 Previous Hardened Latch Designs

CEs are widely used in many hardened latch designs. Fig. 2 shows the schematic of different CEs, including the 2-input and 3-input, and the CG based 2-input and 3-input ones. The 4-input one can be created in a similar manner. When the inputs of a CE have the same value, the CE will output the reversed value of its inputs; when the inputs of the CE change and have different values, the CE will still have the previous correct value at its output due to attached capacitances and/or keepers. Fig. 3 shows the schematics of existing hardened latch designs, including *the FEedback Redundant SNU-Tolerant* (*FERST*) [12], *High Robust and Low Cost* (*HRLC*) [13], *Dual-input Inverter Radiation Tolerant* (*DIRT*) [14], *High Robust and Cost Effective* (*HRCE*) [15], *Low Lost and TNU completely Tolerant* (*LCTNUT*) [16], four DICEs based TNU resilient (DICE4TNU) [17], and *TNU-Tolerant Latch* (*TNUTL*) [3] latch designs.

The schematic of the FERST latch [12] is shown in Fig. 3-(a). It can be seen that the FERST latch consists of two parts. The top part is constructed from two interlocked feedback loops based on CEs and inverters to retain values, and the bottom part is mainly a 2-input CE used as a voter. For avoiding high-impedance state at Q, a weak keeper is added to Q. Note that, the switches in Fig. 3 denote the *transmission gates* (*TGs*) used to control node connections. For example, each TG marked with the *negative system clock* (*NCK*) indicates that the gate terminal of the pMOS transistor is connected with NCK and the gate terminal of the nMOS transistor is connected with the *system clock* (*CLK*). This functioning applies for all latches in this paper. The schematic of the HRLC latch [13] is shown in Fig. 3-(b). It can be seen that the HRLC latch

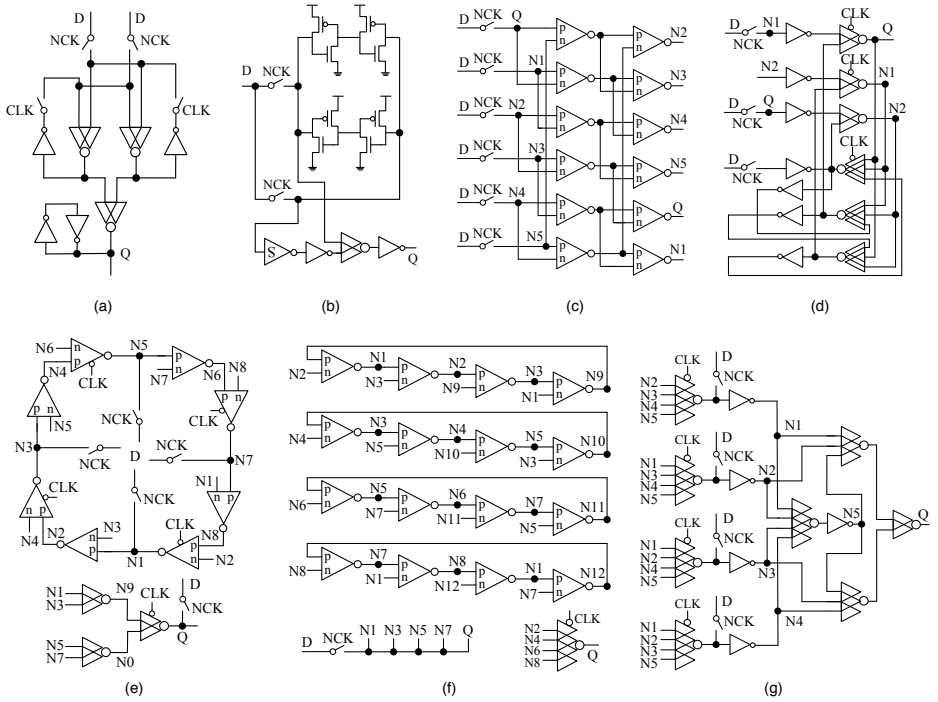

Fig. 3. Schematics of existing hardened latches. (a) FERST [12], (b) HRLC [13], (c) DIRT [14], (d) HRCE [15], (e) LCTNUT [16], (f) DICE4TNU [17], and (g) TNUTL [3].

consists of two parts. The top part is constructed from four interlocked input-output-coupled inverters, and the bottom part is constructed from a Schmitt trigger inverter marked with S, a 2-input CE, and two inverters. The FERST latch and the HRLC latch are SNU-tolerant. However, they are not hardened against DNUs.

The schematic of the DIRT latch [14] is shown in Fig. 3-(c). The latch is constructed from two levels of IINVs. In each level, there are six IINVs, and each IINV consists of a pair of pMOS and nMOS transistors that have different gate-terminals, making the DIRT latch DNU-tolerant. The schematic of the HRCE latch [15] is shown in Fig. 3-(d). The latch is mainly constructed from many 2-input CEs, 3-input CEs, and inverters to form many interlocked feedback loops, making the latch DNU-tolerant. However, these latches cannot provide complete TNU-tolerance.

The schematic of the LCTNUT latch [16] is shown in Fig. 3-(e). The latch consists of a *storage module* (*SM*) and a two-level SIM. The SM comprises eight IINVs that include four CG-based ones. The schematic of the DICE4TNU latch [17] is shown in Fig. 3-(f). The latch consists of four DICEs and a CG-based 4-input CE. The four DICEs are interlocked, and each pair of the DICEs shares a common node. The inputs of the 4-input CE are fed by the internal nodes of these DICEs. The schematic of the TNUTL latch [3] is shown in Fig. 3-(g). It can be seen that the latch comprises two parts. The left part consists of four interlocked 4-input CEs and four inverters, and the right part consists of a 4-input CE, two 3-input CEs, and a 2-input CE. These latches are TNU-tolerant. However, they are not hardened against QNUs.

3 Proposed QNU-Tolerant Latch

3.1 Latch Schematic and Working Principles

Fig. 4 shows the schematic of the proposed QNUTL latch. The latch is mainly constructed from three independent DICEs (i.e., DICE1, DICE2, and DICE3) on the left side and a triple-level SIM on the right side as shown in Fig. 4. The inputs of the SIM are fed by the non-adjacent nodes (i.e., N1, N3, N5, N7, N9, and N11) of DICEs. The SIM consists of six 2-input CEs (i.e., CE1 to CE6) that include one CG-based CE (i.e., CE6) at the output stage. The outputs of CE1, CE2, and CE3 are fed to the inputs of CE4 and CE5. The outputs of CE4 and CE5 are fed to the inputs of CE6, and the output of CE6 is the output of the proposed latch. In the latch, D is the input, Q is the output, N1 to N12, and X1 to X5 are the internal nodes, CLK is the system clock, and NCK is the negative system clock, respectively.

Fig. 5 shows the schematic of the proposed QNUTL-CG latch. Compared with the QNUTL latch, the QNUTL-CG latch has the same fault-tolerance capability, but its overhead especially for power dissipation is effectively reduced due to the use of the CG technique. Thus, we concentrate on the QNUTL latch to describe the working principles.

In transparent mode, CLK = 1 and NCK = 0, and all the transistors in TGs are ON. In the following, we take D = Q = 1, i.e., N2 = N4 = N6 = N8 = N10 = N12 = 1 as an example to describe all behaviors of the latch. Obviously, N1 and N3 can be determined by N2 and N4 through DICE1. Similarly, N5, N7, N9 and N11 can be determined through DICE2 and DICE3, respectively. Thus, N1 = N3 = N5 = N7 = N9 = N11 = 0. To reduce power dissipation and transmission delay, CG has been used in CE6 to avoid current competition on Q in transparent mode. Therefore, the proposed latch can be properly initialized, and Q can be determined from D.

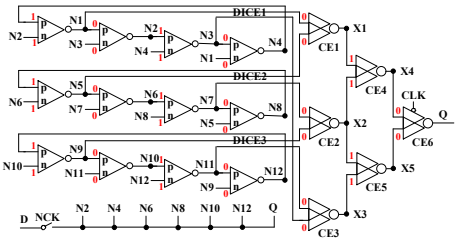

Fig. 4. The schematic of the proposed QNUTL latch.

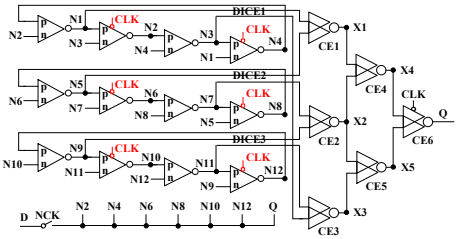

Fig. 5. The schematic of the proposed QNUTL-CG latch.

In hold mode, CLK = 0 and NCK = 1, and all the transistors in TGs are OFF. Thus, Q can be only driven by the signals of nodes X4 and X5 through CE6 instead of D. Since the internal nodes of each DICE are fed to each other, the feedback loops of each DICE can be properly constructed to hold stored values. Therefore, the proposed latch can properly store values, and can output the stored values through Q.

In the appendix, the QNU tolerance of the latch is discussed. It can be seen from the appendix that the proposed QNUTL latch design provides the complete QNU-tolerance. Obviously, the proposed QNUTL latch design provides the complete SNU, DNU, and TNU tolerance.

3.2 Simulation Results

The QNUTL latch design was implemented in an advanced and commercial 22nm CMOS technology from GlobalFoundries and extensive simulations using Synopsys HSPICE were performed. In the simulation, the supply voltage was set to 0.8V, the working temperature was set to room temperature, the PMOS transistors had the ratio W/L = 32/20nm, and the NMOS transistors had the ratio W/L = 22/20nm. Since Intel's 45nm process until recent 10nm nodes, gate lengths have been roughly constant around 20-35nm. So, this is why we assumed a

20nm gate-length in our work. Note that, the lighting marks in Figs. 6 and 7 denote the injected errors.

In the following SNU/DNU/TNU injection simulations, a controllable double exponential current source model was used as in [2, 16, 20]. The time constant of the rise and fall of the current pulse was set to be 0.1ps and 3.0ps, respectively. The worst case injected charge was chosen to be up to 45fC for a single node [16], which was large enough since the purpose was to validate the circuit operation under extreme SNU/DNU/TNU conditions

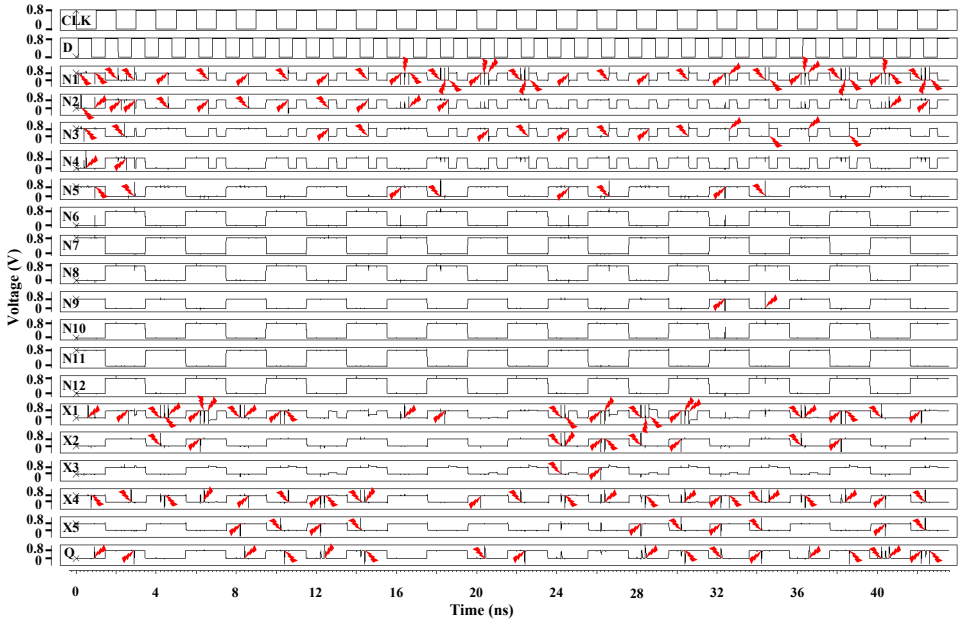

Fig. 6. Simulation results for the key SNU, DNU, and TNU injections of the QNUTL latch design.

TABLE 1
STATISTIC RESULTS FOR THE COMPLETE KEY SNU, DNU, AND TNU INJECTIONS OF THE QNUTL LATCH DESIGN ACCORDING TO FIG. 6.

Time (ns)	SNUs/DNUs /TNUs	State	Time (ns)	SNUs/DNUs /TNUs	State	Time (ns)	SNUs/DNUs /TNUs	State	Time (ns)	SNUs/DNUs /TNUs	State
0.1	N1	Q = 0	6.2	X1, X2	Q = 1	18.4	N1, X1	Q = 1	30.6	N1, N3, X1	Q = 1
0.2	N2	Q = 0	6.4	X1, X4	Q = 1	18.6	N1, N2	Q = 1	32.2	X4, X5, Q	Q = 0
0.4	N3	Q = 0	6.6	N1, N2, X1	Q = 1	20.2	N1, X4	Q = 0	32.4	N1, N5, N9	Q = 0
0.5	N4	Q = 0	8.2	X1, X5	Q = 0	20.4	N1, Q	Q = 0	32.6	N1, N3, X4	Q = 0
0.6	X1	Q = 0	8.4	X1, Q	Q = 0	20.6	N1, N3	Q = 0	34.2	X4, X5, Q	Q = 1
0.7	X4	Q = 0	8.6	N1, N2, X4	Q = 0	22.2	N1, X4	Q = 1	34.4	N1, N5, N9	Q = 1
0.8	Q	Q = 0	10.2	X1, X5	Q = 1	22.4	N1, Q	Q = 1	34.6	N1, N3, X4	Q = 1
0.9	N1, N2, N5	Q = 0	10.4	X1, Q	Q = 1	22.6	N1, N3	Q = 1	36.2	N1, X1, X2	Q = 0
2.1	N1	Q = 1	10.6	N1, N2, X4	Q = 1	24.2	X1, X2, X3	Q = 0	36.4	N1, X1, X4	Q = 0
2.2	N2	Q = 1	12.2	X4, X5	Q = 0	24.4	X1, X2, X4	Q = 0	36.6	N1, N3, Q	Q = 0
2.4	N3	Q = 1	12.4	X4, Q	Q = 0	24.6	N1, N3, N5	Q = 0	38.2	N1, X1, X2	Q = 1
2.5	N4	Q = 1	12.6	N1, N2, N3	Q = 0	26.2	X1, X2, X3	Q = 1	38.4	N1, X1, X4	Q = 1
2.6	X1	Q = 1	14.2	X4, X5	Q = 1	26.4	X1, X2, X4	Q = 1	38.6	N1, N3, Q	Q = 1
2.7	X4	Q = 1	14.4	X4, Q	Q = 1	26.6	N1, N3, N5	Q = 1	40.2	N1, X1, Q	Q = 0
2.8	Q	Q = 1	14.6	N1, N2, N3	Q = 1	28.2	X1, X2, X5	Q = 0	40.4	N1, X4, X5	Q = 0
2.9	N1, N2, N5	Q = 1	16.2	N1, N5	Q = 0	28.4	X1, X4, Q	Q = 0	40.6	N1, N2, Q	Q = 0
4.2	X1, X2	Q = 0	16.4	N1, X1	Q = 0	28.6	N1, N3, X1	Q = 0	42.2	N1, X1, Q	Q = 1
4.4	X1, X4	Q = 0	16.6	N1, N2	Q = 0	30.2	X1, X2, X5	Q = 1	42.4	N1, X4, X5	Q = 1
4.6	N1, N2, X1	Q = 0	18.2	N1, N5	Q = 1	30.4	X1, X4, Q	Q = 1	42.6	N1, N2, Q	Q = 1

that might disturb circuit nodes.

Fig. 6 shows the simulation results for the key SNU, DNU, and TNU injections of the QNUTL latch design. Table 1 shows statistic results for the complete key SNU, DNU, and TNU injections of the QNUTL latch design according to Fig. 6. In Table 1, "Time" denotes the injection time, "SNUs/DNUs/TNUs" denotes the injected SNUs, DNUs, or TNUs on the key nodes, and "State" denotes the correct state of Q. First, because of the symmetry construction of the latch, we need to consider the situations where seven indicative nodes N1, N2, N3, N4, X1, X4, and Q are affected by an SNU, respectively. As shown in Fig. 6, when Q = 0, an SNU was injected on nodes N1, N2, N3, N4, X1, X4, and Q at 0.1ns, 0.25ns, 0.4ns, 0.5ns, 0.6ns, 0.75ns, and 0.9ns, respectively. Note that, for the reverse states of the above nodes, SNU-injections were also performed. It can be seen that, the latch can tolerate these SNUs.

Here, DNUs are considered. Due to the symmetry construction of the latch, we only need to consider three possible DNU cases, i.e., D1 to D3 in the following.

Case D1: None of the nodes in all DICEs is affected by a DNU. The DNU only affects two nodes in the SIM. Therefore, we only need to consider six indicative key node-pairs, i.e., <X1, X2>, <X1, X4>, <X1, X5>, <X1, Q>, <X4, X5>, and <X4, Q> are affected by a DNU.

In the following D2 and D3 cases, all DICEs are equivalent for fault-tolerance, thus we only take DICE1 as an example to consider node-pairs.

Case D2: At most one node in each DICE is affected by a DNU. Due to the symmetric structure of the latch, <N1, N5>, <N1, X1>, <N1, X4>, and <N1, Q> are the indicative key node-pairs.

Case D3: At most two nodes in each DICE are affected by a DNU. Due to the symmetry structure of the latch, we only need to consider two indicative key node-pairs, i.e., <N1, N2> and <N1, N3> are affected by a DNU.

In Fig. 6, when Q = 0, a DNU was injected to key node-pairs <X1, X2>, <X1, X4>, <X1, X5>, <X1, Q>, <X4, X5>, <X4, Q>, <N1, N5>, <N1, X1>, <N1, N2>, <N1, X4>, <N1, Q>, and <N1, N2> at 4.2ns, 4.4ns, 8.2ns, 8.4ns, 12.2ns, 12.4ns, 16.2ns, 16.4ns, 16.6ns, 20.2ns, 20.4ns, and 20.6ns, respectively. Note that, for the reverse states of the above node-pairs, DNU-injections were also performed. It can be seen that, the latch can tolerate these DNUs.

Next, TNUs are considered. Due to the symmetry structure of the latch, we only need to consider four possible TNU cases, i.e., T1 to T4 in the following.

Case T1: None of the nodes in all DICEs is affected by a TNU. The TNU only affects three nodes in the SIM. Therefore, we only need to consider five indicative key node-lists, i.e., <X1, X2, X3>, <X1, X2, X4>, <X1, X2, X5>, <X1, X4, Q>, and <X4, X5, Q> are affected by a TNU.

Case T2: At most one node in each DICE are affected by a TNU. Due to the symmetric structure of the latch, we only need to consider five indicative key node-lists, i.e., <N1, N5, N9>, <N1, X1, X2>, <N1, X1, X4>, <N1, X1, Q>, and <N1, X4, X5> are affected by a TNU.

Case T3: At most two nodes in each DICE are affected by a TNU. Due to the symmetric structure of the latch, we only need to consider eight indicative key node-lists, i.e., <N1, N2, N5>, <N1, N2, X1>, <N1, N2, X4>, <N1, N2, Q>, <N1, N3, N5>, <N1, N3, X1>, <N1, N3, X4>, and <N1, N3, Q> are affected by a TNU.

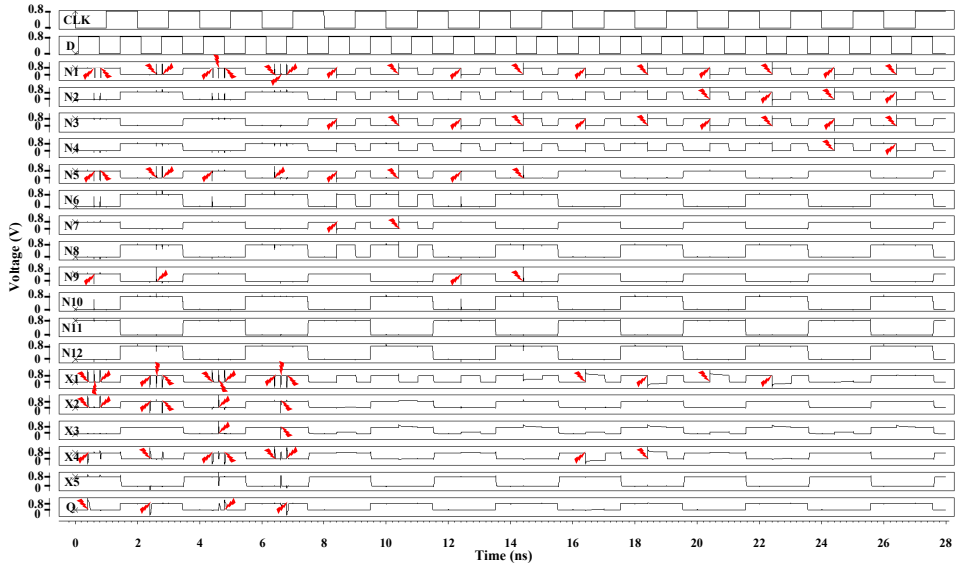

Fig. 7. Simulation results for the key QNU injections of the QNUTL latch design.

Case T4: At most three nodes in each DICE are affected by a TNU. Due to the symmetric structure of the latch, we need to consider one indicative key node-list <N1, N2, N3> that is affected by a TNU.

In Fig. 6, when Q = 0, a TNU was injected to key node-lists <N1, N2, N5>, <N1, N2, X1>, <N1, N2, X4>, <N1, N2, N3>, <X1, X2, X3>, <X1, X2, X4>, <N1, N3, N5>, <X1, X2, X5>, <X1, X4, Q>, <N1, N3, X1>, <X4, X5, Q>, <N1, N5, N9>, <N1, N3, X4>, <N1, X1, X2>, <N1, X1, X4>, <N1, N3, Q>, <N1, X1, Q>, <N1, X4, X5>, and <N1, N2, Q> at 0.93ns, 4.6ns, 8.6ns, 12.6ns, 24.2ns, 24.4ns, 24.6ns, 28.2ns, 28.4ns, 28.6ns, 32.2ns, 32.4ns, 32.6ns, 36.2ns, 36.4ns, 36.6ns, 40.2ns, 40.4ns, and 40.6ns, respectively. Note that, for the reverse states of the above node-lists, TNU-injections were also performed. It can be seen from Fig. 6 that the latch can tolerate these TNUs since Q can self-recover and/or still has its previous correct values. Therefore, the above injections/verifications results clearly demonstrate that the proposed QNUTL latch design can tolerate SNUs, DNUs, and TNUs.

Fig. 7 shows the simulation results for the key QNU injections of the QNUTL latch design. Note that statistic results for the QNU injections of the QNUTL latch design according to Fig. 7 is not shown for brevity. Based on the QNU discussions in the previous section, node-lists <X1, X2, X4, Q>, <N1, N5, N9, X1>, <N1, N5, X1, X2>, <N1, N5, X1, X4>, <N1, X1, X2, X3>, <N1, X1, X4, Q>, <N1, N3, N5, N7>, <N1, N3, N5, N9>, <N1, N3, X1, X4>, <N1, N2, N3, X1>, and <N1, N2, N3, N4> were considered for QNU injections, respectively. In Fig. 7, when Q = 0, a QNU was injected to the above node-lists at 0.4ns, 0.6ns, 0.8ns, 4.4ns, 4.6ns, 4.8ns, 8.4ns, 12.4ns, 16.4ns, 20.4ns, and 24.4ns, respectively. Note that, for the reverse states of the above node-lists, QNU-injections were also performed. It can be seen from Fig. 7 that the latch can tolerate the injected QNUs since Q can self-recover and/or still has its previous correct values. It can be also seen from Fig. 7 that, after 8ns, the latch suffers from some worse cases where it cannot self-recover from QNUs especially for the affected nodes N1, N2, N3, N4, N7, X1, and X4. However, the output of the latch still has its previous correct values for these cases. Therefore, the above injections/verifications results clearly demonstrate that the proposed QNUTL latch design can tolerate QNUs.

In summary, all the above discussions show that the proposed QNUTL latch design can provide the complete SNU, DNU, TNU, and QNU tolerance, thus providing very high reliability for reliable computing of safety-critical applications, especially in harsh radiative environments.

4 Evaluation and Comparison Results

For fair comparisons, the existing hardened latch designs reviewed in Section 2, i.e., the FERST [12], HRLC [13], DIRT [14], HRCE [15], LCTNUT [16], DICE4TNU [17], and TNUTL [3] designs, including DICE [29] and our proposed QNUTL and QNUTL-CG latch designs were implemented with the same parameters listed in Section 3.2.

TABLE 2
Reliability Comparisons Among the SNU, DNU, TNU, and/or QNU Hardened Latches

Latch	Ref.	SNU Tolerant	DNU Tolerant	TNU Tolerant	QNU Tolerant
DICE	[29]	√	×	×	×
FERST	[12]	√	×	×	×
HRLC	[13]	√	×	×	×
DIRT	[14]	√	√	×	×
HRCE	[15]	√	√	×	×
LCTNUT	[16]	√	√	√	×
DICE4TNU	[17]	√	√	√	×
TNUTL	[3]	√	√	√	×
QNUTL	Proposed	√	√	√	√
QNUTL-CG	Proposed	√	√	√	√

Table 2 shows the reliability comparison results among the SNU, DNU, TNU, and/or QNU hardened latches. It can be seen that the DICE, FERST and HRLC latches are SNU-tolerant. However, they cannot provide complete DNU-tolerance. The DIRT latch and the HRCE latch are not only SNU-tolerant but also DNU-tolerant. However, they cannot provide complete TNU-tolerance. The LCTNUT, DICE4TNU, and TNUTL latches can provide SNU, DNU, and TNU tolerance. However, they cannot provide complete QNU-tolerance. From Table 2, it can be seen that only the proposed QNUTL and QNUTL-CG latch designs can simultaneously provide SNU, DNU, TNU, and QNU tolerance. In other words, the proposed QNUTL and QNUTL-CG latch designs can provide the highest reliability simultaneously protected against SNUs, DNUs, TNUs, and QNUs.

TABLE 3
Overhead Comparisons Among the SNU, DNU, TNU, and/or QNU Hardened Latches

Latch	Area (μm·)	D-Q Delay (ps)	CLK-Q Delay (ps)	Setup Time (ps)	Power (μW)
DICE	2.06	4.37	4.33	3.91	0.62
FERST	3.61	50.78	50.07	11.18	1.05
HRLC	3.36	27.12	26.95	6.68	1.76
DIRT	4.95	3.44	3.27	5.69	3.15
HRCE	7.22	2.48	2.34	12.91	3.41
LCTNUT	6.29	1.19	1.11	3.96	1.38
DICE4TNU	6.71	1.20	1.08	12.73	4.17
TNUTL	10.63	71.74	71.06	13.48	1.71
QNUTL	8.30	1.43	1.37	7.26	3.31
QNUTL-CG	9.84	1.43	1.37	3.90	2.09

Table 3 shows the overhead comparison results among the SNU, DNU, TNU, and/or QNU hardened latches. In Table 3, "Area" means the silicon area measured through layout, "D-Q Delay" means the average of the transmission delays (rise and fall) from D to Q, "CLK-Q Delay"

means the average of the transmission delays (rise and fall) from CLK to Q, "Setup Time" means the minimum amount of time during which the input is held steady before a CLK event, and "Power" means the average of the power dissipation (dynamic and static). Note that, we used a prior and tail latch (forming a latch chain) to load capacitances for each latch.

It can be seen from Table 3 that, for silicon area overhead, compared with the DICE, FERST, HRLC, DIRT, HRCE, LCTNUT and DICE4TNU latches, the TNUTL latch and the proposed QNUTL and QNUTL-CG latch designs require more area since they use redundant transistors to achieve very high reliability. However, compared with the state-of-the-art TNUTL latch that cannot provide complete QNU-tolerance, the proposed QNUTL and QNUTL-CG latches consume less area and can additionally provide complete QNU-tolerance.

For the proposed QNUTL and QNUTL-CG latches and some existing hardened latches such as DIRT, HRCE, LCTNUT, and DICE4TNU, their D-Q delay is small, since there is a high-speed transmission path from D to Q for any of them. Conversely, the latches such as the FERST, HRLC, and TNUTL have a large D-Q delay mainly due to the use of too many devices from D to Q for any of them.

It can be seen from Table 3 that the CLK-Q delay of each latch is comparable to its D-Q delay since the average of the transmission delays (rise and fall) from CLK to Q is close to that of the transmission delays (rise and fall) from D to Q. Moreover, due to the intrinsic structure of the latches, such as the DICE, HRLC, DIRT, LCTNUT, QNUTL, and QNUTL-CG, they only need a small amount of time during which the input is held steady before a CLK event, thus making that their setup time is small.

In the existing hardened latch designs, the DICE4TNU latch consumes the highest power dissipation, since the latch has too many feedback loops and current competion to ensure complete TNU-tolerance. Note that, when a latch has a large area and/or does not use the CG technique, its power consumption is large. Clearly, since the QNUTL latch uses redundant silicon area and does not use the CG technique to firstly achieve complete QNU-tolerance, it may consume large power. In the existing hardened latch designs, the DICE, FERST and HRLC latches have less power dissipation, mainly since the silicon area of them is small. The LCTNUT, TNUTL, and QNUTL-CG latches use more area. However, due to the use of the CG technology, they have lower power dissipation.

Moreover, compared with the state-of-the-art TNUTL latch, the quantitative comparisons in terms of overhead for our proposed latches can be calculated from Table 3. That is, compared with the TNUTL latch, our proposed QNUTL latch can save 21.92% area, 98.00% D-Q delay, 98.07% CLK-Q delay, 46.14% setup time, and -94.12% power. As for our proposed QNUTL-CG latch, compared with the TNUTL latch, ours can save 7.43% area, 98.00% D-Q delay, 98.07% CLK-Q delay, 71.07% setup time, and -22.22% power. Meanwhile, compared with the LCTNUL and DICE4TNU latches, our proposed latches have to consume indispensable overhead especially for area, D-Q delay and CLK-Q delay. However, these compared latches cannot provide QNU-toleration at all.

In summary, the proposed QNUTL and QNUTL-CG latches are the first to provide the complete QNU-tolerance at the cost of indispensable and moderate overhead. However, compared with the proposed QNUTL latch, the proposed QNUTL-CG latch is cost-effective, especially in terms of setup time and power dissipation.

5 Conclusions

In nano-scale CMOS technologies, due to the aggressive reduction of transistor feature sizes in integrated circuits and systems, the advanced safety-critical applications, especially those in harsh radioactive environments, are more and more likely to suffer from MNUs that include TNUs and even QNUs. This paper has, for the first time, proposed a novel and completely QNU-tolerant latch (namely QNUTL) as well as its advanced version (namely QNUTL-CG), simultaneously protected against soft errors, such as SNUs, DNUs, TNUs, and QNUs. The latches mainly consist of three independent DICEs and a triple-level SIM. The two non-adjacent nodes of each DICE are used as the inputs of the SIM, and the SIM can intercept soft-errors in the triple-level manner, making the proposed QNUTL and QNUTL-CG latches provide the complete SNU, DNU, TNU, and QNU tolerance. Compared with the QNUTL latch, the setup time and power overhead of the QNUTL-CG latch is effectively reduced by replacing the DICEs with the CG based ones. Simulation results have demonstrated the complete SNU, DNU, TNU, and QNU tolerance of the proposed latches. Moreover, the proposed QNUTL and QNUTL-CG latches have low overhead in terms of area, D-Q delay, CLK-Q delay, and setup time, compared with the state-of-the-art TNUTL latch that cannot provide complete QNU-tolerance.

Appendix

This part introduces QNU tolerance of the latch. Due to the symmetric structure of the latch, we only need to consider five possible cases, i.e., Q1 to Q5 in the following.

Case Q1: None of the nodes in all DICEs is affected by a QNU. Instead, the QNU only affects four nodes in the SIM, and <X1, X2, X4, Q> is an indicative node-list.

When <X1, X2, X4, Q> is affected by a QNU, the temporary flips of X1, X2, and X4 can firstly self-recover through DICEs that are not affected by the QNU. Thus, the temporary flip of Q can self-recover through X4 and X5 of CE6. Therefore, <X1, X2, X4, Q> can self-recover from the QNU. In other words, the latch can self-recover from QNUs for Case Q1.

Case Q2: At most one node in each DICE is affected by a QNU. Due to the symmetric structure of the latch, the main indicative key node-lists are < N1, N5, N9, X1>, <N1, N5, X1, X2>, <N1, N5, X1, X4>, <N1, X1, X2, X3>, and <N1, X1, X4, Q>.

When <N1, N5, N9, X1> is affected by a QNU, due to the SNU self-recoverability of DICEs, N1, N5, and N9 can

firstly self-recover. Thus, the correct values on nodes N1 and N5 can still feed CE1, and X1 can self-recover. Clearly, <N1, N5, N9, X1> can self-recover from the QNU. In a similar manner, <N1, N5, X1, X2>, <N1, N5, X1, X4>, <N1, X1, X2, X3>, and <N1, X1, X4, Q> can self-recover from QNUs since the values stored in DICEs can be still correct, and then Case Q2 becomes equal to Case Q1. Therefore, all these indicative key node-lists can self-recover from QNUs. In other words, the latch can self-recover from QNUs for Case Q2.

Case Q3: At most two nodes in each DICE are affected by a QNU. In this case, all DICEs are equivalent for fault-tolerance, thus we take the scenario that two nodes in DICE1 and/or DICE2 are affected as examples to illustrate the fault-tolerance principle for this case. The indicative key node-lists are <N1, N3, N5, N7>, <N1, N3, N5, N9>, and <N1, N3, X1, X4>.

When <N1, N3, N5, N7> is affected by a QNU, N1, N3, N5, and N7 will be flipped since DICEs cannot provide self-recoverability from DNUs for non-adjacent nodes. Thus, N1, N3, N5, and N7 cannot self-recover. Subsequently, X1 is affected by N1 and N5 through CE1. However, since one input node N9 of CE2 is correct, X2 can still have its previous correct value. Similarly, X3 can still have its previous correct value. Clearly, one input node X2 of CE4 is still correct, thus X4 can still have its previous correct value. Clearly, the inputs of CE5 are still correct, thus X5 can still have its previous correct value. By this way, the inputs of CE6 are still correct, thus Q can still have its previous correct value. Therefore, <N1, N3, N5, N7> can tolerate the QNU.

When <N1, N3, N5, N9> is affected by a QNU, similarly, N1 and N3 will be flipped since a DICE cannot provide self-recoverability from DNUs for non-adjacent nodes. Thus, N1 and N3 cannot self-recover. However, DICEs can self-recover from SNUs, thus N5 and N9 can respectively self-recover. Clearly, one input node N5 of CE1 is still correct, thus X1 can still have its previous correct value. Similarly, the inputs of CE2 are still correct, thus X2 can still have its previous correct value. Finally, one input node N11 of CE3 is correct, thus X3 can still have its previous correct value. Hence, the inputs of CE4 are still correct, and X4 can still have its previous correct value. Similarly, X5 can still have its previous correct value. Since the inputs of CE6 are correct, Q can still have its previous correct value. Therefore, <N1, N3, N5, N9> can tolerate the QNU.

When <N1, N3, X1, X4> is affected by a QNU, similarly, N1 and N3 cannot self-recover. Clearly, one input node N1 of CE1 is flipped. Meanwhile, X1 is directly affected by the QNU. Thus, one input and the output of CE1 are simultaneously affected, and X1 has to retain the wrong value. Since the inputs of CE2 are still correct, X2 can still have its previous correct value. Since one input node N3 of CE3 is flipped, the output node X3 of CE3 can still have its previous correct value. Clearly, one input node X1 of CE4 is flipped. Meanwhile, X4 is directly affected by a QNU. Thus, one input and the output of CE4 are simultaneously affected, and X4 will retain the wrong value. However, since the inputs of CE5 are correct, the output node X5 of CE5 is still correct. Since one input node X4 of CE6 is flipped, the output node Q of CE6 can still have its previous correct value. Therefore, <N1, N3, X1, X4> can tolerate the QNU. It can be seen that all these indicative key node-lists can tolerate QNUs. In other words, the latch can tolerate QNUs for Case Q3.

Case Q4: At most three nodes in a DICE are affected by a QNU. In this case, all DICEs are equivalent for fault-tolerance, thus we take DICE1 together with the SIM as an example to illustrate the fault-tolerance principle for this case. Therefore, we only need to consider one indicative node-list <N1, N2, N3, X1> that is affected by a QNU.

When <N1, N2, N3, X1> is affected by a QNU, N1, N2, and N3 will be flipped since a DICE cannot provide self-recoverability from TNUs. Clearly, one input node N1 of CE1 is flipped. Meanwhile, X1 is directly affected by a QNU. Thus, one input and the output of CE1 are simultaneously affected, and X1 will retain the wrong value. Since the inputs of CE2 are correct, X2 can still have its previous correct value. Since one input node N3 of CE3 is flipped, the output node X3 of CE3 can still have its previous correct value. Since one input node X1 of CE4 is flipped, the output node X4 of CE4 can still have its previous correct value. Since the inputs of CE5 are still correct, X5 can still have its previous correct value. Since the inputs of CE6 are still correct, Q can still have its previous correct value. Therefore, <N1, N2, N3, X1> can tolerate the QNU. In other words, the latch can tolerate QNUs for Case Q4.

Case Q5: At most four nodes in a DICE are affected by a QNU. We still take DICE1 as an example to explain the QNU-tolerance. Clearly, we only need to consider one node-list <N1, N2, N3, N4> that is affected by a QNU.

When <N1, N2, N3, N4> is affected by a QNU, N1, N2, N3, and N4 will be flipped since a DICE cannot provide self-recoverability from QNUs. Clearly, one input node N1 of CE1 is flipped, thus the output node X1 of CE1 can still have its previous correct value. Similarly, X3 can still have its previous correct value. Since the inputs of CE2 are correct, X2 can still have its previous correct value. Similarly, X4 and X5 are still correct. Since the inputs of CE6 are still correct, Q can still have its previous correct value. Therefore, <N1, N2, N3, N4> can tolerate the QNU. In other words, the latch can tolerate QNUs for Case Q5.

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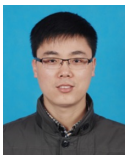

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