Novel Speed-and-Power-Optimized SRAM Cell Designs With Enhanced Self-Recoverability From Single- and Double-Node Upsets

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***Abstract*—The continuous advancement of CMOS technologies makes SRAMs more and more sensitive to soft errors. This paper presents two novel radiation-hardened SRAM cell designs, namely S4P8N and S8P4N, with enhanced self-recoverability from single-node upsets (SNUs) and Double-node upsets (DNUs). First, the S4P8N cell that has more redundant nodes and more access transistors is proposed. The cell has the following advantages: (1) it can self-recover from all possible SNUs; (2) it can self-recover from a part of DNUs; (3) it has small overhead in terms of power dissipation. Then, to reduce read and write access time, the S8P4N cell that uses a special feedback mechanism among its internal nodes is proposed. The cell has similar soft error tolerability as the S4P8N cell. Simulation results validate the high robustness of the proposed SRAM cells. These results also show that the write access time, read access time, and power dissipation of the S8P4N cell are reduced approximately by 29%, 20%, and 21% on average, at the cost of moderate silicon area, when compared with the state-of-the-art radiation-hardened SRAM cells.**

***Index Terms*—SRAM; radiation hardening; soft error; self-recoverability; node upset**

I. Introduction

As CMOS technology scaling, SRAMs can achieve high density, low power consumption and high performance. However, this pushes *integrated circuit* (*IC*) designers and technologists to increasingly focus on SRAM reliability, since small transistor feature sizes also give rise to low supply voltages and small node capacitances that can increase the sensitivity of SRAMs to particle-striking-induced soft errors [1]. It is reported in [2] that high-energy particles, such as protons, neutrons, heavy ions, electrons, muons and alpha particles, including kinds of rays, can severely impact the reliability of advanced nano-scale SRAMs. That is, soft errors can invalidly change the values stored in SRAMs. Although the recently adopted FinFET technology can reduce the soft error rate at transistor or cell level [3], effective and scalable solutions for soft error tolerance are still needed. Therefore, there is a strong need for IC designers to mitigate soft-error-induced reliability issues through designing novel radiation-hardened structures.

When a particle strikes an OFF-state transistor in a logic gate, a dense track of electron-hole pairs can be generated. As a result, a transient pulse, i.e., a *single event transient* (*SET*) pulse, can be produced at the node that collects the charge and the transient pulse can be detected at the output of the affected logic gate. If the SET pulse propagates through downstream combinational logic gates and arrives at a storage element, the pulse may be captured and causes invalid value-retention in the storage element [4]. In the same context, a particle may directly strike an OFF-state transistor in a storage element, causing a node-value change, which is called a *single node upset* (*SNU*). Moreover, transistor feature sizes are becoming smaller and smaller, leading to reduced spacing between nodes. Hence, in a circuit, both OFF-state transistors may be affected by one striking-particle simultaneously because of multiple-node charge-collection mechanisms [5], and thus a *double-node upset* (*DNU*) may occur. In summary, SRAMs may store incorrect values because of SNUs and/or DNUs especially for advanced nano-scale CMOS technologies, resulting in an increasing challenge for IC designers to mitigate reliability issues.

To mitigate SNUs and/or DNUs, IC designers have proposed several novel designs of latches [6-8], flip-flops [9-11] and SRAMs [3, 12-28] through the *radiation hardening by design* (*RHBD*) approach. This paper mainly considers hardening for SRAMs. The conventional SRAM, namely 6T, consists of six transistors, i.e., it includes two PMOS transistors and two NMOS transistors to store values and two NMOS transistors for access operations. Since the 6T SRAM cannot tolerate SNUs, many hardened SRAMs have been proposed to tolerate SNUs. Typical SNU-hardened SRAMs include NASA13T [13], QUCCE10T [14], QUCCE12T [14], We-Quatro [15], PS10T [16], Lin12T [17], and RH12T [18].

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However, these SRAMs still have the following disadvantages.

(1) Some SRAMs cannot provide complete SNU self-recoverability [13-15].

(2) Some SRAMs have large overhead especially in terms of read access time [14, 16-18], write access time [14, 16] and power dissipation [13, 14].

(3) To mitigate SNUs, some SRAMs have to use extra techniques such as sizing up some transistors [13], identifying sensitive and insensitive nodes [14]. These solutions increase the area overhead and design complexity.

Our previous work in [19] has very large overhead; our previous work in [12] has at least one node that cannot self-recover from an SNU; these issues motivate us to propose SRAM cells that have low overhead but advanced self-recoverability. Based on the RHBD approach, this paper first presents a novel reliable SRAM cell whose storage part includes 4 PMOS and 8 NMOS transistors (namely S4P8N cell) hardened against SNUs and DNUs. Due to the elaborately constructed error-interceptive feedback loops, the cell can self-recover from all possible SNUs and a part of DNUs regardless of the energy of striking-particles. To reduce read and write access time, an access-operation optimized SRAM cell whose storage part includes 8 PMOS and 4 NMOS transistors (namely S8P4N cell) is further proposed. The cell has a similar soft error tolerance capability as the S4P8N cell. Moreover, owing to the use of special feedback mechanisms among internal nodes, the proposed cells have low power dissipation. Indeed, each of the cells has two interlocked feedback loops. So, there is no current competition inside (and between) the feedback loops. Moreover, the feedback loops are complementary since, as soon as one feedback loop is activated, the other feedback loop will be also activated. Simulation results demonstrate the reliability and cost-effectiveness of the proposed SRAM cells.

The rest of this paper is organized as follows. Section II presents the schematic and working principles of the proposed S4P8N cell. Section III presents the schematic and working principles of the proposed S8P4N cell. Section IV provides comparison and evaluation results about reliability and overhead for SRAM cells, and Section V concludes the paper.

It should be noted that, for fault injection simulations in the subsequent sections, a flexible dual-exponential current-source model was used [29]. In the simulations, the time constant of the rise and fall of the current pulse was set to 0.1 and 3.0 ps, respectively. The worst case injected charge was chosen to be up to 25fC for a single node, which was large enough. All the simulations of the proposed S4P8N and S8P4N cells were performed using the Synopsys HSPICE tool, with an advanced 22nm CMOS library from GlobalFoundries under room temperature, and the supply voltage was set to 0.8V.

II. Proposed S4P8N SRAM Cell

Figure 1 shows a conceptual view of the proposed SRAMs to enhance self-recoverability from SNUs and DNUs and improve read-access and write-access times. We use two interlocked one-PMOS-transistor-and-one-NMOS-transistor (1P1N) storage blocks (feedback loops) to store values and use

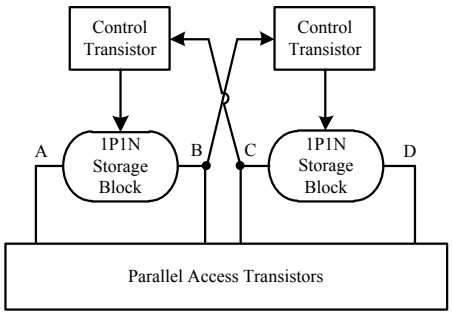

Fig. 1. Conceptual view of the proposed SRAM cells.

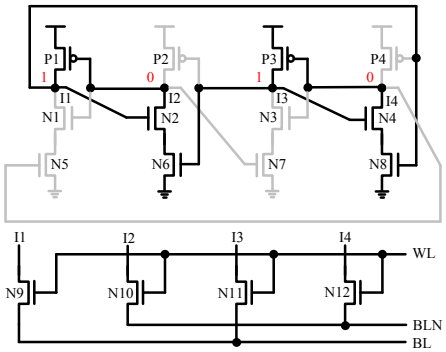

Fig. 2. Schematic of the proposed S4P8N cell.

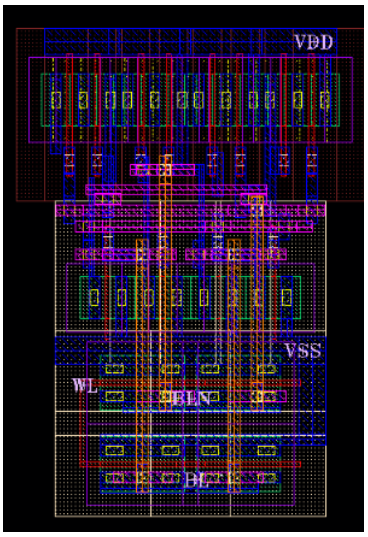

Fig. 3. Layout of the proposed S4P8N cell.

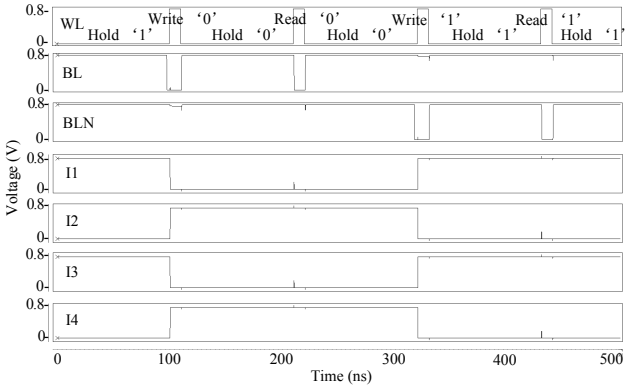

Fig. 4. Simulation results for normal operations of the proposed S4P8N cell.

parallel access transistors to improve access operation. To enhance self-recoverability from SNUs and DNUs, one of the blocks is controlled by the other through a control transistor. The fact that there is no current competition inside (and between) the blocks can also improve access operation. The schematic of the proposed S4P8N cell is depicted in Fig. 2. The S4P8N cell consists of 16 transistors, i.e., PMOS transistors P1 to P4 and NMOS transistors N1 to N12. The storage part of the cell has 4 PMOS transistors and 8 NMOS transistors, i.e., transistors P1 to P4 and N1 to N8. Transistors N9 to N12 are access transistors that are controlled by word line WL. In the proposed S4P8N cell, I1 to I4 are internal nodes and they are connected to bit lines BL and BLN through access transistors N9 to N12, respectively. Figure 3 shows the layout of the proposed S4P8N cell. When WL = 1, all access transistors are ON, and write/read access operations can be executed. When WL = 0, the access transistors are OFF, and the cell retains the stored value.

The normal operations of the proposed S4P8N cell are described as follows. Figure 2 shows the scenario when the S4P8N cell stores 1, i.e., I1 = I3 = 1 and I2 = I4 = 0.

(1) We consider the case of writing 1. At this time, BL is high while BLN is low. When WL is changed to 1, transistors P1, P3, N2, N4, N6, and N8 become ON and transistors P2, P4, N1, N3, N5, and N7 become OFF, and a 1 is written into the S4P8N cell. Since feedback loops are constructed in the S4P8N cell, the cell can retain the value through the feedback loops (i.e., I1 → I4 → I3 → I2 → I1, I2 → I1 → I2, and I3 → I4 → I3).

(2) The hold operation is considered when storing 1. At this time, WL = 0, transistors P1, P3, N2, N4, N6, and N8 are ON while the other transistors are OFF. Hence, the node states of the S4P8N cell are retained due to the constructed feedback loops.

(3) We consider the case of reading 1. Before the read operation, bit lines BL and BLN need to be pre-charged to supply voltage. When WL = 1, the operation of reading 1 from the S4P8N cell is executed. Since transistors N2, N4, N6, and N8 are ON, the voltage of BLN decreases while the voltage of BL does not change. Once the differential sense amplifier detects that the voltage difference between BL and BLN is at a specified constant value, the value stored in the S4P8N cell is successfully read out.

For writing/holding/reading 0, a similar scenario can be observed. Figure 4 shows the simulation results for normal operations of the S4P8N cell. It can be seen from Fig. 4 that a series of "write 0","hold 0", "read 0", "write 1", "hold 1", and "read 1" operations were correctly executed and the written values were correctly retained in the S4P8N cell.

The fault-tolerance principles of the proposed S4P8N cell are described in the following. Here, we still consider the case where the cell stores 1 (i.e., I1 = I3 = 1 and I2 = I4 = 0) for illustration purpose. First, we discuss the SNU self-recovery principle of the proposed S4P8N cell.

A. SNU Self-Recovery Principle

The SNU self-recovery principle is provided according to the state shown in Fig. 2. First, we consider the case where I1 is affected by an SNU. When I1 is temporarily changed to 0 from the original value of 1 due to the SNU, N2 becomes OFF. At this time, the SNU is intercepted by N2. Thus, I2 is not affected (I2 = 0) and N7 remains OFF. Since I3 is also not affected (I3 = 1), N4 remains ON. At the same time, the fact that I1 temporarily changes to 0 from the original value of 1 can cause P4 to be ON and N8 to be OFF temporarily. As a result, I4 is changed to 1 from the original value of 0 temporarily and N5 is ON. On the other hand, since I2 is not affected (I2 = 0), P1 remains ON and N1 remains OFF, making I1 = 1. Therefore, I1 can self-recover from the SNU. Note that, when I3 is affected by an SNU, i.e., I3 is temporarily changed to 0 from 1, the similar SNU self-recovery principle can be observed.

Next, we consider the case where I2 is affected by an SNU. When I2 is temporarily changed to 1 from the original value of 0 due to the SNU, P1 becomes OFF and N1 and N7 become ON. At this time, I4 is not affected by the SNU, it still has the original value (I4 = 0), and hence N3 and N5 remain OFF and P3 remains ON. Thus, I1 and I3 keep their original values (i.e., I1 = 1 and I3 = 1). Since I1 = 1 and I3 = 1, P2 and P4 become OFF and N2, N4, N6, and N8 become ON. Thus, I2 can self-recover from the SNU. Note that, when I4 is affected by an SNU, i.e., I4 is temporarily changed to 1 from 0, the similar SNU self-recovery principle can be observed.

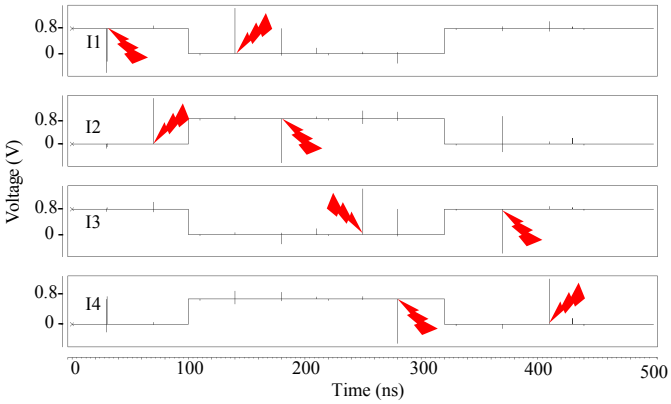

Fig. 5. Simulation results for SNU self-recovery of the proposed S4P8N cell.

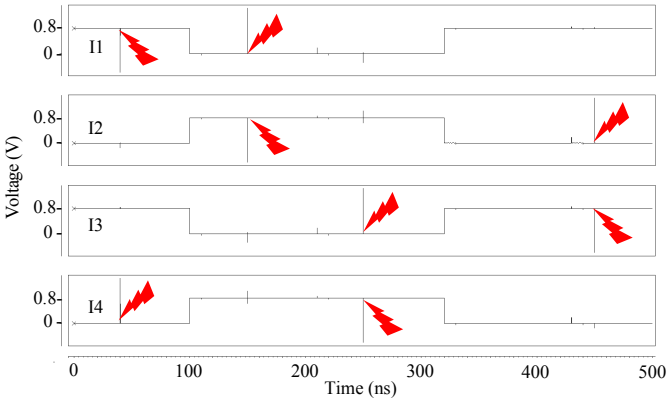

Fig. 6. Simulation results for DNU tolerance of the proposed S4P8N cell.

In the case of 0 being stored in the cell, it can be concluded from analysis and simulation that the cell can also self-recover

from any SNU. We consider the case where I1 is affected by an SNU. When I1 is temporarily changed to 1 from the original value of 0 due to the SNU, P4 becomes OFF and N2 and N8 become ON. At this time, I3 is not affected by the SNU, and it still has the original value (I3 = 1). Hence, N4 and N6 remain ON and P2 remains OFF. Thus, I2 and I4 keep their original values (i.e., I2 = 0 and I4 = 0). Since I2 = 0 and I4 = 0, P1 and P3 become ON and N1, N3, N5, and N7 become OFF. Thus, I1 can self-recover from the SNU. Note that, when I3 is affected by an SNU, i.e., I3 is temporarily changed to 1 from 0, the similar SNU self-recovery principle can be observed.

Next, we consider the case where I2 is affected by an SNU. When I2 is temporarily changed to 0 from the original value of 1 due to the SNU, N7 becomes OFF. At this time, the SNU is intercepted by N7. Thus, I3 is not affected (I3 = 0) and N4 remains OFF. Since I4 is also not affected (I4 = 1), N5 remains ON. At the same time, the fact that I2 temporarily changes to 0 from the original value of 1 can cause P1 to be ON and N1 to be OFF temporarily. As a result, I1 is changed to 1 from the original value of 0 temporarily and N2 is ON. On the other hand, since I3 is not affected (I3 = 0), P2 remains ON and N6 remains OFF, making I2 = 1. Therefore, I2 can self-recover from the SNU. Note that, when I4 is affected by an SNU, i.e., I4 is temporarily changed to 0 from 1, the similar SNU self-recovery principle can be observed.

The simulation results for SNU self-recovery on nodes I1 to I4 of the proposed S4P8N cell are shown in Fig. 5. In the case of 1 being stored (I1 = 1), SNUs were injected to nodes I1 to I4 between 0 and 100 ns and between 350 and 450 ns, respectively. In the case of 0 being stored (I1 = 0), SNUs were injected to nodes I1 to I4 between 100 and 300 ns, respectively. From Fig. 5, it can be seen that the proposed S4P8N cell can self-recover from all possible SNUs.

B. DNU-Tolerance Principle

Let us now consider the DNU tolerance principle of the proposed S4P8N cell. The key node-pairs are <I1, I2>, <I1, I3>, <I1, I4>, <I2, I3>, <I2, I4> and <I3, I4>. We first describe the case where the S4P8N cell stores 1.

First, we consider the case where <I1, I4> is affected by a DNU, i.e., I1 is temporarily changed to 0 from the original value of 1 and I4 is temporarily changed to 1 from the original value of 0. Thus, N2 becomes temporarily OFF and N5 becomes temporarily ON. Since I2 is not directly affected (I2 = 0), P1 remains ON and N1 remains OFF. As a result, I1 = 1, P4 becomes OFF, and N8 becomes ON. Since I3 is also not directly affected (I3 = 1), N4 remains ON. Finally, all nodes and transistors can return to their original states. In other words, <I1, I4> of the proposed S4P8N cell can self-recover from the DNU.

Second, we consider the case where <I2, I3> is affected by a DNU, i.e., I2 is temporarily changed to 1 from the original value of 0 and I3 is temporarily changed to 0 from the original value of 1. Thus, N4 becomes temporarily OFF and N7 becomes temporarily ON. Since I4 is not directly affected (I4 = 0), P3 remains ON and N3 remains OFF. As a result, I3 = 1, P2 becomes OFF, and N6 becomes ON. Since I1 is also not directly affected (I1 = 1), N2 remains ON. Finally, all nodes and transistors can return to their original states. In other words, <I2, I3> of the proposed S4P8N cell can self-recover from the DNU.

Finally, we consider the case where <I1, I2> is affected by a DNU, i.e., I1 is temporarily changed to 0 from the original value of 1 and I2 is temporarily changed to 1 from the original value of 0. Thus, N2 becomes temporarily OFF and N7 becomes temporarily ON. When I1 is changed to 0, P4 is ON and N8 is OFF. Thus, I4 gets an invalid value (I4 = 1). As a result, P3 becomes OFF and N3 becomes ON. Since N7 is ON as mentioned above, I3 gets an invalid value (I3 = 0). Consequently, all nodes and transistors cannot return to their original states. In other words, the proposed S4P8N cell cannot tolerate the DNU on <I1, I2>. Note that, when the other node pairs of the cell suffer from a DNU, similar results can be observed.

To summarize, when the proposed S4P8N cell stores 1, node pairs <I2, I3> and <I1, I4> of the cell can self-recover from a DNU, but the other node pairs of the cell cannot self-recover from a DNU. Next, we discuss the case of 0 being stored in the proposed S4P8N cell.

First, we consider the case where <I1, I2> is affected by a DNU, i.e., I1 is temporarily changed to 1 from the original value of 0 and I2 is temporarily changed to 0 from the original value of 1. Thus, N2 becomes temporarily ON and N7 becomes temporarily OFF. Since I3 is not directly affected (I3 = 0), P2 remains ON and N6 remains OFF. As a result, I2 = 1, P1 becomes OFF, and N1 becomes ON. Since I4 is also not directly affected (I4 = 1), N5 remains ON. Finally, all nodes and transistors can return to their original states. In other words, <I1, I2> of the proposed S4P8N cell can self-recover from the DNU.

Second, we consider the case where <I3, I4> is affected by a DNU, i.e., I3 is temporarily changed to 1 from the original value of 0 and I4 is temporarily changed to 0 from the original value of 1. Thus, N4 becomes temporarily ON and N5 becomes temporarily OFF. Since I1 is not directly affected (I1 = 0), P4 remains ON and N8 remains OFF. As a result, I4 = 1, P3 becomes OFF, and N3 becomes ON. Since I2 is also not directly affected (I2 = 1), N7 remains ON. Finally, all nodes and transistors can return to their original states. In other words, <I3, I4> of the proposed S4P8N cell can self-recover from the DNU.

Finally, we consider the case where <I2, I3> is affected by a DNU, i.e., I2 is temporarily changed to 0 from the original value of 1 and I3 is temporarily changed to 1 from the original value of 0. Thus, N7 becomes temporarily OFF and N4 becomes temporarily ON. When I2 is changed to 0, P1 is ON and N1 is OFF. Thus, I1 gets an invalid value (I1 = 1). As a result, P4 becomes OFF and N8 becomes ON. Since N4 is ON as mentioned above, I4 gets an invalid value (I4 = 0). Finally, all nodes and transistors cannot return to their original states. In other words, the proposed S4P8N cell cannot tolerate the DNU on <I2, I3>. Note that, when the other node pairs of the cell suffer from a DNU, similar results can be observed.

To summarize, when the proposed S4P8N cell stores 0, node pairs <I1, I2> and <I3, I4> of the cell can self-recover from a DNU, but the other node pairs of the cell cannot self-recover from a DNU.

Figure 6 shows the simulation results for DNU self-recovery of node pairs <I1, I4>, <I1, I2>, <I3, I4>, and <I2, I3> of the proposed S4P8N cell. In the case of 1 being stored (I1 = 1), DNUs were injected to node pairs <I1, I4> and <I2, I3> between 0 and 100 ns and between 400 to 500 ns, respectively. In the case of 0 being stored (I1 = 0), DNUs were injected to node pairs <I1, I2> and <I3, I4> between 100 and 300 ns, respectively. From Fig. 6, it can be concluded that the proposed S4P8N cell can self-recover from DNUs on node pairs <I1, I4> and <I2, I3> when storing 1 and the proposed S4P8N cell can self-recover from DNUs on node pairs <I1, I2> and <I3, I4> when storing 0 (totally four node-pairs are DNU-self-recoverable).

III. Proposed S8P4N SRAM Cell

Figure 7 shows the schematic of the proposed S8P4N cell. It can be seen from Fig. 7 that the S8P4N cell consists of 16 transistors, i.e., PMOS transistors P1 to P8 and NMOS transistors N1 to N8. The storage part of the cell has 8 PMOS transistors and 4 NMOS transistors, i.e., transistors P1 to P8 and N1 to N4. Transistors N5 to N8 are used for access operations and their gate terminals are connected to word-line WL. In the proposed S8P4N cell, I1 to I4 are internal nodes and they are connected to bit lines BL and BLN through access transistors N5 to N8, respectively. Figure 8 shows the layout of the proposed S8P4N cell. When WL = 1, the access transistors are ON, allowing write/read access operations to be executed. When WL = 0, the access transistors are OFF, and the cell retains the stored value. Note that, the normal operations of the proposed S8P4N cell are similar to those of the proposed S4P8N cell. So, detailed descriptions are omitted here.

Figure 9 shows the simulation results for normal operations of the proposed S8P4N cell. It can be seen that the cell can correctly perform the "write 0, hold 0, read 0, write 1, hold 1, and read 1" operations.

The fault tolerance principles of the proposed S8P4N cell are described as follows. For illustration purpose, we still consider the case of 1 being stored in the cell (i.e., I1 = I3 = 1 and I2 = I4 = 0).

A. SNU Self-Recovery Principle

The SNU self-recovery principle is provided according to the state shown in Fig. 7. First, we consider the case where I1 is affected due to the SNU, i.e., I1 is temporarily changed to 0 from 1. At this time, since I1 is flipped, P2 and P8 become ON and N4 becomes OFF. I3 is not affected, i.e., I3 = 1, and hence P4 and P6 remain OFF and N2 remains ON. Thus, I2 is not affected (I2 = 0), and I4 still has its previous correct value of 0. Since I2 = 0 and I4 = 0, P1 and P5 remain ON and N1 remains OFF. Thus, I1 can return to the original correct state, i.e., I1 = 1. Therefore, I1 can self-recover from the SNU. Note that, when I3 is affected due to the SNU, i.e., I3 is temporarily changed to 0 from 1, a similar SNU self-recovery principle can be observed.

Next, we consider the case where I2 is affected due to the SNU, i.e., I2 is temporarily changed to 1 from 0. At this time, N1 becomes ON and P1 and P7 become OFF. Thus, I1 is temporarily changed to 0 from 1, and P2 and P8 become temporarily ON and N4 becomes temporarily OFF. Since I3 is not affected by the SNU (it still has the original value of 1), P4 and P6 remain OFF and N2 remains ON. Thus, I2 can return to its original correct value of 0 and I4 still has its previous correct value of 0. Since I2 = 0 and I4 = 0, P1 and P5 can return to their ON state and N1 can return to its OFF state. Therefore, I1 can return to its original value. In other words, the cell can self-recover from the SNU. Note that, when I4 is affected due to the SNU, i.e., I4 is temporarily changed to 1 from 0, a similar SNU self-recovery principle can be observed.

In the case of 0 being stored in the cell, it can be concluded

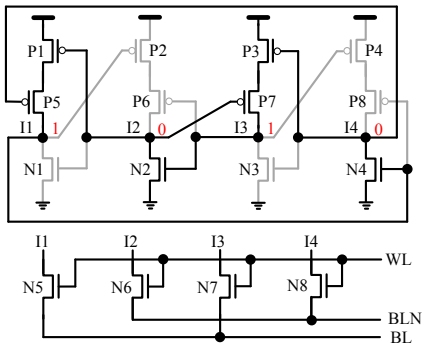

Fig. 7. Schematic of the proposed S8P4N cell.

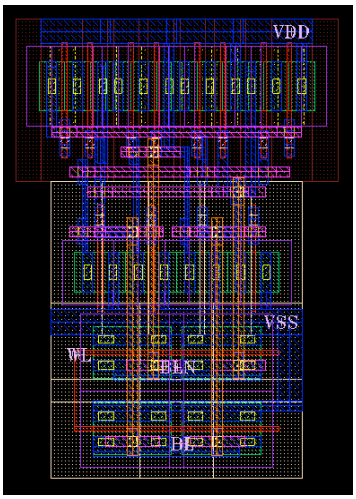

Fig. 8. Layout of the proposed S8P4N cell.

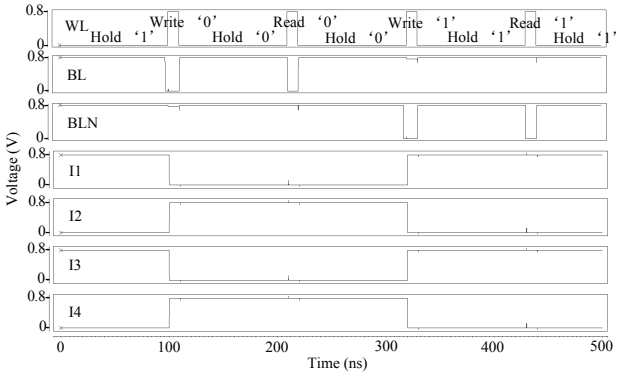

Fig. 9. Simulation results for normal operations of the proposed S8P4N cell.

from analysis and simulation that the cell can also self-recover from any SNU. We consider the case where I1 is affected due to the SNU, i.e., I1 is temporarily changed to 1 from 0. At this time, N4 becomes ON and P2 and P8 become OFF. Thus, I4 is temporarily changed to 0 from 1, and P3 and P5 become temporarily ON and N3 becomes temporarily OFF. Since I2 is not affected by the SNU (still has the original correct value of 1), P1 and P7 remain OFF and N1 remains ON. Thus, I1 can return to its original correct value of 0 and I3 still has its previous correct value of 0. Since I1 = 0 and I3 = 0, P4 and P8 return to their ON state and N4 returns to its OFF state. Therefore, I4 can return to its original correct value. In other words, the cell can self-recover from the SNU. Note that, when I3 is affected due to the SNU, i.e., I3 is temporarily changed to 1 from 0, a similar SNU self-recovery principle can be observed.

Next, we consider the case where I2 is affected due to the SNU, i.e., I2 is temporarily changed to 0 from 1. At this time, since I2 is temporarily flipped, P1 and P7 become ON and N1 becomes OFF. I4 is not affected, i.e., I4 = 1, and hence P3 and P5 remain OFF and N3 remains ON. Thus, I3 is not affected (I3 = 0), and I1 still has its previous correct value of 0. Since I1 = 0 and I3 = 0, P2 and P6 remain ON and N2 remains OFF. Thus, I2 can return to the original correct state, i.e., I2 = 1. Therefore, I2 can self-recover from the SNU. Note that, when I4 is affected due to the SNU, i.e., I4 is temporarily changed to 0 from 1, a similar SNU self-recovery principle can be observed. To summarize, the S8P4N cell can provide a complete SNU self-recoverability.

Figure 10 shows the simulation results for SNU self-recovery of nodes I1, I2, I3, and I4 of the proposed S8P4N cell. As shown in Fig. 10, in the case of 1 being stored, an SNU was injected to I1, I2, I3, and I4 between 0 and 100 ns, and between 350 and 450 ns, respectively. In the case of 0 being stored, an SNU was injected to I1, I2, I3, and I4 between 100 and 300 ns, respectively. As can be seen, all nodes of the S8P4N cell can self-recover from SNUs.

B. DNU-Tolerance Principle

Let us consider the DNU self-recovery principle of the proposed S8P4N cell. The cell has six key node-pairs, i.e., <I1, I2>, <I1, I3>, <I1, I4>, <I2, I3>, <I2, I4> and <I3, I4>. Here we discuss the case of 1 being stored.

First, we consider the case where <I1, I2> is affected by a DNU, i.e., I1 is temporarily changed to 0 and I2 is temporarily changed to 1. Since I1 = 0 and I2 = 1, P2, P8 and N1 become ON, and P1, P7 and N4 become OFF. Since I3 is not affected by the DNU (I3 still has its previous correct value of 1), P4 and P6 remain OFF and N2 remains ON. Therefore, I4 still has its previous correct value of 0, P5 remains ON, and I2 can return to its original correct value of 0. Thus, P1 and P7 return to their ON state, and N1 returns to their OFF state, so I1 can return to its original correct value of 1. In other words, <I1, I2> can self-recover from the DNU.

Second, we consider the case where <I3, I4> is affected by a DNU, i.e., I3 is temporarily changed to 0 and I4 is temporarily changed to 1. At this time, P4, P6 and N3 become ON, and P3, P5 and N2 become OFF. Since I1 is not affected by the DNU, I1 still has its previous correct value of 1, and P2 and P8 remain OFF and N4 remains ON. Therefore, I2 still has its previous correct value of 0, P7 remains ON, and I4 can return to its original correct value of 0. Thus, P3 and P5 return to their ON state, and N3 returns to its OFF state, so I3 can return to its original correct value of 1. In other words, <I3, I4> can self-recover from the DNU.

Finally, we consider the case where <I1, I3> is affected by a DNU, i.e., I1 and I3 are temporarily changed to 0. Thus, N2 and N4 become OFF and P2, P4, P6, and P8 become ON, so that the values of I2 and I4 are flipped. In other words, all nodes of the cell are flipped, and <I1, I3> cannot self-recover from the DNU. Note that for <I1, I4>, <I2, I3>, and <I2, I4>, similar results can be observed.

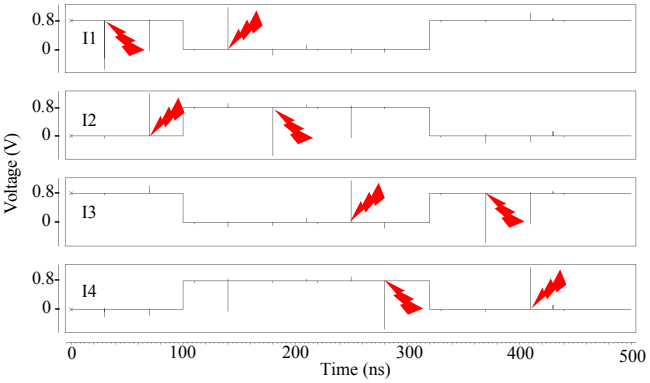

Fig. 10. Simulation results for SNU self-recovery of the proposed S8P4N cell.

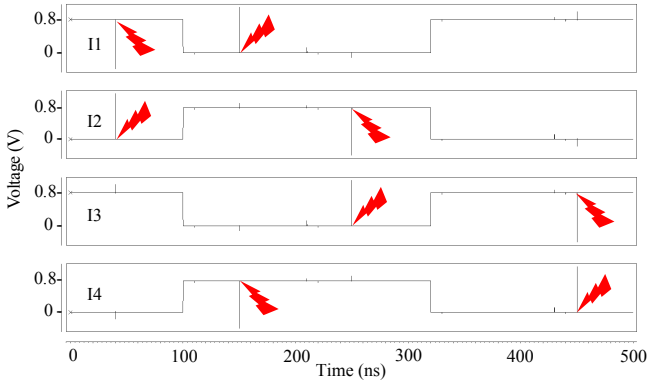

Fig. 11. Simulation results for DNU self-recovery of the proposed S8P4N cell.

To summarize, for the proposed S8P4N cell, in the case of 1 being stored, node pairs <I1, I2> and <I3, I4> can self-recover from DNUs, but the other node pairs cannot self-recover from DNUs. Next, we discuss the case of 0 being stored for the cell.

First, we consider the case where <I1, I4> is affected by a DNU, i.e., I1 is temporarily changed to 1 and I4 is temporarily changed to 0, and hence P3, P5, and N4 become ON and P2, P8, and N3 become OFF. Since I2 is not affected by the DNU, I2 still has its previous correct value of 1, and P1 and P7 remain OFF and N1 remains ON. Thus, I3 still has its previous correct value 0 and I1 can return to its original correct value of 0. At this time, N2 and N4 remain OFF and P2, P4, P6, and P8 remain ON, so that I4 can return to its original correct value of 1. In other words, <I1, I4> can self-recover from the DNU.

Second, we consider the case where <I2, I3> is affected by a DNU, i.e., I2 is temporarily changed to 0 and I3 is temporarily changed to 1, and hence P1, P7, and N2 become ON and P4, P6, and N1 become OFF. Since I4 is not affected by the DNU, I4 still has its previous correct value of 1, and P3 and P5 remain OFF and N3 remains ON. Thus, I1 still has its previous correct value of 0 and I3 can return to its original correct value of 0. At this time, N2 and N4 remain OFF and P2, P4, P6, and P8 remain ON, so that I2 can return to its original correct value of 1. In other words, <I2, I3> can self-recover from the DNU.

Finally, we consider the case where <I1, I2> is affected by a DNU, i.e., I1 is temporarily changed to 1 and I2 is temporarily changed to 0. At this time, P2, P8 and N1 become OFF and P1, P7, and N4 become ON, and hence I4 is flipped to 0. Thus, P3 and P5 become ON and N3 becomes OFF. Since P3 and P7 become ON and N3 becomes OFF, I3 is flipped to 0. In other words, all nodes of the cell are flipped. Therefore, <I1, I2> cannot self-recover from the DNU. Note that for <I1, I3>, <I2, I4>, and <I3, I4>, similar DNU self-recovery results can be observed. To summarize, for the proposed S8P4N cell, in the case of 0 being stored, node pairs <I1, I4> and <I2, I3> can self-recover from a DNU, but the other node pairs cannot self-recover from a DNU.

Figure 11 shows the simulation results for DNU self-recovery of node pairs <I1, I2>, <I1, I4>, <I2, I3>, and <I3, I4> of the proposed S8P4N cell. In the case of 1 being stored (I1 = 1), DNUs were injected to node pairs <I1, I2> and <I3, I4> between 0 and 100 ns and between 400 to 500 ns, respectively. In the case of 0 being stored (I1 = 0), DNUs were injected to node pairs <I1, I4> and <I2, I3> between 100 and 300 ns, respectively. From Fig. 11, we can conclude that the proposed S8P4N cell can self-recover from DNUs on node pairs <I1, I2> and <I3, I4> when storing 1 and can self-recover from DNUs on node pairs <I1, I4> and <I2, I3> when storing 0 (totally four node-pairs are DNU-self-recoverable).

TABLE I
SUMMARY OF NODE-UPSET TOLERANCE OF THE PROPOSED SRAMS.

	S4P8N		S8P4N	
	When I1 = 1	When I1 = 0	When I1 = 1	When I1 = 0
SRN	I1, I2, I3, I4.	I1, I2, I3, I4.	I1, I2, I3, I4.	I1, I2, I3, I4.
DHP	<I1, I4>, <I2, I3>.	<I1, I2>, <I3, I4>.	<I1, I2>, <I3, I4>.	<I1, I4>, <I2, I3>.
DNHP	<I1, I2>, <I1, I3>, <I2, I4>, <I3, I4>.	<I1, I3>, <I1, I4>, <I2, I3>, <I2, I4>.	<I1, I3>, <I1, I4>, <I2, I3>, <I2, I4>.	<I1, I2>, <I1, I3>, <I2, I4>, <I3, I4>.

In summary, the proposed SRAM cells can provide complete self-recovery from all possible SNUs and partial recovery from DNUs. Table I shows a summary of node-upset tolerance of the proposed SRAMs. In Table I, SRN means SNU Recoverable single Nodes, DHP means DNU-Hardened node Pairs, and DNHP means DNU-Not-Hardened node Pairs. It can be seen from Table I that all single nodes of the proposed SRAMs can self-recover from all possible SNUs and the DNU-hardened node pairs of each proposed SRAM cell is up to 4.

IV. COMPARISON AND EVALUATION RESULTS

To make a fair comparison with the state-of-the-art SRAM cells described in Section I, the same simulation conditions and technology node (22nm CMOS) as those described in the above section were used. Table II shows the reliability and overhead comparison results among the unhardened/hardened SRAMs in terms of *SNU recoverability* (*SNUR*), *number* of *DHP* (*#DHP*), average power dissipation (dynamic and static) that is measured with the method in [22], silicon area that is measured with the method in [30], *read access time* (*RAT*), and *write access time* (*WAT*). Note that, the hold operations consume static power, the read/write operations consume dynamic power and the operations are shown in Figs. 4 and 9. The *percentages of reduced costs* (*PRCs*) of the proposed cells compared with the other cells were calculated using the method in [28] and are also shown in Table II.

Let us first discuss about the reliability comparison. It can be seen from Table II that, the proposed S4P8N and S8P4N cells, and the Lin12T, RH12T, DNUCTM, and DNUSRM cells can provide complete SNU self-recoverability from all possible SNUs, while the other cells cannot provide complete SNU self-recoverability since any of them has at least one node that cannot self-recover from an SNU. Regarding #DHNPs, the 6T and NASA13T cells have no DHNP, and the We-Quatro, PS10T, Lin12T, RH12T, DNUCTM, and DNUSRM cells have two or more than two DHNPs. Clearly, except the DNUCTM and DNUSRM cells, only the proposed S4P8N and S8P4N cells have the maximum number of DHNPs which is 4. Although the DNUCTM and DNUSRM cells have up to 16 DHNPs, they require large power dissipation and silicon area overhead. This point will be discussed in the following. To summarize, the proposed cells achieve a better balance between reliability and overhead.

For power and area, it can be seen from Table II that the 6T cell has the smallest power and area due to the use of only 6 transistors. Generally, a cell having a few transistors has a small area. It can be seen from Table II that the proposed cells have to use extra transistors/area to ensure the self-recoverability from all possible SNUs and a part of DNUs as well as optimized speed and power. However, the proposed S4P8N and S8P4N cells have smaller power compared with the other hardened cells. Note that, the NASA13T consumes the largest power mainly due to the large current competition in its feedback loops and the use of extra access transistors.

For RATs and WATs, it can be seen from Table II that the 6T cell has the smallest WAT. This is mainly because the cell has less current competition when writing a value. Conversely, the QCCM10T has the largest WAT due to more current competition when writing a value. It also can be seen from Table II that the proposed S4P8N cell has a comparable WAT and RAT compared with the other hardened cells. The proposed S8P4N has a smaller WAT and RAT than most of the other hardened cells. This is mainly because the cell has less current competition during access operations through parallel access transistors. Note that the S8P4N cell has more PMOS transistors and we used smaller transistor sizes for PMOS transistors to achieve better performance compared to the S4P8N cell. The NASA13T has the largest RAT due to its

special read operation (slow current flow through read transistors). Indeed, the intrinsic charge/discharge operations of cell-nodes through access transistors can affect RATs and WATs. Therefore, the better reliability and optimized overhead of the proposed S4P8N and S8P4N cells are effectively balanced.

Let us now discuss the PRCs. For the sake of brevity, only the average PRCs are discussed. For the proposed S4P8N cell, compared with other hardened cells, the average PRCs of the power dissipation, silicon area, RAT, and WAT are 26.72%, -41.06%, -10.50%, and 0.27%, respectively. It means that the power dissipation of the proposed S4P8N cell is reduced approximately by 27% on average mainly at the cost of silicon area. For the proposed S8P4N cell, compared with the state-of-the-art hardened cells, the average PRCs of the power dissipation, silicon area, RAT, and WAT are 20.63%, -18.57%, 20.25%, and 29.48%, respectively. It means that the power dissipation, RAT, and WAT of the proposed S8P4N cell are reduced approximately by 21%, 20%, and 29% on average, at the cost of moderate silicon area.

To summarize, the fault-tolerance ability of the proposed S4P8N and S8P4N cells are achieved mainly at the cost of extra indispensable silicon area compared with the existing state-of-the-art hardened cells. Moreover, compared with most of the existing state-of-the-art hardened cells, the proposed S4P8N cell has a low overhead especially in terms of power dissipation, and the proposed S4P8N cell has a lower overhead especially in terms of power dissipation, RAT, and WAT.

The *process, voltage and temperature* (*PVT*) variations can seriously impact the performance of SRAM cells, and SRAM cells are more sensitive to PVT variations in advanced nano-scale technologies [30-31]. Figure 12 shows the results of PVT variation impacts on power, WAT, and RAT for SRAM cells. Note that, the normal temperature was set to 25℃ and the temperature was ranged from -25℃ to 125℃. The normal supply voltage was set to 0.8V and the supply voltage variation was ranged from 0.65V to 0.95V. The threshold-voltage increment was ranged from 0.01V to 0.06V.

Fig. 12-(a), (b), and (c) show the impact of temperature variations on power, WAT, and RAT. It is clear that as the temperature increases, the SRAM cells need to consume more power, WAT, and RAT. It can be seen from Fig. 12-(a) that the DNUSRM and DNUCTM are more sensitive to temperature variations on power, mainly due to the large current competition in their feedback loops and the use of extra access transistors. However, the 6T and S4P8N are less sensitive to temperature variations on power. It can be seen from Fig. 12-(b) that the QUCCE10T is more sensitive to temperature variations on WAT, and the NASA13T cell is less sensitive to temperature variations on WAT. It can be seen from Fig. 12-(c) that the NASA13T is more sensitive to temperature variations on RAT, mainly due to its more decreased carrier mobility when the temperature is rising. Otherwise, the temperature variations have a low impact on the RAT of the cells, such as DNUSRM, QCCM12T, S4P8N, and S8P4N.

Fig. 12-(d), (e), and (f) show the impact of supply voltage variations on power, WAT, and RAT. It is clear that as the supply voltage increases, large supply voltage can lead to large power dissipation of SRAM cells but can reduce access time. It can be seen from Fig. 12-(d) that the DNUSRM cell is the most sensitive to supply voltage variations on power, but the 6T is less sensitive to supply voltage variations on power

TABLE II
RELIABILITY AND OVERHEAD COMPARISON RESULTS AMONG THE UNHARDENED AND HARDENED SRAMS UNDER 22NM CMOS TECHNOLOGY NODE.

	SNUR	#DHP	Power (nW)	$10^{-3}\times$ Area (nm^2)	RAT (ps)	WAT (ps)	PRC (%)							
							Power		Area		RAT		WAT	
							4P8N	8P4N	4P8N	8P4N	4P8N	8P4N	4P8N	8P4N
6T	×	0	5.24	4.35	25.88	3.65	-	-	-	-	-	-	-	-
QCCM10T [12]	×	1	11.45	7.79	18.20	23.21	25.33	19.13	-62.64	-36.71	1.48	28.90	77.64	84.19
QCCM12T [12]	×	1	10.43	8.71	12.99	4.22	18.02	11.22	-45.46	-22.27	-38.03	0.38	-22.99	13.03
NASA13T [13]	×	0	18.92	9.70	128.67	16.39	54.81	51.06	-30.62	-9.79	86.07	89.94	68.33	77.61
QUCCE10T [14]	×	1	10.08	6.16	36.36	6.29	15.18	8.13	-105.68	-72.89	50.69	64.41	17.49	41.65
QUCCE12T [14]	×	1	10.43	8.71	13.02	4.31	18.02	11.22	-45.46	-22.27	-37.71	0.61	-20.42	14.85
We-Quatro [15]	×	2	10.43	8.71	12.99	4.38	18.02	11.22	-45.46	-22.27	-38.03	0.38	-18.49	16.21
PS10T [16]	×	2	10.14	7.30	25.79	5.14	15.68	8.68	-73.56	-45.89	30.48	49.83	-0.97	28.60
Lin12T [17]	√	2	9.74	9.28	37.68	3.78	12.22	4.93	-36.53	-14.76	52.42	65.66	-37.30	2.91
RH12T [18]	√	2	9.74	9.28	37.72	3.85	12.22	4.93	-36.53	-14.76	52.47	65.69	-34.81	4.68
DNUCTM [19]	√	16	15.65	13.07	8.75	4.50	45.37	40.83	3.06	18.52	-104.91	-47.89	-15.33	18.44
DNUSRM [19]	√	16	20.86	17.42	6.63	4.71	59.01	55.61	27.27	38.86	-170.44	-95.17	-10.19	22.08
S4P8N (Proposed)	√	4	8.55	12.67	17.93	5.19	26.72	-	-41.06	-	-10.50	-	0.27	-
S8P4N (Proposed)	√	4	9.26	10.65	12.94	3.67	-	20.63	-	-18.57	-	20.25	-	29.48

mainly due to the use of only 6 transistors. It can be seen from Fig. 12-(e) that the QCCM10T is the most sensitive to supply voltage variations on WAT, but the variations have a low impact on the WAT of the cells, such as QCCM12T, S4P8N and S8P4N. It can be seen from Fig. 12-(f) that the NASA13T cell is the most sensitive to supply voltage variations on RAT. This is mainly due to its special read operation. Otherwise, the supply voltage variations have a low impact on the RAT of the cells, such as DNUSRM, QCCM12T, DNUCTM, S4P8N, and S8P4N.

Fig. 12-(g), (h), and (i) show the impact of threshold voltage variations on power, WAT, and RAT. It is clear that as the threshold voltage increases, large threshold voltage can decrease power dissipation of SRAM cells but can increase access time. It can be seen from Fig 12-(g) that the DNUSRM is the most sensitive to threshold voltage variation on power mainly due to the large current competition in its feedback loops and the use of extra access transistors. However, the QCCM10T, Lin12T, and RH12T cells are less sensitive to

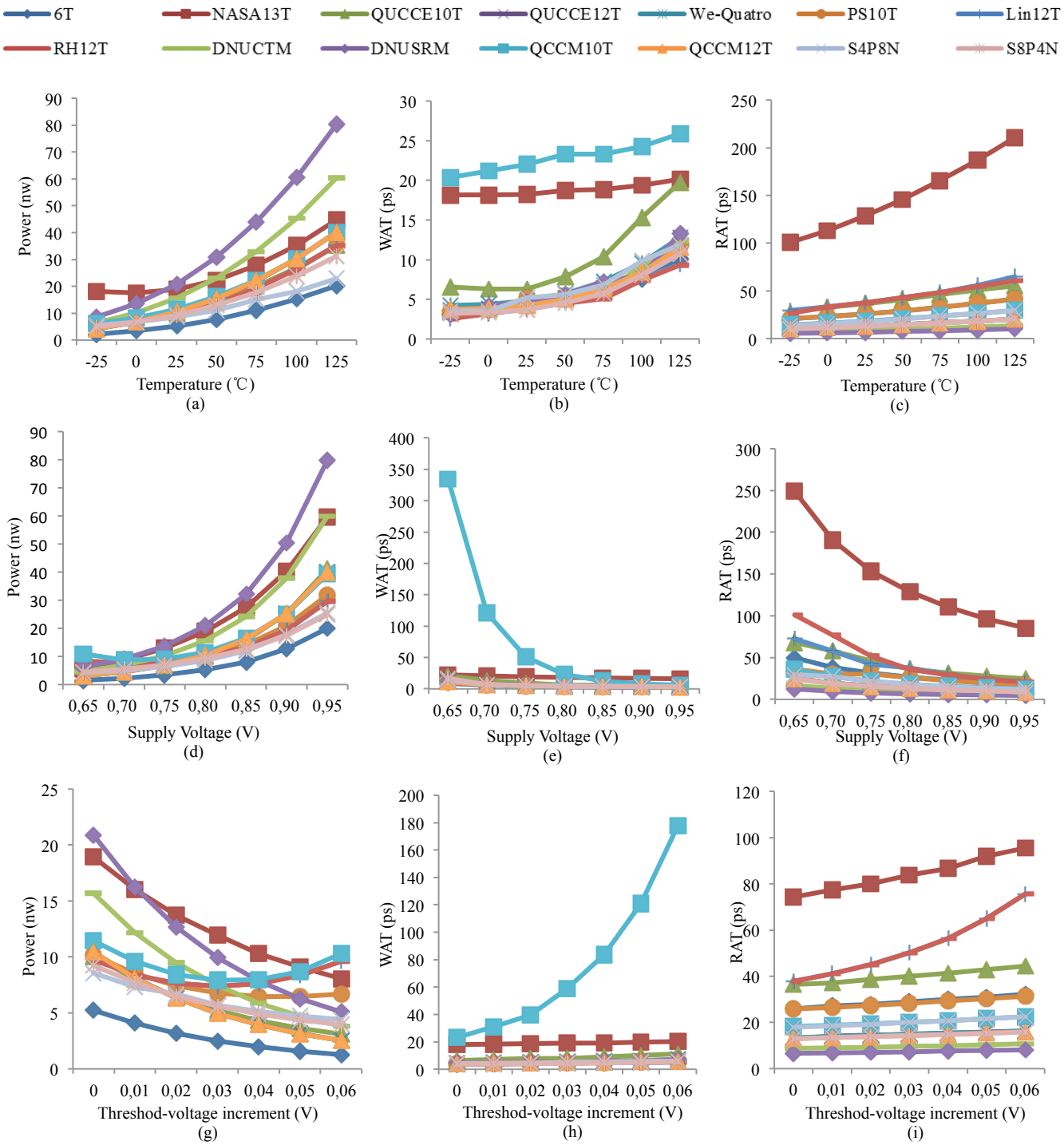

Fig. 12. Estimation results of PVT variation impacts on power, WAT, and RAT for SRAM designs. (a) Impacts of temperature variations on power. (b) Impacts of temperature variations on WAT. (c) Impacts of temperature variations on RAT. (d) Impacts of supply voltage variations on power. (e) Impacts of supply voltage variations on WAT. (f) Impacts of supply voltage variations on RAT. (g) Impacts of threshold-voltage variations on power. (h) Impacts of threshold-voltage variations on WAT. (i) Impacts of threshold-voltage variations on RAT.

supply voltage variations on power. It can be seen from Fig 12-(h) that the QCCM10T is more sensitive to threshold voltage variation on WAT, but the variation has a low impact on the WAT of the cells, such as S4P8N and S8P4N. It can be seen from Fig 12-(i) that the RH12T and Lin12T are more sensitive to threshold voltage variation on RAT. This is mainly because they employ many devices from their storage nodes to their output. Finally, the threshold voltage variation has a low impact on the WAT of the cells, such as DNUCTM, QCCM12T, S4P8N, and S8P4N. To summarize, PVT variation has moderate impacts on power, WAT, and RAT of the proposed S4P8N and S8P4N cells, compared with the state-of-the-art hardened SRAM cells.

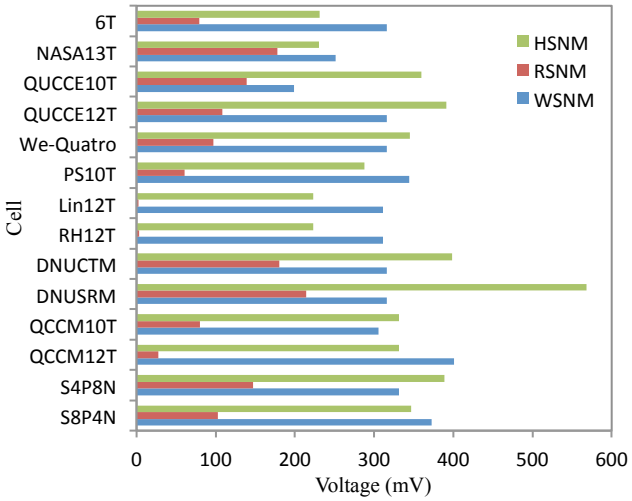

Fig. 13. SNM comparison under the supply voltage of 0.8V.

It is reported in [20] that *static noise margin* (*SNM*) is an important metric to analyze stability of SRAM cells for normal operations. Figure 13 shows the comparison results of SNMs for different SRAM cells under a supply voltage of 0.8V. Note that the normal temperature was set to 25℃. From Fig. 13, it can be seen that the *hold SNM* (*HSNM*) value of the proposed S4P8N and S8P4N cells are higher than those of the hardened NASA13T, We-Quatro, PS10T, Lin12T, RH12T, QCCM10T, and QCCM12T cells, but lower than those of the QUCCE12T, DNUCTM, DNUSRM cells. It can be seen that the *read SNM* (*RSNM*) value of the proposed S4P8N and S8P4N cells are higher than those of the hardened We-Quatro, PS10T, Lin12T, RH12T, QCCM10T, and QCCM12T cells, but lower than those of the NASA13T, DNUCTM, DNUSRM cells. It can also be seen that the *write SNM* (*WSNM*) value of the proposed S4P8N and S8P4N cells are higher than those of the hardened NASA13T, QUCCE10T, QUCCE12T, We-Quatro, Lin12T, RH12T, DNUCTM, DNUSRM, and QCCM10T cells, but lower than those of the QCCM10T cell. To summarize, the comparison results of the SNMs show that the proposed S4P8N and S8P4N cells have moderate SNMs, compared with the state-of-the-art hardened SRAM cells.

Figure 14 shows the comparison results of SNMs under different supply voltages. Note that the normal supply voltage was set to 0.8V and the supply voltage variation was ranged from 0.60V to 1.30V. The normal temperature was still set to 25℃. Fig. 14-(a), (b), and (c) show the impact of supply voltage variations on HSNM, RSNM, and WSNM. It can be seen that, as the supply voltage increases, the value of HSNM is generally increasing, the value of RSNM is generally decreasing, and the value of WSNM is generally increasing. It can be seen from Fig. 13-(a) that, as the supply voltage increases, the proposed S4P8N cell has a similar HSNM sensitivity compared to the DNUSRM cell, but the proposed S8P4N has a lower HSNM sensitivity. It can be seen from Fig. 14-(b) that, as the supply voltage increases, the proposed S8P4N cell has a similar RSNM sensitivity compared to the DNUCTM cell, but the proposed S4P8N has a lower RSNM sensitivity. Finally, it can be seen from Fig. 14-(c) that, as the supply voltage increases, the proposed S8P4N cell has a similar WSNM sensitivity compared to the PS10T, Lin12T, RH12T, and QCCM10T cells, but the proposed S4P8N has a lower WSNM sensitivity.

V. Conclusions

The continuous advancement of CMOS technologies makes SRAMs more and more sensitive to soft errors such as SNUs and DNUs. Based on the RHBD approach, two novel reliable SRAM cells, namely S4P8N and S8P4N, with optimized speed and power, have been proposed in this paper. The proposed S4P8N and S8P4N cells can self-recover from all possible SNUs and a part of DNUs. The access operations of the proposed cells are optimized through the use of four

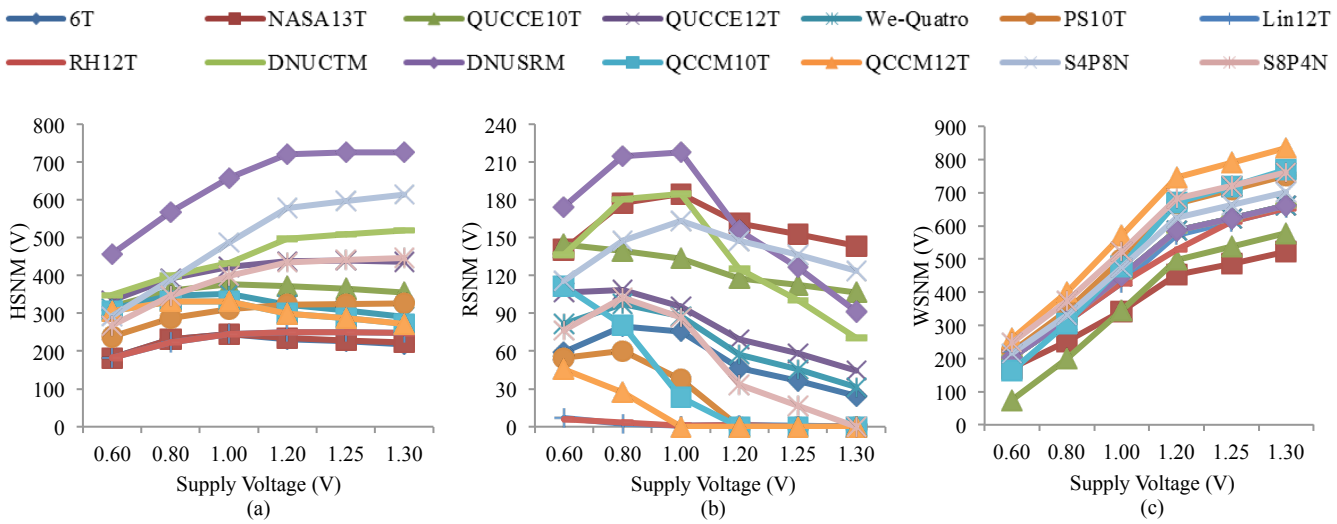

Fig. 14. SNM comparisons under different supply voltages. (a) HSNM. (b) RSNM. (c) WSNM.

parallel access transistors. The proposed S4P8N and S8P4N cells have low overhead especially in terms of power dissipation. Compared with S4P8N, the S8P4N cell has a smaller WAT and RAT. The proposed S4P8N and S8P4N cells can be effectively applied to fields such as low-orbit aerospace and terrestrial safety-critical applications, where the DNU issue is not severe. For applications in harsh radiation environments, our previous work in [19] is suitable to provide very high reliability.

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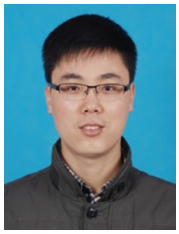

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