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# Design of Double-Upset Recoverable and Transient-Pulse Filterable Latches for Low-Power and Low-Orbit Aerospace Applications

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**To meet the requirements of both high reliability and low power in low-orbit aerospace applications, this article first presents a single-event Double-Upset (SEDU) self-Recoverable and single-event Transient (SET) Pulse Filterable (DURTPF) latch design with low power. The DURTPF latch mainly consists of eight mutually feeding-back C-elements (CEs) and an SET pulse filterable Schmitt-trigger (ST). To make an ST behave not only as a pulse filterable ST but also as an error interceptive CE, an input-split ST is created, leading to an enhanced-version of the DURTPF latch, namely DURTPF-EV. The DURTPF-EV latch mainly consists of seven mutually feeding-back CEs including an input-split ST. Simulation results demonstrate both the SEDU self-recoverability and SET pulse filterability of the proposed latches at the cost of moderate silicon area. Using the clock gating technology, the DURTPF latch reduces power dissipation by about 63% on average compared with the state-of-the-art SEDU self-recoverable latch designs that are not SET-pulse filterable. Moreover, the DURTPF-EV latch is more cost-effective and its reliability is also enhanced, making it more suitable for low power and low-orbit aerospace applications.**

## I. INTRODUCTION

Nano-scale complementary metal-oxide semiconductor (CMOS) chips make it possible for aerospace vehicles, relay satellites, 5G terminals, etc., to connect, interact, and exchange data with each other. However, for unhardened electronic devices fabricated using the advanced nano-scale CMOS technologies, radiation effects can easily cause soft errors due to the strike of high-energy particles such as neutrons, protons, alpha particles, and electrons [1]. Soft errors behave as transient but not permanent errors, and with technology scaling, more and more represent a serious concern for circuit reliability [2]. This implies that the logic states of circuit nodes become more easily disturbed by striking-particles in silicon, causing data corruptions, execution errors, or even system crashes. Therefore, integrated circuits in aerospace applications and even terrestrial medical devices require novel designs for efficient radiation tolerance [3].

Single-event upset (SEU), single-event double-upset (SEDU), and single-event transient (SET) are the typical types of soft errors for low-orbit aerospace applications and even terrestrial medical devices. In deep-submicron technologies, the strike of a particle can invalidly change the logic state of a single node in a storage cell, resulting in an SEU. However, in the advanced nano-scale CMOS technologies, the strike of a particle can simultaneously change the logic states of a node pair, resulting in an SEDU. This may also result in a transient pulse at the output of a logic gate in a combinational circuit, resulting in an SET. If an SET pulse propagates through logical gates and arrives at a downstream storage cell, it may be captured by the cell [4]. Like SEUs and SEDUs, SETs can also cause data corruptions, execution errors, or even system crashes. Therefore, it is crucial to propose novel storage cells that are robust against SEUs, SEDUs, and SETs, especially for low-orbit aerospace applications and even terrestrial medical devices that face to moderate radiation effects.

Many novel schemes have been proposed to effectively tolerate SEUs [5]–[18]. Using redundant hold nodes or techniques such as transistor resizing and dual-modular



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redundancy, most of these schemes can robustly retain values against SEUs. Note that, using temporal redundancy, some of these schemes are also SET-pulse filterable, especially for the latch designs in [14]–[16], and [18]. However, SEU and/or SET hardening only are not sufficient for low-orbit aerospace applications. It has been reported that ever-increasing integration scale, ever-decreasing transistor sizes, and ever-lowering supply voltages can allow striking-particle induced single-event charge collection to affect double nodes and cause SEDUs [19]. In [20], it is reported that SEDUs are becoming more prominent and the soft error rate of circuits and systems caused by SEDUs is rising. Hence, existing SEU and/or SET hardened schemes are not robust, making them not applicable to low-orbit aerospace applications.

Many state-of-the-art schemes have been proposed to effectively tolerate SEDUs [21]–[28]. Enlarging transistors seems a feasible method to tolerate SEDUs, but the weak node pairs can nevertheless be flipped especially when the energy of the radiation particle is high. Similarly, layout-based solutions such as well isolation and node spacing increase can also make a circuit SEDU tolerant, but these techniques can increase the complexity of integrated circuit designs [25]. Hence, an efficient way to tolerate SEDUs relies on the radiation hardening by design (RHBD) technique using multiple-modular redundancy or redundant hold nodes. Despite its efficiency, this technique suffers from severe problems in terms of SEDU self-recoverability, SET pulse filterability, and cost effectiveness. Moreover, although some triple-node upset tolerant latches have been proposed [29]–[31], these designs are mainly used for applications that have to face very harsh radiation environments. Online self-recoverability is crucial for aerospace applications as indicated in [30], and this motivates us to provide the SEDU self-recoverability of our proposed latch designs.

In this article, an SEDU self-recoverable and SET pulse filterable (DURTPF) latch design is first proposed. To the best of our knowledge, the latch is the first ever latch that is SEDU self-recoverable and SET pulse filterable. The DURTPF latch mainly employs eight mutually feeding-back C-elements (CEs) and a Schmitt-trigger (ST), making the latch not only SEDU self-recoverable but also SET pulse filterable under moderate striking-particle energy. Second, to harden against some particles that have higher energy, an enhanced version of DURTPF, namely a DURTPF-EV latch, is proposed using seven mutually feeding-back CEs including an input-split ST (ISST). The ISST is created through splitting the original input of the ST into two inputs, making the ISST behave not only as an ST but also as a CE. Simulation results demonstrate the SEDU self-recoverability and SET pulse filterability of the proposed latches under moderate and higher striking-particle energy, respectively. Moreover, the DURTPF-EV latch consumes less power due to the use of a few transistors and the clock-gating (CG) technology, making the latch more suitable for low power and low-orbit aerospace applications.

The contribution of this article can be summarized as follows.

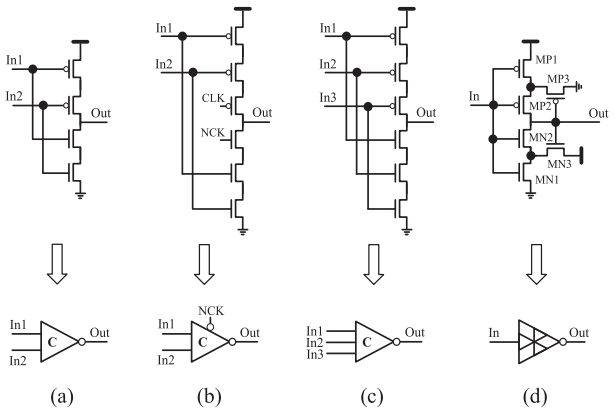


Fig. 1. Widely used components for radiation hardened latch designs. (a) Two-input C-element. (b) Clock gating based two-input C-element. (c) three-input C-element. (d) Schmitt trigger.

1) We first propose a DURTPF latch that allows both SEDU self-recoverability and SET pulse filterability using several CEs and an ST, in the case of moderate striking-particle energy.
2) We then propose an enhanced version of the latch (DURTPF-EV) that allows both SEDU self-recoverability and SET pulse filterability using several CEs and an ISST, in the case of higher striking-particle energy.
3) Using the CG technology, the power dissipation of the two proposed latches is low. Using a few transistors, the power dissipation of the enhanced DURTPF-EV latch is much lower.

The rest of the article is organized as follows. Section II reviews previous hardened latch designs. Section III presents the schematics, working principles and validations of the proposed DURTPF and DURTPF-EV latches, respectively. Section V quantitatively shows the overhead comparison results. Finally, Section V concludes this article.

## II. PREVIOUS HARDENED LATCH DESIGNS

Fig. 1 shows the widely used components of many hardened latch designs. A two-input CE behaves as an inverter if its inputs are identical and it retains its previous value if its inputs become different. As for a CG based two-input C-element, its behavior can also be controlled by system clock (CLK) and negative system clock (NCK) signals. We will discuss the ST in the following section.

Fig. 2 shows the schematics of the representative SEU, SEDU, and/or SET hardened latch designs. The TMR latch in Fig. 2(a) uses three traditional D-latches and a voter to tolerate SEUs. However, the latch cannot tolerate SEDUs and SET pulses. The DET-SEHP latch [14] in Fig. 2(b) mainly uses an ST to filter SET pulses and a CE feeding back to its inputs to tolerate SEUs. However, if there is an SEU at Q or an SEDU at the inputs of the CE, the latch will retain an invalid value. The LCHR latch [15] in Fig. 2(c) employs three keepers feeding a CE to tolerate SEUs and uses an ST to filter SET pulses. However, if there is an



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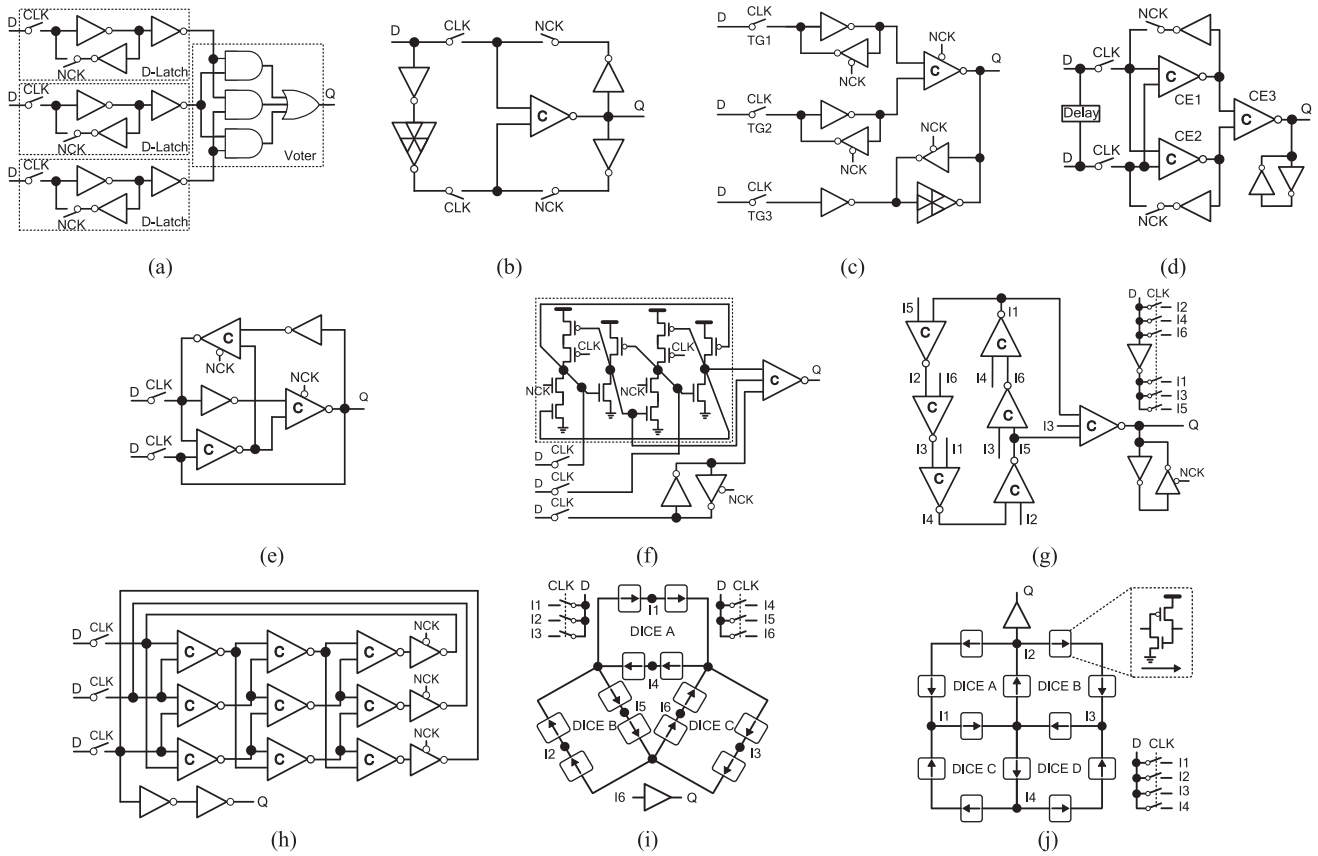


Fig. 2. Schematics of the previous hardened latch designs. (a) TMR. (b) DET-SEHP [14]. (c) LCHR [15]. (d) FERST-EV [16]. (e) RFC [17]. (f) CLCT [24]. (g) DNCS [25]. (h) NTHLTCH [26]. (i) DeltaDICE [27]. (j) DONUT [28].

SEDU at the inputs of the CE, the latch cannot tolerate it. The FERST-EV latch [16] in Fig. 2(d) mainly employs temporal redundancy to filter SET pulses and uses two interlocked feedback loops connecting to CE3 to tolerate SEUs. However, if there is an SEDU at the inputs of CE3, the latch cannot tolerate it. The RFC latch [17] in Fig. 2(e) employs three interlocked and mutually feeding-back CEs to achieve SEU self-recoverability. However, if the outputs of the two CEs are flipped due to an SEDU, the latch will retain an invalid value. In addition, the latch cannot filter SET pulses.

The CLCT latch [24] in Fig. 2(f) mainly uses a CG-based DICE cell [32] and a keeper connecting to a three-input CE to tolerate SEDUs. However, there are many node pairs that cannot self-recover from SEDUs in the latch and the latch cannot filter SET pulses. As shown in Fig. 2(g), using a feedback loop connecting to a three-input CE, the DNCS latch [25] tolerates SEDUs. However, like the CLCT latch, the latch cannot provide SEDU self-recoverability and SET pulse filterability. The NTHLTCH latch [26] in Fig. 2(h) mainly employs nine two-input CEs and three CG based inverters to achieve SEDU self-recoverability. However, the latch cannot filter SET pulses. The DeltaDICE latch [27] in Fig. 2(i) uses three interlocked DICE cells to achieve SEDU self-recoverability. However, the latch has the same drawbacks compared with the DONUT latch that will be described here. The DONUT latch [28] in Fig. 2(j) comprises four interconnected DICE cells to provide enough redundant nodes to ensure SEDU self-recoverability. However, the latch cannot filter SET pulses and has large power dissipation due to more current competition between many internal nodes.

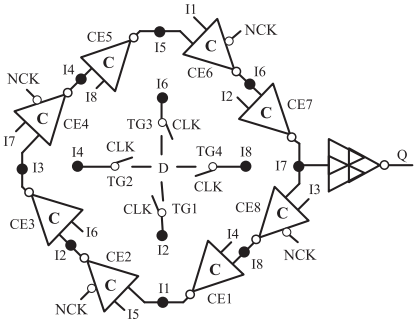


Fig. 3. Circuit schematic of the proposed DURTPF latch design.

## III. PROPOSED LATCH DESIGNS

### A. Proposed DURTPF Latch

The circuit schematic of our proposed DURTPF latch design is depicted in Fig. 3. Fig. 4 shows the layout of the



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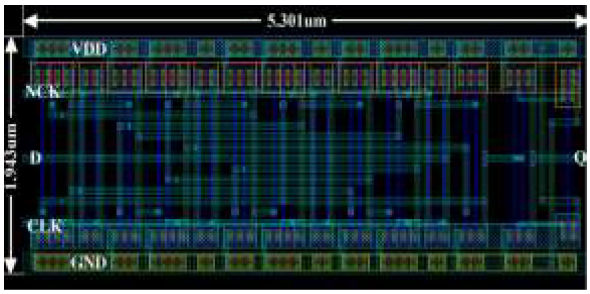


Fig. 4. Layout of the proposed DURTPF latch design.

latch. It can be seen that it is constructed from eight two-input CEs (CE1 to CE8), four transmission gates (TG1 to TG4), and one ST at the output stage of the latch. Note that, CE2, CE4, CE6, and CE8 are CG-based CEs. In the latch, D is the input, I1 to I8 are the internal nodes, and Q is the output, respectively.

When CLK is high and NCK is low, the transmission gates are ON and the latch works in transparent mode. In this mode, all clock-signal controlled transistors in the CG-based CEs are OFF. It can be seen from Fig. 3 that the inputs of both CE1 and CE5 are driven by D through TG2 and TG4, respectively; thus, the outputs of CE1 and CE5 can be known. Similarly, the outputs of CE3 and CE7 can be known. Therefore, we can get the output of any CE among CE1, CE3, CE5, and CE7.

It can be seen from Fig. 3 that the inputs of CE2 are driven by the outputs of CE1 and CE5; however, the output of CE2 is blocked using the CG technology. This avoids current competition at the output of CE2 so as to save power dissipation. Similarly, the outputs of CE4, CE6, and CE8 are blocked to save power dissipation. On the other hand, since the output of CE7 feeds the ST at the output stage of the latch, we can get the output of the latch and thus all the transistors in the latch are biased properly.

The reason why the latch is SET pulse filterable when working in transparent mode is described as follows. If an SET pulse arrives at D, the pulse will be first reversed by CE7 and then will be filtered by the ST. Here, as an example, we consider the case of a positive SET pulse (low-high-low). The transistors MP1, MP2, and MN3 in Fig. 1(d) are precharged and biased properly. As a result, when D changes from low to high (the rise stage), the output of the ST will not change until the drain of MN1 is discharged from high to low. This needs a period of time especially when the aspect ratios of MN1 and MN3 are large. Within that period of time, D may change from high to low (the fall stage), and the output of the ST will not change, i.e., the SET pulse is masked/filtered.

When CLK is low and NCK is high, the transmission gates are OFF and the latch switches to hold mode. In this mode, all clock-signal controlled transistors in the CG-based CEs are ON. Thus, the outputs of the CG-based CEs are prevented from being driven by D through the transmission gates and instead they are driven by the CG-based CEs. This way, all the interlocked feedback loops in the latch are constructed to effectively keep values. The feedback rule for the CEs is as follows. The output of any CE in the ordered and circulated CE list <CE1, CE2, CE3, CE4, CE5, CE6, CE7, CE8> is fed back to both one input of the next CE and one input of the previously third CE. Finally, Q is robustly driven by the output of CE7 through the ST to keep values.

In the presence of an SEU for the latch when it works in hold mode, there are totally nine cases because an SEU may affect any of the internal nodes I1 to I8 as well as the output of the latch. Here, as an example, we consider the case where an SEU affects I1 resulting in a glitch. According to the CEs' feedback rule, the glitch can propagate to one input of CE2 as well as one input of CE6, but CE2 and CE6 can intercept the glitch. On the other hand, because the SEU cannot affect the inputs of CE1, I1 can restore back the correct value through the correct inputs of CE1. This way, the internal nodes of the latch can restore back the correct values from any SEU, and finally the output of the latch can restore back the correct value through the ST. Therefore, all nodes in the latch keep correct values, i.e., the latch is SEU self-recoverable.

In the presence of an SEDU for the latch when it works in hold mode, any node pair should be considered. In the circular structure of Fig. 3, since any two of the internal nodes I1 to I8 can be affected by an SEDU, there are totally $C_8^2 = 28$ cases in the presence of an SEDU. On the other hand, since the output of the latch and one of the eight internal nodes I1 to I8 can also be affected by an SEDU, there are eight more cases in the presence of an SEDU. However, since the latch is SEU self-recoverable, as for the just mentioned eight more cases in the presence of an SEDU, the internal node can first self-recover and the output node can then self-recover from the SEDU. Hence, the latch is SEDU self-recoverable for the eight cases and we only have to prove that the circular structure of the latch is SEDU self-recoverable (totally 28 cases).

As for two adjacent CEs in the circular structure of the latch, if we denote the node distance between their outputs by $\lambda$, we can get all output-node distances between CEs as and only as $\lambda$, $2\lambda$, $3\lambda$, and $4\lambda$. This is because the CEs are ordered, circulated, and symmetrical as presented in Fig. 3. Hence, we only need four indicative node pairs such as <I1, I2>, <I1, I3>, <I1, I4>, and <I1, I5> for the 28 cases in the presence of an SEDU to prove the self-recoverability for the latch.

In the presence of an SEDU for <I1, I2> resulting in glitches, according to the above-mentioned CEs' feedback rule, the glitch at I1 can propagate to one input of CE2 and one input of CE6, the glitch at I2 can propagate to one input of CE3 and one input of CE7; however, all the other one or two inputs of all the other CEs are not affected by the SEDU. Since a CE can intercept a glitch although one of its inputs is affected, CE6 and CE7 can intercept the glitches. Thus, the outputs of them, i.e., I6 and I7, are correct. Meanwhile, since I6 is fed back to one input of CE3, the output (I3) of CE3 is correct as well. On the other hand, since the outputs of CE8 and CE4 are correct, I1 can restore back to the correct value through CE1, and finally I2 can restore back



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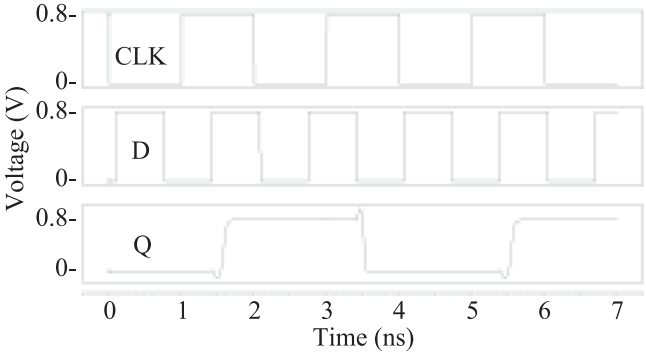


Fig. 5. Simulation results of the DURTPF latch considering error free case.

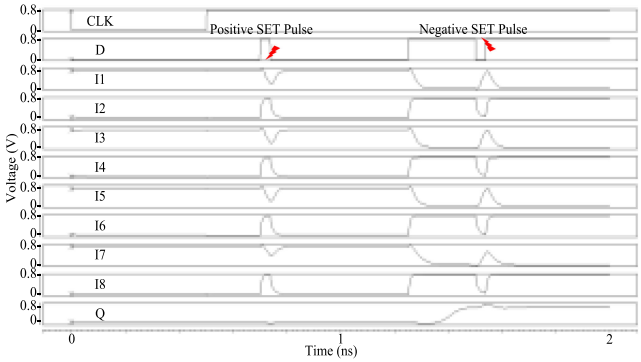


Fig. 6. Simulation results of the DURTPF latch considering the negative and positive SET pulses.

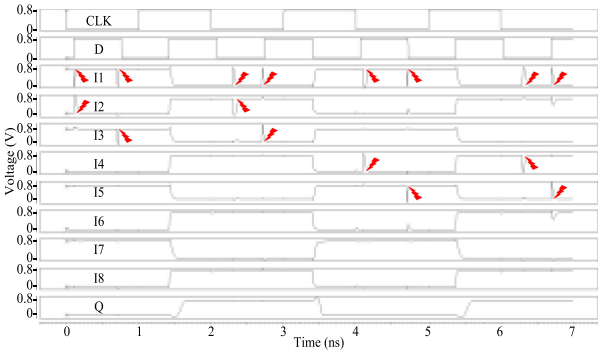


Fig. 7. Simulation results of the DURTPF latch considering SEDUs at key node pairs <I1, I2>, <I1, I3>, <I1, I4>, and <I1, I5>.

to the correct value through CE2. Therefore, the latch can self-recover from the SEDU at <I1, I2>. Similarly, it can be easily known that in the presence of an SEDU for <I1, I3> or <I1, I4> resulting in glitches, they can also self-recover from the SEDU.

In the presence of an SEDU for <I1, I5> resulting in glitches, if the striking-particle has moderate energy, the node pair can still self-recover from the SEDU. This is because the striking-particle induced SEDU only behaves as transient pulses at I1 and I5, and CE2 and CE6 can intercept the small glitches. However, if the striking-particle has higher energy causing an SEDU at the node pair <I1, I5>, the node pair can be flipped causing invalid value retention, since I1 and I5 are the inputs of CE2 and CE6 and the error can propagate to I2 and I6, and finally, to Q through CE3, CE7, and the ST. This case motivates us to propose an enhanced latch version to self-recover from SEDUs for these four indicative node pairs when the striking-particle energy is higher. This enhanced version will be presented in the following section.

As discussed earlier, the latch can properly operate in transparent mode and can retain values in hold mode. Moreover, the latch can filter SET pulses in transparent mode due to the employment of the ST. When the striking-particle has moderate energy, the latch can self-recover from SEDUs in hold mode.

The DURTPF latch was implemented with an advanced 22 nm CMOS technology and the validations for the SET pulse filterability and SEDU self-recoverability of the latch using Synopsys HSPICE tool were performed. The supply voltage was set to 0.8 V. The working temperature was set to room temperature.

The transistor sizes for the latch design are as follows: a) for the normal CEs, the PMOS transistor had W/L = 130/22 nm, the NMOS transistor had W/L = 40/22 nm; b) for the CG based CEs, the PMOS transistor had W/L = 130/22 nm, the NMOS transistor had W/L = 80/22 nm; c) for the ST, the PMOS transistor had W/L = 120/44 nm, the NMOS transistor had W/L = 120/44 nm.

To verify the normal operation of the proposed DURTPF latch, the simulation for the latch considering the error free case was performed as presented in Fig. 5. The simulation results show that the normal operation of the latch in transparent and hold mode is similar to that of a traditional D-latch.

To verify the SET pulse filterability of our proposed DURTPF latch, Fig. 6 shows the simulation results of the DURTPF latch considering the representative negative and positive SET pulses. Note that Fig. 6 is only illustrated for the filtering ability of the latch, and the filterable-pulse widths will be listed and evaluated in Section IV. It can be seen from Fig. 6 that the injected pulses cause nearly no any effect on Q, i.e., these pulses are filtered by the latch. Therefore, the latch is SET pulse filterable. It should be noted that, to filter higher-energy striking-particle-induced large SET pulses, large transistor sizes and/or D to Q transmission delay should be introduced for latches, which will be introduced in Section IV.

To verify the SEDU self-recoverability of the proposed DURTPF latch, Fig. 7 shows the simulation results considering SEDUs at key node pairs <I1, I2>, <I1, I3>, <I1, I4>, and <I1, I5>. As presented in Fig. 7, at 0.3, 0.7, 2.3, 2.7, 4.3, 4.7, 6.3, and 6.7 ns, an SEDU was, respectively, injected at node pairs <I1, I2>, <I1, I3>, <I1, I2>, <I1, I3>, <I1, I4>, <I1, I5>, <I1, I4>, and <I1, I5>, but the node pairs can restore back to the correct values. Therefore, all the key node pairs can self-recover from an SEDU, no matter was the correct value (high or low), i.e., the latch is SEDU self-recoverable for all these key node pairs.



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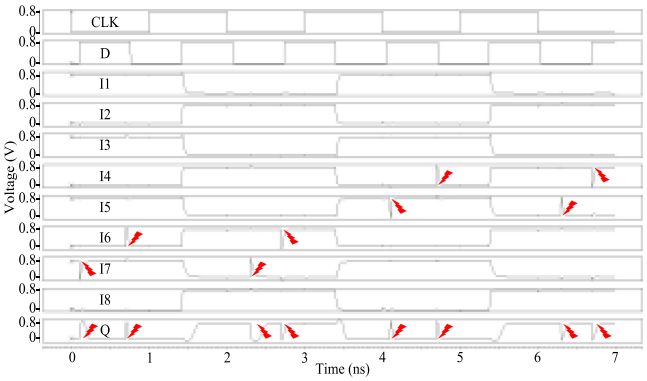


Fig. 8. Simulation results of the DURTPF latch considering SEDUs at key node pairs <I7, Q>, <I6, Q>, <I5, Q>, and <I4, Q>.

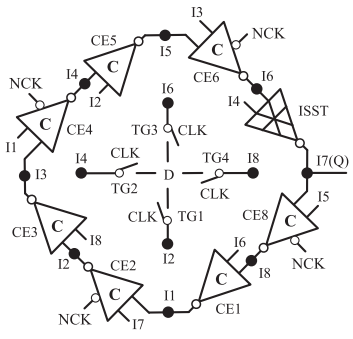


Fig. 9. Circuit schematic of the proposed DURTPF-EV latch design.

On the other hand, as for a node pair including the output of the latch and one of the eight internal nodes I1 to I8, Fig. 8 shows the simulation results for the DURTPF latch considering key node pairs <I7, Q>, <I6, Q>, <I5, Q>, and <I4, Q>. At 0.3, 0.7, 2.3, 2.7, 4.3, 4.7, 6.3, and 6.7 ns, an SEDU was, respectively, injected at node pairs <I7, Q>, <I6, Q>, <I7, Q>, <I6, Q>, <I5, Q>, <I4, Q>, <I5, Q>, and <I4, Q>, and these node pairs can also restore back to the correct values. Therefore, all key node pairs can self-recover from an SEDU no matter was the correct value (high or low), i.e., the latch is SEDU self-recoverable for all these node pairs. Note that the abovementioned simulations were under moderate striking-particle energy (i.e., the injected erroneous charge is up to 8.0 fC).

In summary, simulation results have demonstrated the SET pulse filterability as well as SEDU self-recoverability of the DURTPF latch under moderate striking-particle energy. In the abovementioned simulations, we used a controllable double-exponential current source model to perform the SET and SEDU injections as in [25] to simulate striking-particles. The time constants of the rise and the fall of the current pulse were set to 0.1 and 3.0 ps, respectively.

## B. Proposed DURTPF-EV Latch

The circuit schematic of the proposed DURTPF-EV latch is shown in Figs. 9, and Fig. 10 shows the layout of the DURTPF-EV latch. Based on the DURTPF latch, the DURTPF-EV latch is constructed by replacing CE7 in the DURTPF latch with an ISST, and the original ST

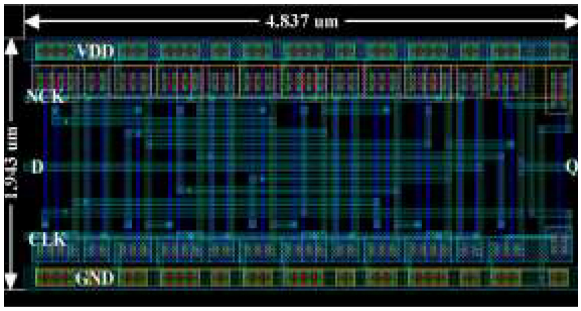


Fig. 10. Layout of the proposed DURTPF-EV latch design.

is removed. Moreover, the feedback rule for the CEs and ISST is enhanced in order to achieve the advanced SEDU self-recoverability, i.e., the DURTPF-EV latch can consistently provide the SEDU self-recoverability when the striking-particle energy is higher.

Note that, the ISST is constructed by splitting the input "In" in Fig. 1(d) into two inputs "In1" and "In2," i.e., the gate terminals of the transistors MP1 and MN2 are connected as "In1" and the gate terminals of the transistors MN1 and MP2 are connected as "In2." By this way, the ISST has the functions of both a CE and an ST. The input D and the clock signals CLK and NCK of the DURTPF-EV latch are the same as those of the DURTPF latch, and I7 is reused for the output of the DURTPF-EV latch.

It can be easily seen that, when the DURTPF-EV latch works in transparent mode, its normal working, and SET pulse filtering principles are similar to those of the DURTPF latch. In the presence of an SEU for the DURTPF-EV latch in hold mode, the SEU recovery principle is also similar to that of the DURTPF latch. However, in the presence of an SEDU for the DURTPF-EV latch in hold mode, a total of $C_8^2 = 28$ node-pair cases must be evaluated to prove that the latch is SEDU self-recoverable under the new feedback rule.

For two adjacent CEs including the ISST, in the circular structure of the latch, similarly, if we denote the node distance between their outputs as $\lambda$, we can get all output-node distances as and only as $\lambda$, $2\lambda$, $3\lambda$, and $4\lambda$. Since the CEs including the ISST are ordered, circulated, and symmetrical as presented in Fig. 9, we only need to consider four indicative node pairs such as <I1, I2>, <I1, I3>, <I1, I4>, and <I1, I5> for the 28 cases in the presence of an SEDU to prove the self-recoverability for the latch.

In the presence of an SEDU for <I1, I2> resulting in glitches, it is obvious that the glitch at I1 can propagate to one input of CE2 and one input of CE4, and the glitch at I2 can propagate to one input of CE3 and one input of CE5. However, all the inputs of all the other CEs or the ISST are not affected by the SEDU. Since a CE can intercept a glitch although one of its inputs is affected, CE3 to CE5 can intercept the glitches and the outputs of them (i.e., I3 to I5) are correct. Since I3 and I5 are fed back to the inputs of CE6, the output (I6) of CE6 is correct as well. This way, I7 and I8 are still correct, making I1 to restore back to the correct value through CE1, and finally, I2 can also restore



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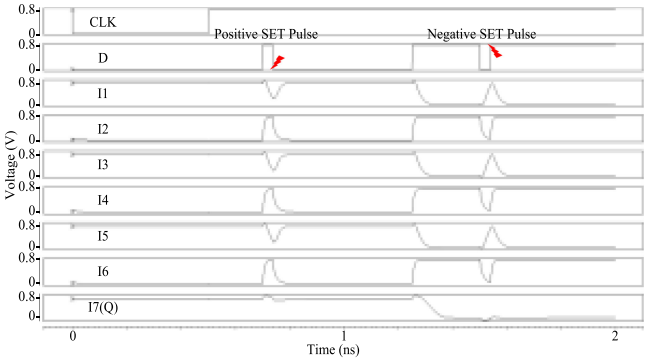


Fig. 11. Simulation results of the DURTPF-EV latch considering the negative and positive SET pulses.

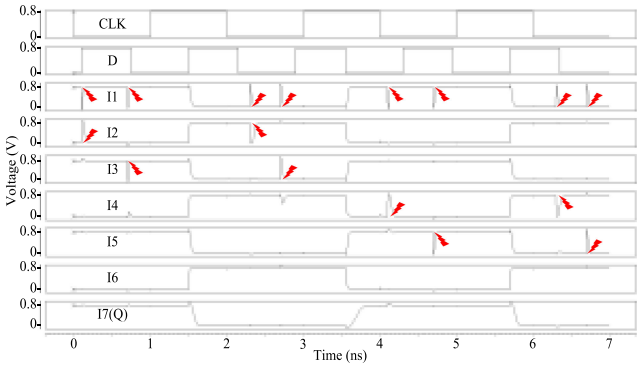


Fig. 12. Simulation results of the DURTPF-EV latch considering SEDUs at key node pairs <I1, I2>, <I1, I3>, <I1, I4>, and <I1, I5>.

back to the correct value through CE2. Therefore, the latch can self-recover from the SEDU at <I1, I2>. Similarly, it can be easily found that in the presence of an SEDU for <I1, I3> or <I1, I4> resulting in glitches, they can also self-recover from the SEDU.

In the presence of an SEDU for <I1, I5> resulting in glitches, it is obvious that the glitch at I1 can propagate to one input of CE2 and one input of CE4, the glitch at I5 can propagate to one input of CE6 and one input of CE8. However, all inputs of all the other CEs are not directly affected by the SEDU. Since a CE can intercept a glitch although one of its inputs is affected, CE2, CE4, CE6, and CE8 can intercept the glitches and the outputs of them (i.e., I2, I4, I6, and I8) are correct. Moreover, I2, I4, I6, and I8 are the inputs of CE1, CE3, CE5, and the ISST, and thus, their outputs I1, I3, I5, and I7 (Q) can restore back to their correct values through CE1, CE3, CE5, and the ISST. Therefore, the latch can self-recover from the SEDU at <I1, I5>. Note that the abovementioned analysis in this section still holds true for the case of higher striking-particle energy, and the amount of the injected current charge will be introduced in the following.

As discussed earlier, the latch can properly operate in transparent mode and can retain values in hold mode. In addition, the latch can filter SET pulses in transparent mode and can self-recover from SEDUs in hold mode, i.e., the latch is SEDU self-recoverable and SET pulse filterable. In the following, SEDU simulation results will be shown under the assumption of higher striking-particle energy.

Using all the same design parameters for the DURTPF latch, the DURTPF-EV latch was also implemented. Comprehensive simulation results demonstrate that the normal operation of the DURTPF-EV latch in transparent and hold mode is still similar to that of a traditional D-latch.

Figs. 11–13 show the simulation results considering SETs and SEDUs. It can be seen from Fig. 11 that the DURTPF-EV latch can still effectively filter SET pulses. Note that Fig. 11 is only illustrated for the filtering ability of the DURTPF-EV latch, and the filterable-pulse widths will be listed and evaluated in Section IV. For the SEDU self-recoverability verification, a striking-particle with higher

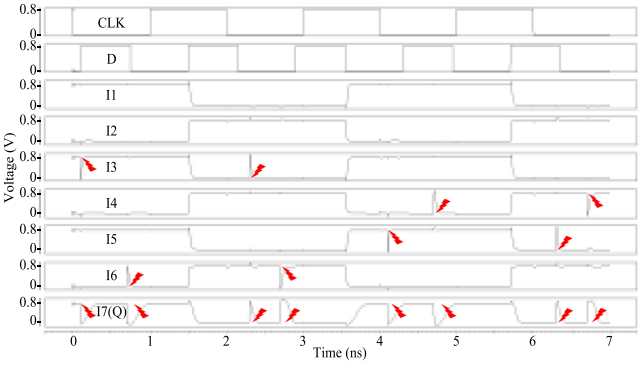


Fig. 13. Simulation results of the DURTPF-EV latch considering SEDUs at key node pairs <I7, Q>, <I6, Q>, <I5, Q>, and <I4, Q>.

energy (i.e., the smallest injected current charge is about 11.0 fC, which is large enough to simulate the worst case operations for the latch) was assumed. Note that, the verification methodology is the same as that of the DURTPF latch as described in the abovementioned section. Thus, the validation results are directly described here. It can be seen from Figs. 12 and 13 that, the DURTPF-EV latch can effectively self-recover from an SEDU at key node pairs <I1, I2>, <I1, I3>, <I1, I4>, <I1, I5>, <I3, Q>, <I4, Q>, <I5, Q>, and <I6, Q>, respectively, under higher striking-particle energy. Note that, for the sake of brevity, the redundant signal I8 is omitted in Figs. 11 to 13.

## IV. LATCH COMPARISON AND EVALUATION RESULTS

To make a fair quantitative comparison, the latch designs reviewed in Section II were implemented using the same parameters as the proposed latch designs. Detailed comparison results among the latch designs including ours are presented in Table I, with respect to the average (dynamic and static) power dissipation, D to Q transmission delay (i.e., the average of rise and fall delays of D to Q), silicon area, average filterable-SET-pulse width (AFSW), power-delay-width product (PDWP), and SET pulse filtering ability (SPFA), respectively. The PDWP and SPFA calculation



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TABLE I
Comparison Results for Alternative SEU/SEDU/SET Hardened Latch Designs

| # | Latch Name | Ref. | Overhead | | | AFSW (ps) | PDWP | SPFA (%) |
|---|---|---|---|---|---|---|---|---|
| | | | Power (μW) | Delay (ps) | $10^2$×Area ($\mu m^2$) | | | |
| 1 | TMR | - | 1.51 | 47.67 | 13.52 | - | 71.98 | - |
| 2 | DET-SEHP | [14] | 1.52 | 154.52 | 5.89 | 118.41 | 54.89 | 76.63 |
| 3 | LCHR | [15] | 0.98 | 111.02 | 7.93 | 39.08 | 70.50 | 35.20 |
| 4 | FERST-EV | [16] | 1.25 | 73.84 | 6.15 | 43.42 | 38.03 | 58.80 |
| 5 | RFC | [17] | 0.45 | 4.58 | 4.82 | - | 2.06 | - |
| 6 | CLCT | [24] | 0.65 | 31.68 | 5.85 | - | 20.59 | - |
| 7 | DNCS | [25] | 1.72 | 63.12 | 10.21 | - | 108.57 | - |
| 8 | NTHLTCH | [26] | 2.87 | 16.19 | 12.42 | - | 46.47 | - |
| 9 | DeltaDICE | [27] | 1.95 | 7.09 | 14.32 | - | 13.83 | - |
| 10 | DOUNT | [28] | 2.96 | 20.24 | 10.32 | - | 59.91 | - |
| 11 | DURTPF | Proposed | 0.93 | 135.65 | 12.83 | 78.19 | 53.44 | 57.64 |
| 12 | DURTPF-EV | Proposed | 0.82 | 109.83 | 12.08 | 48.57 | 50.23 | 44.22 |

formulas are given as follows:

$$\text{PDWP} = \text{Power} \times \big(\text{Delay} - \text{Width}\big) \quad (1)$$

$$\text{SPFA} = \big(\text{Width}/\text{Delay}\big) \times 100\%. \quad (2)$$

In the abovementioned formulas, power is the average power dissipation, delay is D to Q transmission delay, and width is the AFSW whose value is not available for SET-not-filterable latch designs. It can be seen that, among the same type latch designs (e.g., SET pulse filterable ones), a smaller PDWP, and/or a larger SPFA is better.

It can be seen from Table I that, in order to ensure SEDU self-recoverability and SET pulse filterability, larger silicon area is needed for the proposed DURTPF latch. However, compared with SET pulse filterable (second to fourth) or the SEDU self-recoverable (eighth to tenth) latches, our proposed latches have the smallest power dissipation due to the use of the CG technology. As for the DURTPF-EV latch, the delay is smaller than the DURTPF latch since a few transistors are employed between the input and the output of the latch. Besides, the SPFAs of the FERST-EV latch and the DET-SHEP latch are large due to the multiple-level filtering mechanism of CEs; however, the SPFA of our proposed latch designs is comparable to that of most of the SET filterable latches.

To make further detailed quantitative comparisons, the relative overhead in terms of power (ΔPower), delay (ΔDelay), area (ΔArea), and PDWP (ΔPDWP) among the reference latch designs compared with our designs have been listed in Tables II–V, and the calculation formula is given as follows:

$$\Delta = \big(\text{Compared} - \text{Proposed}\big)/\text{Compared} \times 100\%. \quad (3)$$

As for the DURTPF latch, it can be seen from Table II that, to perform both SEDU and SET hardening, compared with the SEDU self-recoverable latches, our latch consumes 5.74% extra silicon area on average. However, owing to the employment of the CG technology, our latch saves about 62.83% power dissipation on average, and these compared latches are not SET filterable. Note that the ΔDelay is not suitable for comparisons since these latches and ours are not of the same type. Table III presents comparisons of SET pulse filterable latches. It can be seen from Table III that, compared with the SET pulse filterable latches, all the average data of our DURTPF latch are not bad except for ΔArea since our latch can achieve not only SEDU self-recoverability under moderate striking-particle energy

TABLE II
Relative Overhead of SEDU Self-Recoverable Latch Designs Compared With the DURTPF Latch

| Latch Name | ΔPower (%) | ΔDelay (%) | ΔArea (%) |
|---|---|---|---|
| NTHLTCH [26] | 67.60 | - | -3.30 |
| DeltaDICE [27] | 52.31 | - | 10.41 |
| DONUT [28] | 68.58 | - | -24.32 |
| Average (Savings of ours) | 62.83 | - | -5.74 |

TABLE III
Relative Overhead of SET Pulse Filterable Latch Designs Compared With the DURTPF Latch

| Latch Name | ΔPower (%) | ΔDelay (%) | ΔArea (%) |
|---|---|---|---|
| DET-SEHP [14] | 38.82 | 12.21 | -117.83 |
| LCHR [15] | 5.10 | -22.19 | -61.79 |
| FERST-EV [16] | 25.60 | -83.71 | -108.62 |
| Average (Savings of ours) | 23.17 | -31.23 | -96.08 |

TABLE IV
Relative Overhead of SEDU Self-Recoverable Latch Designs Compared With the DURTPF-EV Latch

| Latch Name | ΔPower (%) | ΔDelay (%) | ΔArea (%) |
|---|---|---|---|
| NTHLTCH [26] | 71.43 | - | 2.74 |
| DeltaDICE [27] | 57.95 | - | 15.64 |
| DONUT [28] | 72.30 | - | -17.05 |
| Average (Savings of ours) | 67.23 | - | 0.44 |



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TABLE V
Relative Overhead of SET Pulse Filterable Latch Designs Compared With the DURTPF-EV Latch

| Latch Name | ΔPower (%) | ΔDelay (%) | ΔArea (%) |
|---|---|---|---|
| DET-SEHP [14] | 46.05 | 28.92 | -105.09 |
| LCHR [15] | 16.33 | 1.07 | --52.33 |
| FERST-EV [16] | 34.40 | -48.74 | -96.42 |
| Average (Savings of ours) | 32.26 | -6.25 | -84.61 |

TABLE VI
Simulation Results using Differently Sized ST for the DURTPF Latch

| ST Transistor Sizes (Length, Width) (nm) | Power (uW) | Delay (ps) | $10^2$×Area ($\mu m^2$) | AFSW (ps) | SPFA (%) |
|---|---|---|---|---|---|
| (44,120) | 0.93 | 135.65 | 12.83 | 78.19 | 57.64 |
| (88,120) | 1.03 | 279.23 | 16.00 | 127.56 | 45.68 |
| (44,240) | 1.28 | 163.97 | 16.00 | 101.88 | 62.13 |
| (88,240) | 1.46 | 316.38 | 22.33 | 166.32 | 52.57 |

but also SET filterability at the cost of extra silicon area. In summary, we have introduced redundant silicon area to achieve high reliability and low power for the proposed DURTPF latch.

As for the DURTPF-EV latch, it can be seen from Table IV that, compared with the SEDU self-recoverable latches, the DURTPF-EV latch saves about 0.44% silicon area on average. In addition, due to the employment of the CG technology and a few transistors, the DURTPF-EV latch saves about 67.23% power dissipation on average. However, these SEDU self-recoverable latches are not SET filterable. Moreover, it can be seen from Table V that, compared with the SET pulse filterable latches, all the simulation data of the DURTPF-EV latch are not bad except for ΔArea since the SEDU self-recoverability and the SET filterability of the DURTPF-EV latch are still at the cost of extra silicon area. The increase in silicon area may make our latch vulnerable to soft errors. However, our latch can online self-recover from SEUs and SEDUs and can filter SET pulses. In summary, we have introduced redundant silicon area to achieve high reliability and low power for our proposed latches. Meanwhile, compared with the DURTPF latch, the DURTPF-EV latch can save more power dissipation, delay, and PDWP, making the DURTPF-EV latch more suitable for low-orbit aerospace applications that require high reliability and low cost. Note that propagation-induced pulse broadening (PIPB) not occur through simulations in the proposed latches. PIPB mainly occur in combinational logic circuits [33].

ST and ISST can filter SET pulses, but different transistor sizes of ST and ISST can cause different SET-filtering ability and latch overhead. Tables VI and VII show the simulation results using differently sized ST and ISST for the proposed DURTPF and DURTPF-EV latches, respectively. It can be seen from these tables that increasing ST/ISST transistor sizes can provide large AFSW especially when only the width parameters of transistors are enlarged. However, the overhead in terms of power, delay, and area has to be introduced and the SPFA cannot be significantly enhanced. Therefore, the small transistor sizes of the ST and ISST as indicated in Tables VI and VII can provide a better balance between reliability and overhead of the proposed latches.

TABLE VII
Simulation Results Using Differently Sized ISST for the DURTPF-EV Latch

| ISST Transistor Sizes (Length, Width) (nm) | Power (uW) | Delay (ps) | $10^2$×Area ($\mu m^2$) | AFSW (ps) | SPFA (%) |
|---|---|---|---|---|---|
| (44,120) | 0.82 | 109.83 | 12.08 | 48.57 | 44.22 |
| (88,120) | 0.86 | 274.78 | 15.25 | 86.95 | 31.64 |
| (44,240) | 1.04 | 108.62 | 15.25 | 56.46 | 51.98 |
| (88,240) | 1.14 | 264.47 | 21.59 | 101.83 | 38.50 |

## V. CONCLUSION

Technology scaling has made soft errors, such as SEUs, SEDUs, and SETs, a serious concern in advanced nanoscale CMOS technologies. However, most of the typical latch designs are either not hardened simultaneously against SEDUs and SETs, or they incur excessive overhead especially in terms of power dissipation, making them not suitable for low-orbit aerospace applications where both high reliability and low cost are required. This article has proposed a DURTPF latch design, which is SET pulse filterable and SEDU self-recoverable in the case of moderate striking-particle energy. This article has further proposed an enhanced version of DURTPF, namely DURTPF-EV, which is SEDU self-recoverable even in the case of higher striking-particle energy. Comprehensive simulations have demonstrated the SET pulse filterability, SEDU self-recoverability, and low-power consumption of the proposed latch designs at the cost of moderate silicon area overhead. Compared with DURTPF, DURTPF-EV is more robust and low power, making it more suitable for low-orbit aerospace applications that require high reliability and low cost.

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