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***Abstract*—Aging and soft errors are the two most critical reliability issues for nanoscale CMOS circuits. The soft error becomes more severe if the circuit performance degraded with the aging. In this paper, we address the issue of analyzing the effects of Negative Bias Temperature Instability (NBTI) mechanisms on Integrated Circuit's (ICs') soft error susceptibility. We first analyzed the critical charge sensitivity of two-input NAND gate for various operating temperatures with three years of stress. Results show that the critical charge decreases with the temperature and has the maximum degradation of 19.98% if the input AB is at 01 logic compare to 12.06%, 16.8%, and 11.15% for 00, 10, and 11. Further, we validated the results with c17 from ISCAS'85 benchmark suite to estimate the soft error. The critical charge at the sensitive node of the c17 circuit is decreased by 9.87% for the worst case input pattern 00010. Thus thorough investigation of the critical charge provides a measure for the soft error susceptibility with the NBTI effect on ICs.**

***Index Terms*—NBTI, Circuit simulation, Soft error, Reliability, ISCAS'85 benchmark circuit.**

I. Introduction

With the scaling of CMOS technology, variability between identical transistors and reliability challenges have become more important for the performance and lifetime of integrated circuits. In this context, negative bias temperature instabilities (NBTI) and positive BTI (PBTI) play an important role for NMOS and PMOS transistors. Experimental investigations clearly reveal that NBTI in PMOS transistors is more severe compared to PBTI in NMOS transistors. Thus, NBTI is generally considered to be the dominant limiting factor of a device lifetime and to some extend also of circuit lifetime [1]. In more detail, NBTI refers to the stress case when a negative bias is applied at the gate contact of the transistor. This negative bias can trigger the creation of so-called interface states and oxide defects, which lead to a drift of the threshold voltage, reduction of the sub-threshold slope and to a reduction of the on-current [1]. When the gate stress is released the shift of the threshold voltage accumulated during stress phase partially recovers. The permanent shift of the threshold voltage is particularly disadvantageous for CMOS circuits, as it can introduce some uncertainty in the device and circuit behaviour and can lead to a decrease of the device/circuit lifetime [2].

Along with susceptibility to NBTI, nanoscale devices are more sensitive to radiation-induced errors, which also aggravates the noise immunity of the circuits [3]. Also, the recent technology generation operates at low supply voltages which can reduce the circuit node capacitances, but increase the probability of soft errors [4]. When high energy particles, like alpha particles from impurities in the packaging material or neutrons from cosmic rays, strike on a sensitive node of the circuit or on a sensitive region of the semiconductor device, they may lead to single event upset (SEU) or single event transient (SET) which can hamper the proper functionality of the circuit, and lead to soft errors [5][6]. Single event upset (SEU) is the most common type of single event effects (SEE) occurring in storage elements (latches and memory cells), which can flip the logic state of a circuit. In combinational circuits SETs can be induced which may cause an additional current that propagates through the logics and lead to soft errors [7]. Direct ionization from secondary protons in combination with the low operation voltage of scaled CMOS circuits reduces the critical-charge ($Q_{\rm crit}$) [8]. The critical charge is the minimum charge required to flip the logic.

In this work we assess the effect of NBTI aging on reliability implications of CMOS circuits when the soft error radiation hardening enhancement is considered. We compute and compare the critical charge sensitivity to evaluate the worst-case input combination for a two input NAND gate which is maximum susceptible to soft errors. We further implement the c17 benchmark circuit from ISCAS'85 suite [9] and study the most sensitive node which is responsible to propagate the SET to the output of the circuit and may affect the results in subsequent stages.

II. Radiation hardening analysis methodology

To study the performance of circuits considering device aging due to NBTI, we used the PTM 32nm CMOS technology and evaluated using HSPICE MOSRA model [10]. All the simulations are performed considering a supply voltage $V_{\rm dd}$ = 0.9V and the operating temperature is set to 125°C.

A. Soft Error Rate

The soft error resilience of any circuit can be evaluated from its $Q_{\rm crit}$. The soft error rate (SER) has exponential dependency on $Q_{\rm crit}$ and it is observed that the higher value of $Q_{\rm crit}$ directly translates into lower SER [11]. SER can be express as

$$SER \propto N_{\rm flux} A e^{-\frac{Q_{\rm crit}}{Q_{\rm S}}} \tag{1}$$

where $N_{\rm flux}$ is the neutron flux intensity, A is the cross section area of the sensitive node, and $Q_{\rm S}$ is the charge collection efficiency of the device in fC.

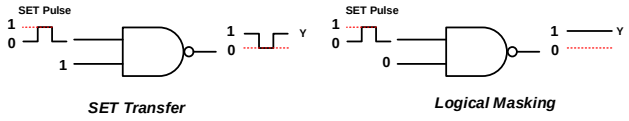


Fig. 1: Logical masking of the SET shown for two-input NAND gate.

For the validation of soft error enhancement on two input NAND gate for different input combinations, the approximate soft error rate ratio with and without stress (SERR) is introduced. The SERR is calculated by assuming all other device parameters unaffected except $Q_{\rm crit}$ at the used operating temperature and is given by

$$SERR \approx \text{ antilog}_e \left[Q_{\rm crit}^{\rm 3Years} - Q_{\rm crit}^{\rm 0Year}\right]\Big|_{@T} \qquad (2)$$

where $Q_{\rm crit}^{\rm 0Year}$ and $Q_{\rm crit}^{\rm 3Years}$ are the critical charges without stress and after 3 years of NBTI stress, respectively.

B. Masking Factors

The masking of the SET from the logic input is one of the way to improve the immunity of a circuit to radiation. The factors like sensitization that affect the circuit by propagating SET to the output of the circuit and cause a soft error can be used for this purpose. The logical masking of any circuit depends on the input pattern, which is applied to the given circuit. Fig. 1 shows the two possible combinations for the sensitization and logical masking for a two-input NAND gate. If one of the inputs is at logic high, a possible SET occuring at the other input at the same time will be directly transferred to the output. Whereas if one of the two inputs is at logic low state, the SET occuring at other input terminal is logically masked and it will not be transferred to the output and thus the SET will not affect subsequent stages. The probability of logical masking for any circuit is given by [12]

$$P_{\text{Logical masking}} = 1 - P_{\text{Sensitization}} \qquad (3)$$

where $P_{\text{Sensitization}}$ is the sensitization probability and $P_{\text{Logical masking}}$ is the logical masking probalility.

III. Single Event Transient Effect on Circuit Performance

Fig. 2 shows the simulation setup for a two-input NAND gate. In the simulation, the effect of the SET strike is considered to occur on all the transistors. The parallel PMOS transistors are sensitive to the particle strike when both M1 and M2 are under stress and we inject SET current into the circuit node Y. In this situation, the active area for strike includes drain area of both of the PMOS transistors. On the other hand, if we inject SET current with opposite direction then it will perform strike on M3. Similarly, if a SET current is injected at node N, it will perform strike on M4 [13]. Here, we have considered a SET strike on only PMOS transistors because the effect of NBTI is more severe for PMOS transistors.

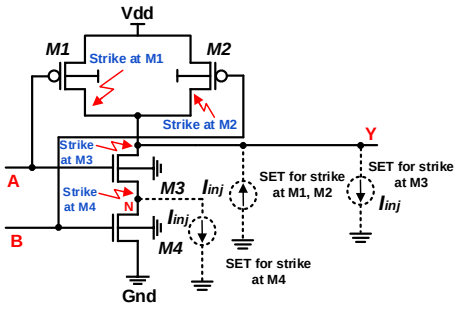


Fig. 2: Possible particle strikes on the all four transistors and their equivalent SET current source injecting into the sensitive node of two-input NAND gate.

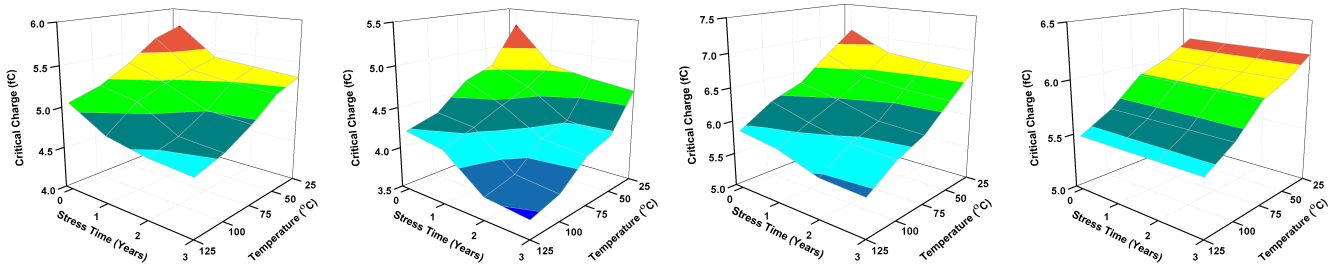
A. Critical Charge Analysis

Fig. 3 shows the critical charge of a two-input NAND gate as a function of the temperature and stress time for the four possible input combinations. Results demonstrate that the input combinations AB = 01 and AB = 10 exhibit the lowest and highest critical charge compared to the two other input combinations, respectively. It indicates that the two-input NAND gate is more susceptible to the soft errors at the input combinations of AB = 01. The critical charge decreases with increasing stress time and temperature. It is also observed that the rate of critical charge decrement for the input combinations 00, 01, 10, and 11 are 12.06%, 19.98%, 16.8%, and 11.15% if the operating temperature increases towards 125°C starting from 25°C. Similarly, the decrement in critical charge is 12.22% after the stress time of 3 years for the input combination AB = 01, which is the highest value observed among all the possible combinations.

From the above results, we conclude that the two-input NAND gate has a minimum critical charge at AB = 01 indicating that the effect of the soft error is high for this input combination. We have considered this input combination for further analysis in Fig. 4(a), which shows the critical charge variation for different supply voltages, considering different load capacitances. As can be seen, the critical charge of the sensitive node increases with the supply voltage due to the higher current flowing from the supply to the node and thus providing more charge collection capability. In other words, an increase of the load capacitance also increases the effective circuit capacitance and thus a higher charge is required to unintendedly flip the logic.

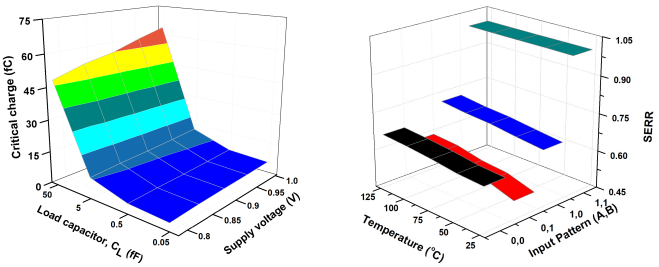
B. Soft Error Analysis

For the resistivity of the two-input NAND gate against soft errors, the soft error rate ratio (SERR) has been evaluated. Fig. 4(b) shows the SERR after three years of stress at different operating temperatures. It is observed that the SERR increases with temperature for three possible input combinations of two-input NAND gate. In the case of AB = 11 the opposite trend is observed because we have considered NBTI in PMOS transistors. The change in SERR with change in temperature



(a) A,B = 0,0 (b) A,B = 0,1 (c) A,B = 1,0 (d) A,B = 1,1

Fig. 3: Critical charge of the two input NAND gate as a function of temperature for different stress times with different input patterns.



(a) (b)

Fig. 4: (a) Two-input NAND gate critical charge characteristics shown at different supply voltages for various load capacitors (C_L). (b) Soft error rate ratio (SERR) with stress time at various operating temperatures for all possible input combinations of two input NAND gate.

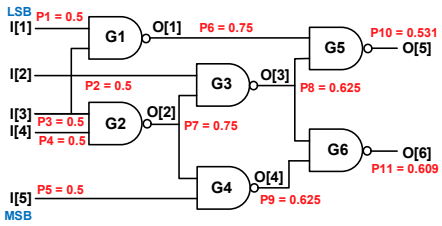


Fig. 5: Schematic of the c17 circuit from ISCAS'85 benchmark suite. P_1 through P_{11} are the input and output signal probabilities for six NAND gates of the c17 circuit.

from 25°C to 125°C for the input combinations AB = 00, AB = 01, and AB = 10 are 0.036, 0.072, and 0.046, respectively. Thus, the two-input NAND gate is most sensitive to soft errors at the input combination of AB = 01. To extend our analysis, we use the c17 circuit from the ISCAS'85 benchmark suite is explained in subsequent section.

IV. ISCAS'85 C17 BENCHMARK CIRCUIT

Fig. 5 shows the c17 circuit which consists of six NAND gates. For circuit, one has to identify the worst case input pattern where the most PMOS transistors are stressed during normal operation. As we primarily focus on the NBTI for PMOS case, the transistors are stressed when a logical low state is applied at the respective input of the NAND blocks. Fig. 5 shows the probabilities of getting logic high at each node of the circuit, P_1 through P_{11}, and are computed by applying all possible input pattern combinations to the inputs I[1]-I[5] of the circuit. The signal probability for each inputs I[1]-I[5] is considered to be 0.5, as the probability of primary input being 0 or 1 is assumed to be equal. The total degradation of the PMOS transistor due to NBTI depends on the input signal probability. Furthermore, the impact of NBTI on the entire c17 circuit depends on the input and output signal probability of each NAND gate, which is again the input probability of a subsequent NAND gate.

From Fig. 5 it can be observed that gates G1 and G2 have the highest probability to be stressed, as one or both inputs see the logic low state more frequently than the inputs of other NAND gates. NAND gate G5 has the minimum probability of being stressed during operation. Out of total 12 PMOS transistors, seven and three PMOS transistors are stressed for worst case stress patterns and minimum stress patterns respectively, of the twelve PMOS transistors of six NAND gates of the c17 circuit. The input patterns leading to maximum number of stressed PMOS transistors (00010 and 10010) are further used to analyse the degradation of the c17 circuit.

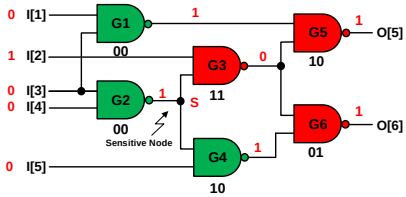
A. *Sensitization and Logical Masking*

Fig. 6(a) shows the logical masking and sensitization probabilities of all NAND gates in the c17 benchmark circuit. It can be observed that the logical masking decreases when the number of stages increases.

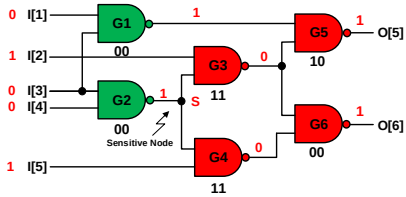
For further analysis, the two worst-case input combinations (00010 and 10010) having the maximum number of PMOS transistors under stress are considered. The logical masking and sensitization of NAND gates on the c17 circuit for the most critical input patterns are shown in Fig. 6. For the input pattern 00010, the gates G1, G2, and G4 are logically masked. As the output node (S) of G2 transfer the logic to the next stage, it is the primarily sensitive node in the c17 circuit. If a high energy particle strikes at the sensitive node in the circuit, it will transfer the SET to the outputs through G3, G5, and G6 as shown in Fig. 6(b). The effect of the soft error to NAND gate G6 is higher as compared to G5 because the critical charge for the NAND gate input combination 01 is the smallest among all other possible combinations. Thus the

NAND Gates	$P_{\text{Sensitization}}$	$P_{\text{Logical-masking}}$
G1	0.25	0.75
G2	0.25	0.75
G3	0.375	0.625
G4	0.375	0.625
G5	0.4375	0.5625
G6	0.4375	0.5625

(a)



(b)



(c)

Fig. 6: (a) Sensitization and Logical masking probabilities of all NAND gates of the c17 circuit. Logical masking of the SET of the c17 circuit for two input combinations having maximum stressed PMOS transistors (b) For the input pattern 00010, and (c) for the input pattern 10010. The logically masked NAND gates are represented in green whereas unmasked as represented in red.

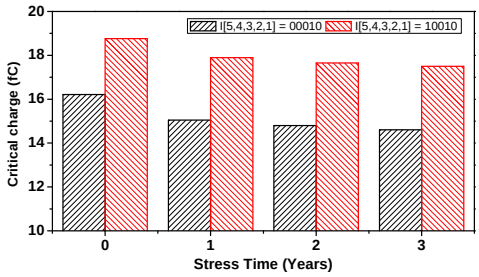


Fig. 7: Critical charge at the sensitive node (S) of c17 circuit for two worst case input combinations with the different stress time.

transfer of SET to the O[6] will be higher as compared to the output O[5]. Similarly for the input pattern 10010, gates G1 and G2 are logically masked. If a high energy particle strikes at the sensitive node (S) in the circuit, it will transfer the SET to the outputs through G3, G4, G5, and G6 as shown in Fig. 6(c).

B. Effect of SET on c17 Circuit

Fig. 7 shows the critical charge at the sensitive node (S) of the c17 circuit for the input leading to maximum net stress for PMOS transistors, which is considered to be three years of stress time. The result shows that the critical charge decreases with the stress time for both input combinations. The critical charge at the sensitive node (S) for input combination 00010 is lower than 10010 and thus, the effect of SET is higher for 00010. The critical charge for the c17 circuit is decreased by 9.87% for the input combination 00010 after the stress time of 3 years, whereas, the critical charge is decreased by 6.72% in case the pattern 10010 is applied. This indicates that the soft error hardening of the circuit seriously depends on the NBTI stress of the PMOS transistor, on the selected input pattern of the circuit, and on the logical masking and sensitization probability of the gates involved in the circuit.

V. Conclusion

Performance degradation of transistors due to NBTI and single event transients occuring in ICs might give rise for instable electronic applications. We analyze the effect of NBTI on the soft error susceptibility on NAND gates as well as on the ISCAS'85 c17 benchmark circuit. We showed that NBTI significantly reduces the critical charge at the sensitive nodes of the circuits. We further introduced a soft error rate ratio (SERR) to validate the effect of NBTI at various operating temperatures and observed that the NAND gate is more sensitive to soft error at the input combination AB = 01. Further, we also determined the critical charge of the sensitive node for all possible worst-case input combinations of c17 benchmark circuit. The result indicates that the c17 circuit is more sensitive to the soft error if the maximum number of PMOS transistors are under stress.

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