HITTSFL: Design of a Cost-Effective HIS-Insensitive TNU-Tolerant and SET-Filterable Latch for Safety-Critical Applications

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***Abstract*—This paper proposes a cost-effective, high-impedance-state (HIS)-insensitive, triple-node-upset (TNU)-tolerant and single-event-transient (SET)-filterable latch, namely HITTSFL, to ensure high reliability with low-cost. The latch mainly comprises an output-level SET-filterable Schmitt-trigger and three inverters that make the values stored in three parallel single-node-upset (SNU)-recoverable dual-interlocked-storage-cells (DICEs) converge at a common node to tolerate any possible TNU. The latch does not use C-elements to be insensitive to the HIS. Simulation results demonstrate the TNU-tolerability and SET-filterability of the proposed HITTSFL latch. Moreover, due to the use of clock-gating technologies and fewer transistors, the proposed latch can reduce delay, power, and area by 76.65%, 6.16%, and 28.55%, respectively, compared with the state-of-the-art TNU hardened latch (TNUHL) that cannot filter SETs.**

I. Introduction

With the aggressive scaling of semiconductor technologies, the advanced nano-scale integrated circuits and systems are becoming increasingly vulnerable to soft-error-induced reliability issues. In CMOS technologies, soft errors are mainly caused by radioactive striking-particles, such as neutrons, protons, heavy ions, alpha particles, and electrons [1-2]. Soft errors include *single-node upset* (*SNU*), *double-node upset* (*DNU*), *triple-node upset* (*TNU*), *single-event-transient* (*SET*), etc. In nano-scale CMOS technologies, a high-energy striking-particle can easily invalidly change the logic state of a node in a storage cell, resulting in an SNU; in a combinational circuit, a high-energy striking-particle can easily result in a transient faulty pulse at the output of a logic gate, i.e., an SET pulse. If an SET propagates through logic gates arriving at a downstream storage cell, it may be captured by the cell, resulting in invalid value-retention [3]. However, in the advanced highly-integrated nano-scale CMOS technologies, due to charge-sharing, a high-energy striking-particle can unfortunately simultaneously change the logic states of double nodes in a storage cell, resulting in a DNU. The scenario that triple nodes are simultaneously affected is called a TNU [4-8]. Obviously, reliability design against soft errors only targeting SNUs and/or SETs are no longer sufficient for high reliability requirements in safety-critical applications. Therefore, it is crucial to design not only SNU/DNU/TNU-tolerant but also SET-filterable storage cells to construct highly reliable circuits and systems for safety-critical applications.

To mitigate SNUs, DNUs, TNUs, and/or SETs, by means of *radiation-hardening-by-design* (*RHBD*) approaches, many hardened storage cells such as *static random access memories* (*SRAMs*) [9-12], flip-flops [13-16], and latches [5-8, 17-27], have been proposed. This paper focuses on latches. Among these latches, using temporal redundancies such as introducing delay elements and/or SET-filterable components, some of them are SET-filterable [19-20]; using spatial redundancies such as introducing redundant hold nodes, *triple-modular redundancy* (*TMR*), and *double-level error-interception* (*DLEI*), some of them can tolerate SNUs [17-18, 20, 24, 25] and some of them can tolerate *multiple-node-upsets* (*MNUs*) that include DNUs and TNUs [5-8, 21-23, 25, 27]. However, some of these state-of-the-art latches still suffer from some problems such as the following.

1) They cannot provide complete TNU-tolerability [17-26] since there is at least one counterexample that an invalid value will be retained if any of them suffers from a TNU.
2) They cannot provide SET-filterability [5-8, 17-18, 21, 23-27] since SETs can unfortunately propagate to the output from the input for any of them.
3) They cannot simultaneously provide complete TNU-tolerability and SET-filterability. To the best of our knowledge, there is no latch that can simultaneously have these abilities.
4) They are sensitive to *high-impedance state* (*HIS*) due to the use of *C-elements* (*CEs*) [5-6, 8, 17, 27]. Moreover, some latches have to use a TMR-voter, delay element, and/or extra redundant device, leading to large overhead.

In this paper, a novel cost-effective, *HIS-Insensitive, TNU-Tolerant and SET-Filterable Latch* (*HITTSFL*) design is for the first time proposed. The latch is mainly constructed from three parallel SNU-self-recoverable *Dual-Interlocked-storage-Cells* (*DICEs*) [28] to store values as well as three inverters to make the stored values converge at the input of a *Schmitt-trigger* (*ST*). The converged node feed the SET-filterable ST and cannot retain a TNU-induced flipped-value due to current-competition, enabling the latch to tolerate possible TNUs and filter possible SETs. The latch is insensitive to the HIS due to the disuse of C-elements, making the latch more reliable for safety-critical applications. Simulation results demonstrate the TNU-tolerability and SET-filterability of the proposed HITTSFL latch. Moreover, due to the use of *clock-gating* (*CG*) technologies and fewer transistors, the proposed latch has low overhead in terms of power dissipation and silicon area, compared with the state-of-the-art TNU-tolerant latches that cannot filter SETs.

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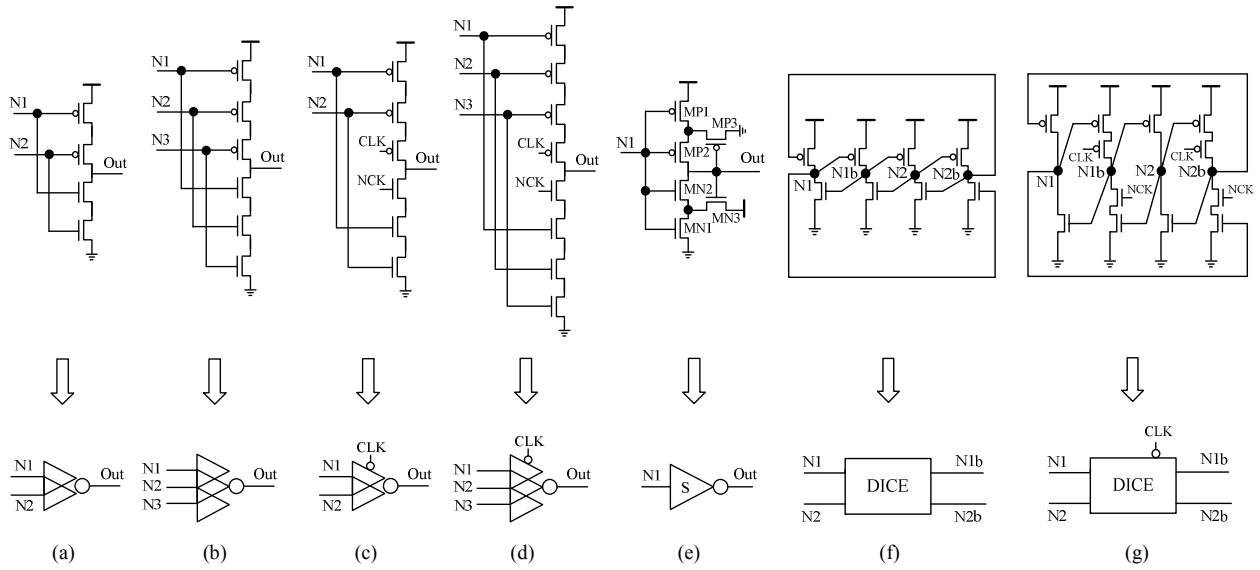


Fig. 1. Schematics of widely used components in previous hardened latches. (a) 2-input C-element. (b) Clock-gating based 2-input C-element. (c) 3-input C-element. (d) Clock-gating based 3-input C-element. (e) Schmitt-trigger. (f) Dual-interlocked-storage-cell (DICE). (g) Clock-gating based DICE.

The rest of the paper is organized as follows: Section II reviews previous hardened latch designs. Section III presents the schematic, working principles, and verifications of the proposed latch design. Section IV provides comparison and evaluation results. Section V concludes the paper.

II. Previous Hardened Latch Designs

This section reviews typical previous hardened latch designs, namely DET-SEHPL [19], LSEH [20], DNURL [21], THLTCH [22], TNUDICE [6], and TNUHL [5]. In these designs, some components such as CEs, STs, and DICEs are widely used, and Fig. 1 shows schematics of them. Fig. 1-(a) and (b) show the 2-input and 3-input CEs and the 4-input CE can be easily created. A CE can work as an inverter if its inputs have the same value and its output will temporally keep the previous correct value if its inputs become having different values. However, if its inputs keep different values for an extended period of time, its output will enter into the HIS, floating to an unknown value. A CE is also controllable by the *system clock* (*CLK*) and *negative system clock* (*NCK*) signals. Fig. 1-(c) and (d) show the CG-based CEs. Fig. 1-(e), (f), and (g) show the ST, the DICE, and the CG-based DICE. Details about STs and DICEs will be introduced in the next section.

Fig. 2 shows the schematics of previous hardened latches. In Fig. 2, the switches marked with CLK or NCK are *transmission gates* (*TGs*). For clock-signal connections to a TG, e.g., if it is marked with CLK, CLK is connected to the gate terminals of its PMOS transistors and NCK is connected to the gate terminals of its NMOS transistors. This rule is applicable to all latches in this paper.

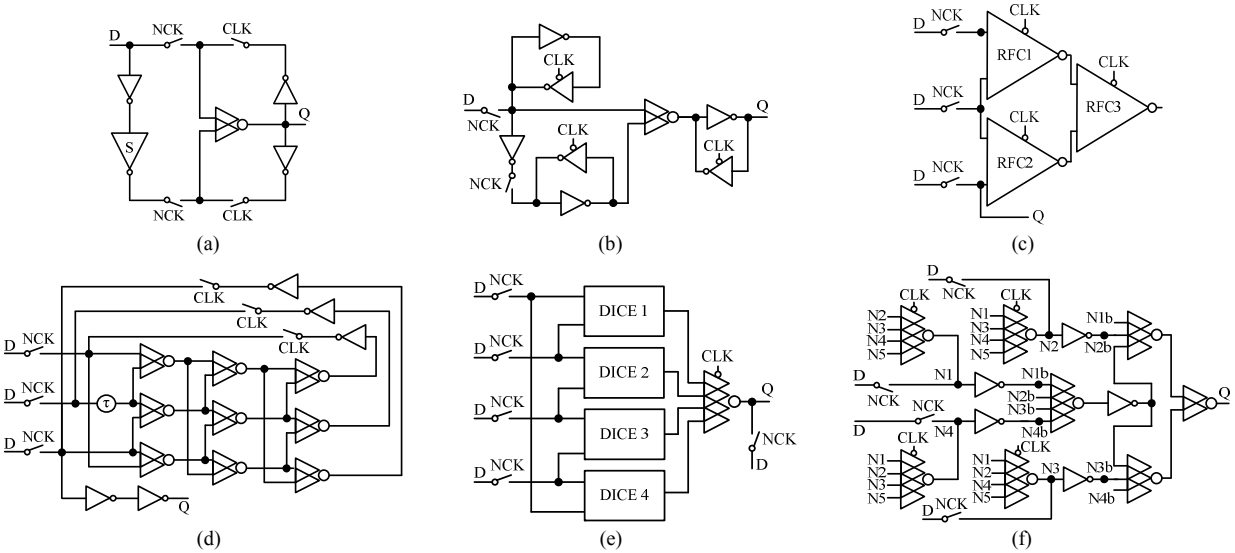


Fig. 2. Schematics of previous hardened latches. (a) DET-SEHPL [19]. (b) LSEH [20]. (c) DNURL [21]. (d) THLTCH [22]. (e) TNUDICE [6]. (f) TNUHL [5].

Fig.2-(a) shows the DET-SEHPL latch [19]. The latch is hardened targeting SNUs/SETs. It uses two inverters to make the output of a CE feed the inputs of the CE to tolerate SNUs. It uses an ST to filter SETs. However, it is obvious that the latch cannot tolerate an SNU at Q. Fig.2-(b) shows the LSEH latch [20]. The latch is hardened targeting SNUs/SETs. It uses two feedback loops feeding a CE to tolerate SNUs. Due to a delay-differential from D to inputs of the CE, the CE can filter SETs. To avoid the sensitivity to an HIS, a keeper is connected to the output of the CE. However, it is obvious that the latch cannot tolerate MNUs.

Fig.2-(c) shows the DNURL latch [21]. The latch is hardened targeting DNUs. It uses three interlocked SNU-self-recoverable RFCs [18] to achieve complete DNU-self-recoverability. However, the latch cannot filter SETs and cannot tolerate TNUs (e.g. three common-nodes among RFCs can be flipped by a TNU causing invalid value-retention). Fig.2-(d) shows the THLTCH latch [22]. The latch is hardened targeting DNUs/SETs. It mainly employs nine interlocked CEs to tolerate SNUs/DNUs; it uses a delay element marked with τ to have a delay-differential from D to inputs of some CEs to filter SETs. However, the latch cannot tolerate TNUs especially for the CEs in series-connection.

Fig.2-(e) shows the TNUDICE latch [6]. The latch is hardened targeting TNUs. It uses four interlocked DICEs feeding a 4-input CE to tolerate TNUs. However, it cannot filter SETs and is sensitive to the HIS (e.g., a DICE suffering from a TNU can make inputs of the CE different although the output of the CE can temporally keep its correct value only for a period of time). Fig.2-(f) shows the TNUHL latch [5]. The latch is hardened targeting TNUs. Similarly to the TNUDICE latch, the latch is still sensitive to the HIS and cannot filter SETs. Moreover, it uses many redundant transistors for hardening, leading to large overhead.

III. Proposed HITTSFL Latch Design

A. Circuit Schematic and Behavior

Fig. 3 shows the schematic of the proposed HITTSFL latch. The latch is constructed from six TGs to initialize values, three parallel CG-based DICEs (DICE1, DICE2, and DICE3) to store values, three inverters (Inv1, Inv2, and Inv3) to make DICEs converge at a common node (Qb), an output-level ST to output the stored values. N1 to N6, N1b to N6b, and Qb are the internal nodes. D and Q are the input and output ports, and CLK and NCK are the system clock and negative system clock signals, respectively.

When CLK is high and NCK is low, the latch works in transparent mode. In this mode, the transistors in TGs are ON, making N1 to N6 have the same value from D. Then, the value of Qb can be determined by N1, N3, and/or N5 through Inv1, Inv2, and/or Inv3. Thus, the value of Q can be determined by Qb through the ST. To reduce power, CG technologies are used in DICEs to avoid the formation of feedback loops so as to reduce current competition in this mode. Thus, N1b to N6b have no values and cannot feed N1 to N6. To summarize, the proposed HITTSFL latch can be properly initialized, and Q can output its value received from D.

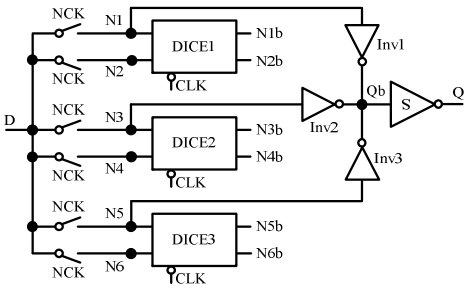


Fig. 3. Proposed HITTSFL latch design.

The SET-filtering principle in transparent mode of the latch is introduced in the following. If an SET arrives at D from upstream combinational gates, the SET will pass through TGs arriving at N1 to N6. Then, the SET will be reversed by Inv1, Inv2, and Inv3, converging at Qb. Therefore, the SET at Qb can be filtered by the ST. A positive SET (low-high-low) at Qb is illustrated as an example for the SET-filtering principle. Since the previous correct value of Qb is low, i.e., the value of N1 in Fig. 1-(e) is low, transistors MP1 and MP2 are ON. Thus, the value of Out is high and MN3 is ON. As a result, when N1 changes from low to high (pulse rise stage) due to the SET, the value of Out will not change until the drain of MN1 is discharged from high to low. This needs a period of time especially when the aspect ratios of MN1 and MN3 are large. Within that period of time, D may change from high to low (pulse fall stage) due to the SET. Therefore, the value of Out will not change. In other words, this positive SET cannot pass through the ST. For a negative SET, we can get the similar scenario. To summarize, the latch can filter SETs.

When CLK is low and NCK is high, the latch works in hold mode. In this mode, the transistors in TGs are OFF. The CLK/NCK-controlled transistors in DICEs are ON, making the values of N1b to N6b feed N1 to N6 and the values of N1 to N6 feed N1b to N6b. Thus, many feedback loops are formed to store values in DICEs. Then, the stored values in DICEs feed Qb through Inv1, Inv2, and/or Inv3, and the value of Qb feed Q through the ST. Hence, the stored values in the latch can output to Q. To summarize, the latch can properly store values, and can output the stored values through Q.

The TNU-toleration principle in hold mode of the latch is introduced in the following. Since any triple-node can be affected by a TNU, there are totally six indicative cases, i.e., **Case T1**: Two nodes in a DICE along with Qb or Q are affected by a TNU; **Case T2**: Three nodes in a DICE are affected by a TNU; **Case T3**: Two nodes in a DICE and one node in another DICE are affected by a TNU; **Case T4**: One node in every DICE is simultaneously affected by a TNU; **Case T5**: One node in a DICE along with Qb and Q are simultaneously affected by a TNU; and **Case T6**: Single nodes in two DICEs along with Qb or Q are affected by a TNU.

For Case T1, we only need to consider DICE1 for illustration. Obviously, the key triple-nodes are only <N1,N1b,Qb>, <N1,N1b,Q>, <N1,N2,Qb>, and <N1,N2,Q>. Note that <N1,N1b> and <N1,N2> cannot self-recover from DNUs if N1 is low [27]. Thus, the values kept in DICE1 will be totally wrong and a wrong value will feed Qb through Inv1.

However, the values kept in DICE2 and DICE3 are correct and the correct values will feed Qb through Inv2 and Inv3. Therefore, the correct value of Qb cannot be determined. Obviously, at the point when Qb is also affected by the TNU, there will be four values converging at Qb, i.e., the first is the wrong value outputting through Inv1, the second is the wrong value coming from the direct particle-striking of the TNU, the third and the fourth are the correct values outputting through Inv2 and Inv3. Fortunately, the second wrong value will not be kept for an extended period of time. This means that, as time passes, the value of Qb will still be jointly determined through Inv1, Inv2, and Inv3, and eventually Qb will still be close to the correct value due to current competition. Therefore, the value of Qb will be reversed and strengthened to be a correct value through the ST, i.e., the output of the latch can be still correct. Obviously, if Q is affected due to a TNU, it can be refreshed to its correct value through Qb. On the other hand, <N1,N1b> can self-recover from a DNU if N1 is high [27]. At this time, in the case where <N1,N1b,Qb> or <N1,N1b,Q> is affected by a TNU, the values kept in DICE1 will still be correct. Thus, the error at Qb or Q will be removed by DICEs through inverters, i.e., the values of all nodes in the latch will still be correct. It can be seen that the latch can tolerate all key TNUs of Case T1.

For Case T2, we still only need to consider DICE1 for illustration. This case is similar to Case T1, but Qb/Q is not directly affected and all nodes in DICE1 can be flipped. Obviously, the key triple-node is only <N1,N1b,N2>. When suffering from a TNU, the wrong values kept in DICE1 will feed Qb through Inv1. However, the correct values kept in DICE2 and DICE3 will feed Qb through Inv2 and Inv3, respectively. Therefore, the value of Qb cannot be determined. Fortunately and eventually, the value of Qb will still be close to the correct value due to current competition and will be reversed and strengthened to be a correct value through the ST, i.e., the output of the latch can be still correct. It can be seen that the latch can tolerate TNUs for Case T2. For Case T3, the indicative key triple-nodes are <N1,N1b,N3> and <N1,N2,N3>. In this case, the single-node-affected DICE can firstly self-recover. Thus, the TNU can downgrade to a DNU, making this case be similar to Case T1. Therefore, the latch can still tolerate TNUs for Case T3.

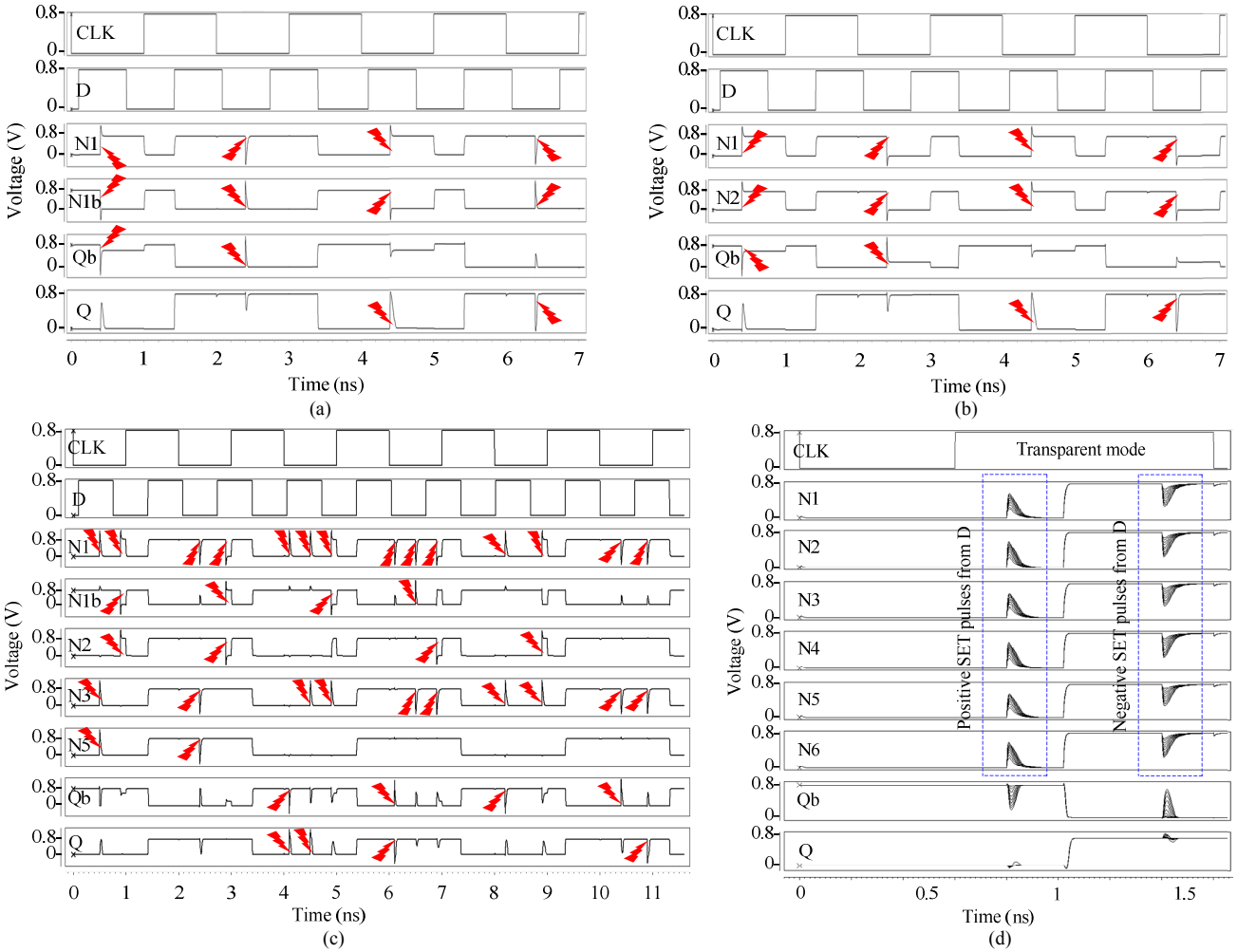


Fig. 4. Simulation results of the proposed HITTSFL latch. (a) Key TNU injections for <N1,N1b,Qb> and <N1,N1b,Q> of Case T1. (b) Key TNU injections for <N1,N2,Qb> and <N1,N2,Q> of Case T1. (c) Other key TNU injections. (d) SET injections.

TABLE I
RELIABILITY COMPARISON RESULTS AMONG THE SNU, DNU, TNU, AND/OR SET UNHARDENED/HARDENED LATCHES

Latch	SNU Tolerant	DNU Tolerant	TNU Tolerant	SET Filterable	HIS Insensitive
Unhardened	NO	NO	NO	NO	YES
TMR	YES	NO	NO	NO	YES
DET-SEHPL [19]	NO	NO	NO	YES	YES
LSEH [20]	YES	NO	NO	YES	YES
DNURL [21]	YES	YES	NO	NO	YES
THLTCH [22]	YES	YES	NO	YES	YES
TNUDICE [6]	YES	YES	YES	NO	NO
TNUHL [5]	YES	YES	YES	NO	NO
HITTSFL (Proposed)	YES	YES	YES	YES	YES

For Case T4, the indicative key triple-node is <N1,N3,N5>. For Case T5, the indicative key triple-node is <N1,Qb,Q>. For Case T6, the indicative key triple-nodes are <N1,N3,Qb> and <N1,N3,Q>. In these cases, since only single nodes are affected in DICEs, DICEs can firstly self-recover [27], i.e., the values kept in DICEs will still be correct. Thus, the errors at Qb and/or Q will be removed by DICEs through inverters and all nodes in the latch will still have correct values, i.e., the latch can tolerate all key TNUs of Cases T4, T5, and T6. To summarize, the above discussions validate that the latch can provide complete TNU tolerability.

B. Simulation Results

The HITTSFL latch was implemented in the 22 nm CMOS technology. Extensive simulations using Synopsys HSPICE were performed. The supply voltage was set to 0.8V, the working temperature was set to room temperature, the PMOS transistors had the ratio W/L = 90/22nm, and the NMOS transistors had the ratio W/L = 45/22nm. In striking-particle simulations, a double-exponential current source model was used [27], and the time constants of the rise and fall periods of the injected pulses were set to 0.1 ps and 3 ps, respectively.

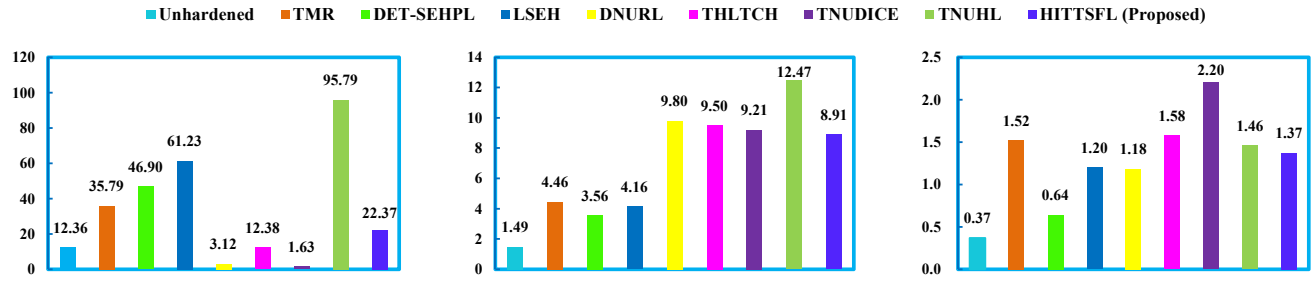
Fig. 4 shows simulation results of the proposed HITTSFL latch. The lighting marks in Fig. 4 denote the injected TNUs. In Fig. 4-(a), when Q = 0, a TNU was injected to triple-nodes <N1,N1b,Qb> and <N1,N1b,Q>, respectively. It can be seen that, no matter Qb was directly affected or not, the value of Qb cannot be flipped, i.e., it was still or close to its correct value. Thus, Q was finally still correct. Moreover, when Q = 1, a TNU was injected to the same triple-nodes. It can be seen that the latch can self-recover from these TNUs. Similarly, it can be seen from Fig. 4-(b) and (c) that the latch can tolerate the injected key TNUs. To summarize, the proposed HITTSFL latch is TNU-tolerant.

In Fig. 4-(d), in transparent mode, positive and negative SETs were respectively injected through the latch-input, and the SETs passed through TGs arriving at N1 to N6. Then, the SETs were reversed through inverters and converged at Qb. It can be seen from Fig. 4-(d) that, the pulses at Qb were filtered by the ST, having almost no impact on Q. To summarize, the proposed HITTSFL latch is SET-filterable. Clearly, simulation results have demonstrated the TNU-tolerability and SET-filterability of the proposed HITTSFL latch.

IV. COMPARISON AND EVALUATION RESULTS

To make a fair comparison, the reviewed latches in Section II as well as the unhardened latch and the TMR latch were also implemented using the same conditions mentioned in the above section. Table I shows the reliability comparison results. It can be seen that only the proposed latch can get five YES, i.e., the proposed HITTSFL latch is the most reliable.

Fig. 5 shows the qualitative overhead comparison results for latches in terms of D to Q delay (i.e., the average of rise and fall delays from D to Q), average power dissipation (dynamic and static) and silicon area (measured with the same method as in [7]). ***Delay Comparison*** It can be seen from Fig. 5-(a) that the DNURL and TNUDICE latches have a smaller delay since any of them uses a high-speed path from D to Q to reduce delay (they cannot filter SETs). The TNUHL latch has the largest delay since it has many transistors from D to Q (it cannot filter SETs either). Generally, a large delay has to be introduced for an SET-filterable latch. Therefore, the delay of any SET-filterable latch is not small. ***Area Comparison*** It can be seen from Fig. 5-(b) that the unhardened latch has the smallest area, since soft-error-hardened latches have to use extra transistors. The TNUHL latch has the largest area as it uses many transistors. The left-side 2nd to 4th latches have a smaller area since they are only SNU and/or SET hardened. Generally, a large area has to be used for a DNU/TNU-tolerant latch. However, the proposed HITTSFL latch has the smallest area compared with the DNU/TNU-tolerant latches. ***Power Comparison*** It can be seen from Fig. 5-(c) that the unhardened latch consumes the smallest power mainly due to its smallest amount of transistors. Similarly, the DET-SEHPL latch also consumes smaller power. The TNUDICE latch consumes the



(a) Delay (b) Area (c) Power

Fig. 5 Qualitative overhead comparison results among the SNU, DNU, TNU, and/or SET unhardened/hardened latches.

largest power although its area is not the largest since it constructs too many feedback loops even in transparent mode leading to much current competition. Generally, the power can be reduced if a latch has a smaller area and/or uses clock-gating technologies to reduce current competition. Thus, the proposed latch consumes the smallest power among the TNU-tolerant latches. To summarize, the above discussions demonstrate that the proposed HITTSFL latch is cost-effective especially in terms of area and power compared with the state-of-the-art TNU-tolerant latches.

$$DRP = \frac{Compared_{\text{delay}} - Proposed_{\text{delay}}}{Compared_{\text{delay}}} \times 100\% \qquad (1)$$

Based on Fig. 5, *delay reduction percentages* (*DRPs*) of the proposed HITTSFL latch compared with the other hardened latches are calculated with Eq. (1) and the other overhead reduction percentages can be similarly calculated. For delay, compared with the TNUDICE latch, the proposed latch has to use an extra 1272.39% delay to ensure SET-filterability. However, compared with the TNUHL latch, the proposed latch can reduce the delay by 76.65% and these compared latches are not SET-filterable. For area, compared with these TNU-tolerant latches, the proposed latch can reduce the area by 3.26% and 28.55%, respectively. For power, compared with these TNU-tolerant latches, the proposed latch can reduce the power by 37.73% and 6.16%, respectively. To summarize, the above discussions demonstrate that the proposed HITTSFL latch is cost-effective compared with the TNU-tolerant latches especially in terms of area and power.

V. Conclusions

With the CMOS technology scaling down, due to the aggressive shrinking of transistor sizes, radiation-induced SETs and MNUs/TNUs are becoming more and more an issue in storage cells used for safety-critical applications. This paper has proposed a novel first-ever TNU-tolerant HIS-insensitive and SET-filterable latch to ensure both high reliability and low overhead. The latch uses three inverters to converge the values kept in three DICEs on a common node feeding an output-level Schmitt-trigger to achieve MNU-tolerability SET-filterability and HIS-insensitivity. Using clock-gating technologies and fewer transistors, the latch is cost-effective. Simulation results have demonstrated the robustness and cost-effectiveness of the proposed latch compared with the TNU-tolerant latches.

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