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***Abstract*—In this paper, a highly reliable SRAM cell, namely SESRS cell, is proposed. Since the cell has a special feedback mechanism among its internal nodes and has more access transistors compared to a standard SRAM cell, the SESRS cell provides the following advantages: (1) it can self-recover from single node upsets (SNUs) and double-node upsets (DNUs); (2) it can reduce power consumption by 49.78% and silicon area by 7.92%, compared with the only existing SRAM cell which can self-recover from all possible DNUs. Simulation results validate the robustness of the proposed SESRS cell. Moreover, compared with the state-of-the-art hardened SRAM cells, the proposed SESRS cell can reduce read access time by 61.93% on average.**

I. Introduction

Aggressive technology scaling employed for manufacturing modern advanced SRAM memories allows high integration density and improved performance. However, an adverse consequence is that the amount of critical charge stored on a node of an SRAM cell decreases due to the ever-decreasing supply voltages and node capacitances. As a result, advanced SRAM cells are becoming more and more susceptive to soft errors induced by the striking of particles, such as protons, neutrons, heavy ions, electrons, muons, and alpha particles [1-2]. Soft errors can invalidly change the values stored in SRAM memories, or even crash SRAM circuits in advanced technologies. Therefore, it is crucial to design hardened structures to achieve high SRAM-reliability with respect to soft errors.

When a particle strikes an OFF-state transistor in a SRAM cell, a dense track of electron-hole pairs can be generated. Therefore, a transient pulse, i.e., *single event transient* (*SET*), may be generated at the node that collects the charge, and it can be detected at the output of the affected logic gate. If the SET pulse propagates through the downstream combinational logic gates arriving at a storage element, the pulse may be captured causing an invalid value-retention in the storage element [3]. On the other hand, the particle may directly strike an OFF-state transistor in a storage element, causing a *single-node upset* (*SNU*). Moreover, integration density of SRAMs is constantly increasing and node spacing is becoming much smaller. Hence, one striking-particle may simultaneously affect two OFF-state transistors in a storage element due to multiple node charge collection mechanisms [4], causing a *double-node upset* (*DNU*). Indeed, SNUs and DNUs can cause invalid value-retention in a SRAM cell. Consequently, to improve the robustness of SRAM cells to protect them against potential data corruptions, execution errors, or even crashes, circuit designers need to mitigate soft errors to improve the reliability of SRAM cells for safety-critical applications. The recent adoption of FinFET technologies can reduce the soft error rate at transistor or cell level [5]. However, this feature of FinFET-based circuits is insufficient to exempt designers to provide valuable and scalable solutions for soft error tolerance, especially for safety-critical applications in harsh environments.

To mitigate SNUs or even DNUs, many designs of SRAM cells [4, 6-15] have been proposed by using the *Radiation Hardening By Design* (*RHBD*) approach. RHBD, which is also used for designing latches [16-17] and flip-flops [18-20], can effectively mitigate the impact of radiation particles on SRAM cells. The traditional SRAM cell is called 6T since it consists of 6 transistors including 2 PMOS and 2 NMOS transistors for value-retention and 2 NMOS transistors for access operations. Since the 6T cell cannot tolerate SNUs, many hardened SRAM cells have been proposed for reliability improvement. Typical SNU hardened cells include ST10T [4], NASA13T [6], RHD12T [7], NS10T [8] and RSP14T [9]. Typical DNU hardened cells include RH12T [10] and DNUSRM [11]. However, these cells still suffer from some serious issues as follows.

(1) Some SRAM cells cannot self-recover from any SNU, such as ST10T [4] and NASA13T [6]. Some SRAM cells can self-recover from SNUs only for a part of internal nodes, such as RHD12T [7], NS10T [8] and RSP14T [9]. Meanwhile, some SRAM cells cannot self-recover from any DNU, such as ST10T [4] and NASA13T [6], and some SRAM cells can self-recover from DNUs only for a part of node pairs, such as RHD12T [7], NS10T [8], RSP14T [9] and RH12T [10].

(2) Some existing hardened SRAM cells suffer from large overhead especially in terms of read access time, such as NASA13T [6] and RH12T [10]. Moreover, some of the cells still suffer from a high write access time, such as ST10T [4] and NASA13T [6], and/or from a high power dissipation, such as NASA13T [6] and DNUSRM [11].

(3) Some existing hardened SRAM cells use additional techniques to ensure SRAM reliability, such as sizing up some transistors [6], increasing spacing between nodes [9], identifying sensitive and insensitive nodes [10], etc. These

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solutions increase the area overhead and design complexity.

Our previously proposed SRAM cell in [21] still suffers from the problem that it cannot provide complete self-recoverability from SNUs although it has small overhead. Based on the RHBD approach, this paper presents a highly reliable SRAM cell with improved self-recoverability from soft errors. Owing to a novel constructed error-interceptive feedback loop, the storage module of the proposed cell can effectively store values and the proposed cell can self-recover from any possible SNU and DNU, irrespective of the energy of striking-particles. Moreover, using six parallel access transistors, the cell suffers from a moderate overhead in terms of read access time and write access time, compared with the state-of-the-art SNU/DNU hardened SRAM cells. Simulation results demonstrate the high reliability and optimized overhead of the proposed SRAM cell.

The rest of this paper is organized as follows. Section II reviews existing hardened SRAM cells. Section III describes the schematic and working principles of the proposed SRAM cell. Section IV presents the comparison and evaluation results. Section V concludes the paper.

II. Typical Existing SRAM Cells

Fig. 1 shows the schematics of typing existing SRAM cells, including the standard 6T cell, the hardened ST10T [4], NASA13T [6], RHD12T [7], NS10T [8], RSP14T [9], RH12T [10] and DNUSRM [11] cells. Fig. 1-(a) shows the schematic of the 6T cell that consists of six transistors (i.e., two PMOS transistors and two NMOS transistors to store values and two NMOS transistors for access operations). Owing to a simple

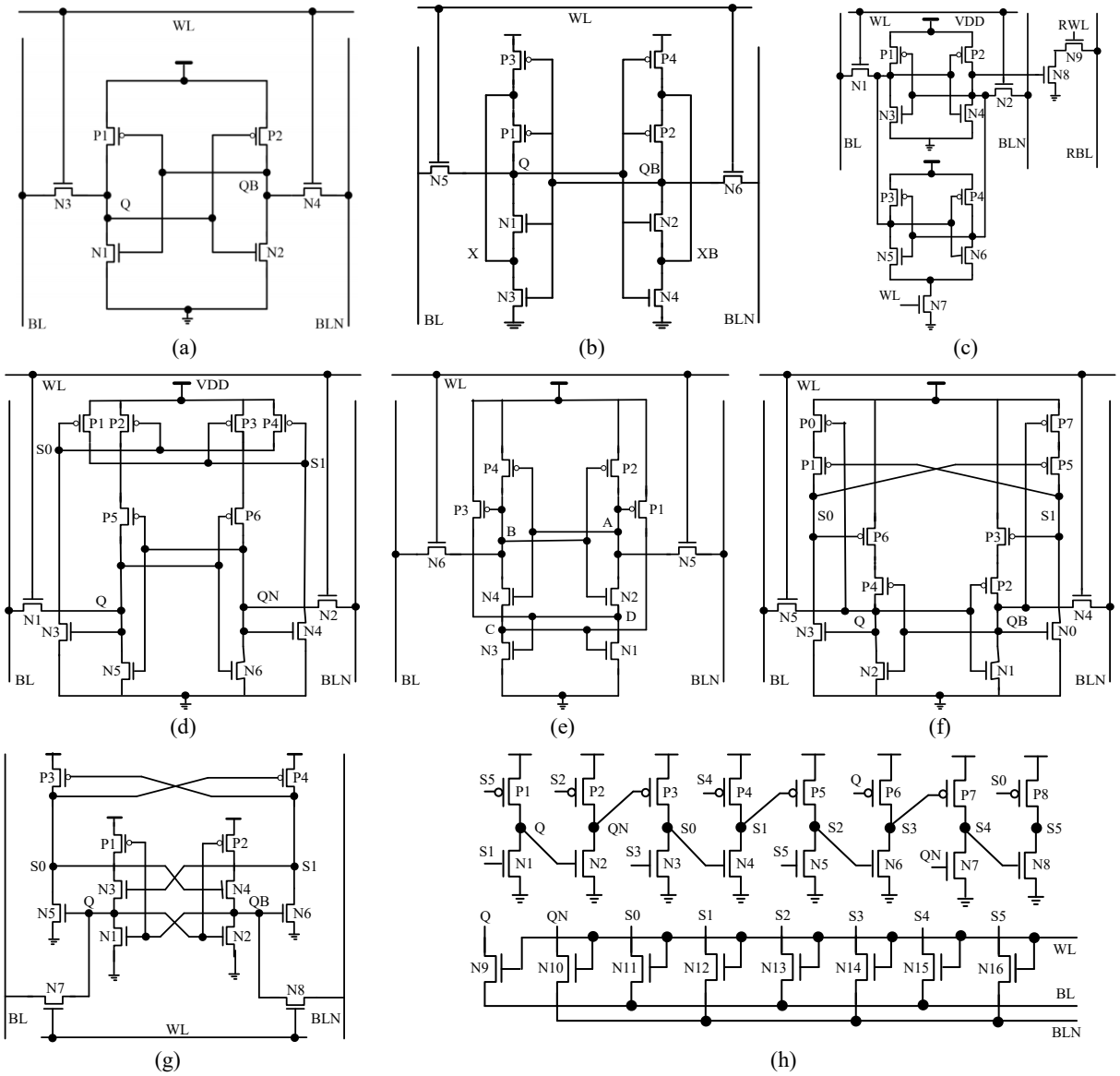

Fig. 1. Schematic of standard and hardened existing SRAM cells. (a) 6T. (b) ST10T [4]. (c) NASA13T [6]. (d) RHD12T [7]. (e) NS10T [8]. (f) RSP14T [9]. (g) RH12T [10]. (h) DNUSRM [11].

construction and small overhead, the 6T cell is widely used. However, this 6T cell cannot tolerate SNUs. Therefore, many hardened SRAM cells have been proposed for reliability improvement.

Fig. 1-(b) shows the schematic of the ST10T cell [4]. It can be seen that Q and QB are internal nodes and they are connected to bit lines BL and BLN through access transistors N5 to N6, respectively. For other transistors (i.e., P1 to P4 and N1 to N4), they are used to store values. Compared with 6T, four transistors (P3, P4, N3 and N4) are redundant stacked transistors to improve reliability of the cell. However, the ST10T cell cannot tolerate SNUs caused by high energy particles since the cell has only one simple feedback loop to store values.

Fig. 1-(c) shows the schematic of the NASA13T cell [6]. It is divided into three parts. The left-top part is used as a primary storage module with a write block. The left-bottom part acts as a secondary storage module. The right part is a special read block for reading values. The read and write blocks ensure its read-ability and write-ability. Compared with 6T, NASA13T provides a high level of protection against SNUs to improve soft-error tolerance, but it still cannot tolerate SNUs caused by high energy particles.

Fig. 1-(d) shows the schematic of the RHD12T cell [7]. The RHD12T cell consists of 12 transistors, i.e., PMOS transistors P1 to P6 and NMOS transistors N1 to N6. Transistors P1 to P6 and N3 to N6 are used for value-retention. Transistors N1 to N2 are access transistors that are controlled by word line WL. Due to the special construction of feedback loops, a large part of single nodes of the RHD12T cell is SNU-hardened. However, only one pair of nodes (i.e., <S0, S1>) of the cell can recover from a DNU.

Fig. 1-(e) shows the schematic of the NS10T cell [8]. The NS10T cell consists of 10 transistors, i.e., PMOS transistors P1 to P4 and NMOS transistors N1 to N6. Access transistors N5 and N6 connect the bit lines (BL and BLN) and the storage nodes (A and B). Since nodes C and D are driven by P1 and P3, respectively, one of C and D goes to supply voltage definitely to retain values. Compared with 6T, only a part of single nodes of the NS10T cell can self-recover from SNUs and only one pair of nodes (i.e., <C, D>) of the NS10T cell can self-recover from a DNU.

Fig. 1-(f) shows the schematic of the RSP14T cell [9]. It can be seen that the RSP14T cell has 4 internal nodes Q, QB, S0 and S1. Nodes S0 and S1 are redundant nodes to improve reliability. Transistors N4 and N5 are access transistors that are controlled by word line WL. Similarly to other cells, some single nodes of the RSP14T still cannot self-recover from SNUs and only one pair of nodes (i.e., <S0, S1>) of the RSP14T cell can self-recover from a DNU.

Fig. 1-(g) shows the schematic of the RH12T cell [10]. The RH12T cell consists of 12 transistors, i.e., PMOS transistors P1 to P4 and NMOS transistors N1 to N8. Transistors P1 to P4 and N1 to N6 are used for value-retention. Transistors N7 to N8 are access transistors that are controlled by word line WL. Due to special feedback rules of the RH12T, all internal nodes can self-recover from SNUs. However, only one pair of nodes (i.e., <S0, S1>) can self-recover from a DNU.

Fig. 1-(h) shows the schematic of the DNUSRM cell [11]. The DNUSRM cell consists of 24 transistors, i.e., PMOS transistors P1 to P8 and NMOS transistors N1 to N16. Transistors P1 to P8 and N1 to N8 are used for value-retention. Transistors N9 to N16 are access transistors that are controlled by word line WL. The DNUSRM cell can self-recover from all possible SNUs and DNUs due to the special construction of feedback loops. However, the DNUSRM cell suffers from a large overhead in terms of power dissipation due to large current competition in its feedback loops, and silicon area overhead due to the use of a large number of transistors.

III. Proposed SRAM Cell

A. Schematic and Normal Operations

The schematic of the proposed *soft-error self-recoverable SRAM* (*SESRS*) cell is depicted in Fig. 2. The SESRS cell consists of 21 transistors, i.e., PMOS transistors P1 to P6 and NMOS transistors N1 to N15. Transistors P1 to P6 and N1 to N9 are used for value-retention. Transistors N10 to N15 are access transistors that are controlled by word line WL. I1 to I6 are internal nodes and they are connected to bit lines BL and BLN through access transistors N10 to N15, respectively. When WL = 1, the access transistors are ON, allowing write/read access operations to be executed. When WL = 0, the access transistors are OFF, and the cell retains the stored value. Fig. 3 shows the layout of the SESRS cell.

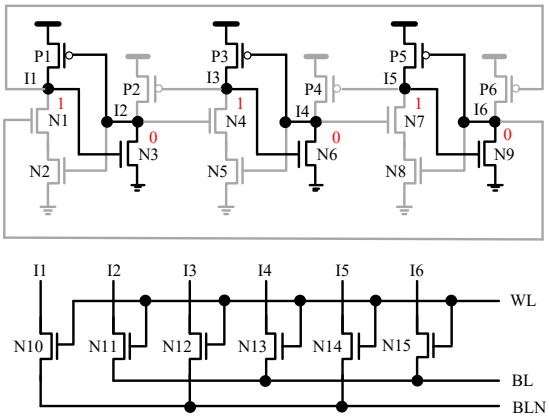

Fig. 2. Schematic of the proposed SESRS cell.

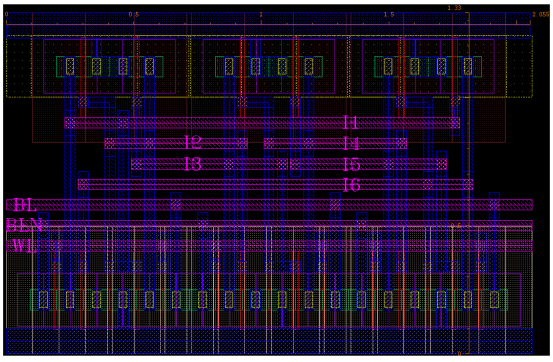

Fig. 3. Layout of the proposed SESRS cell.

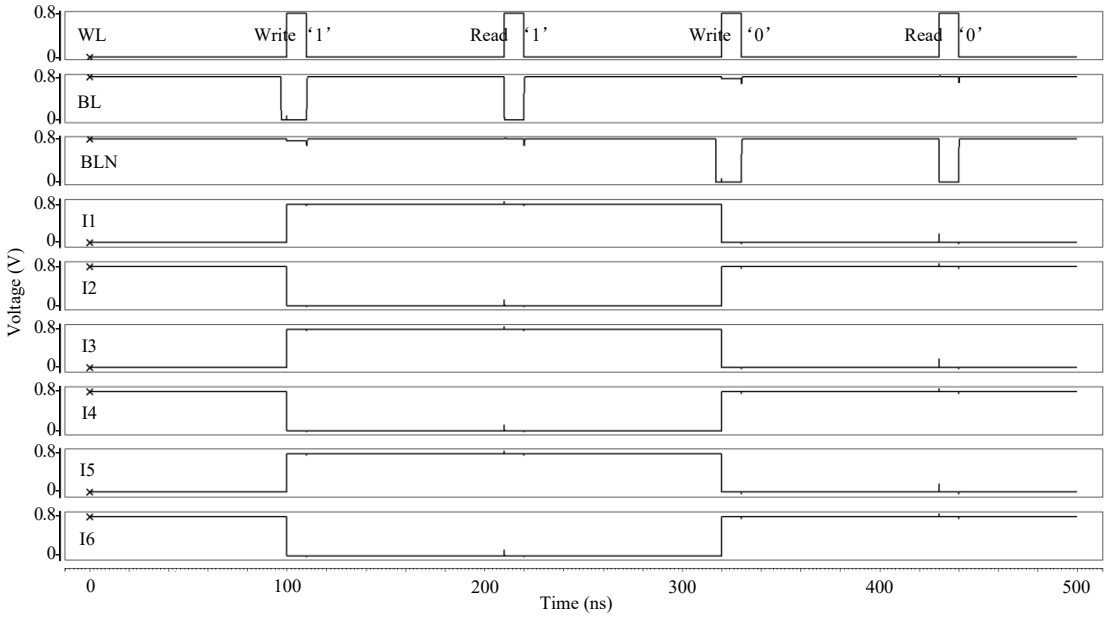

Fig. 4. Simulation results for normal operations of the proposed SESRS cell.

Let us consider the case of storing 1 (i.e., I1 = I3 = I5 = 1 and I2 = I4 = I6 = 0) as an example to introduce the working principles of the proposed SESRS cell. The normal operations are as follows. First, we consider the write access operation, i.e., the case of writing 1 to the cell. In this case, BL = 0 and BLN = 1. When WL = 1, transistors N1, N2, N4, N5, N7, N8, P2, P4 and P6 are OFF while the other transistors are ON, and the stored value is correctly changed to 1.

Next, the case of reading the stored 1 is considered. Before the read operation, bit lines BL and BLN need to be pre-charged to supply voltage. When WL = 1, the voltage of BL decreases since transistors N3, N6 and N9 are ON while the voltage of BLN does not change. Once the differential sense amplifier detects that the voltage difference between BL and BLN is a specified constant value, the value stored in the SESRS cell is successfully read out. For the cases of writing 0 and reading 0, the similar scenarios can be observed.

Fig. 4 shows the simulation results for normal operations of the proposed SESRS cell. It can be seen from Fig. 4 that a series of write 1, read 1, write 0, and read 0 operations were correctly executed and these written values were correctly retained in the proposed SESRS cell.

The fault-tolerance principles of the proposed SESRS cell are described in the subsequent subsections. Here we consider the case of storing 1 (i.e., I1 = I3 = I5 = 1 and I2 = I4 = I6 = 0) shown in Fig. 2 as an example to introduce fault-tolerance principles. First, we discuss the SNU self-recovery principles.

B. SNU Self-Recovery Principle

Let us consider the case where I1 is affected by an SNU as an example to introduce the SNU self-recovery principle. When I1 is changed to 0 due to the SNU, N3 becomes OFF while P6 becomes ON (I6 outputs week 1). Since I5 is not affected (I5 = 1), N9 remains ON (I6 outputs strong 0). So, the strong 0 of I6 can neutralize the weak 1 and hence I6 is still correct (I6 = 0 and N1 remains OFF). On the other hand, I3 is not affected (I3 = 1), P2 remains OFF. As a result, I2 = 0 and P1 remains ON while N2 remains OFF, making I1 = 1. Thus, I1 can self-recover from the SNU. For any other single-nodes, the similar SNU self-recovery principle can be observed.

Fig. 5 shows the simulation results for SNU self-recovery on nodes I1 to I6 of the proposed SESRS cell. As shown in Fig. 5, an SNU was respectively injected to nodes I1 to I6. It can be seen from Fig. 5 that the proposed SESRS cell can self-recover from all SNUs.

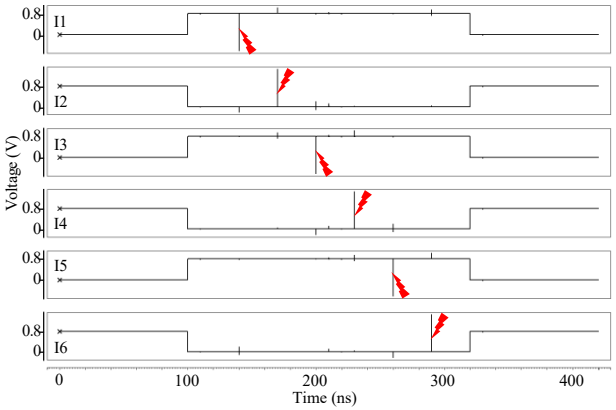

Fig. 5. Simulation results for SNU self-recovery of the proposed SESRS cell.

C. DNU Self-Recovery Principle

Let us consider the case where I1 and I2 are affected by a DNU as an example to introduce the SNU self-recovery principle. When I1 is changed to 0 and I2 is changed to 1 due to the DNU, P1 and N3 become OFF while N2, N4 and P6 become ON (I6 outputs weak 1). Since I5 is not affected (I5 = 1), N9 remains ON (I6 outputs strong 0). So, the strong 0 of I6 can neutralize the weak 1 and hence I6 is still correct (I6 = 0 and N1 is still OFF). At the same time, I3 is not directly affected (I3

= 1), P2 remains OFF. Clearly, the left-side feedback loop is destroyed and the incorrect values of I1 and I2 cannot be kept. However, after a short time, the values of I1 and I2 change back to their correct values since the DNU is only a transient error. In other words, the node pair <I1, I2> can self-recover from a DNU. For the other node pairs, the similar scenarios can be observed.

Fig. 6 shows the simulation results for DNU self-recovery of the proposed SESRS cell. As shown in Fig. 6, a DNU was respectively injected to all possible node pairs <I1, I2>, <I1, I3>, <I1, I4>, <I1, I5>, <I1, I6>, <I2, I3>, <I2, I4>, <I2, I5>, <I2, I6>, <I3, I4>, <I3, I5>, <I3, I6>, <I4, I5>, <I4, I6> and <I5, I6>. It can be seen that the proposed SESRS cell can self-recover from all DNUs.

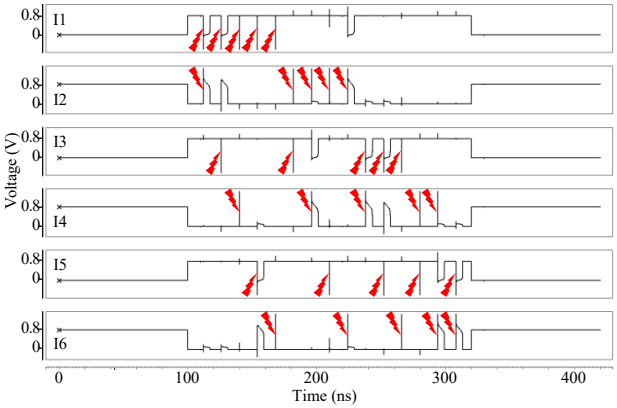

Fig. 6. Simulation results for DNU self-recovery of the proposed SESRS cell.

For the above simulations of the proposed SESRS cell, a flexible double-exponential current-source model was used to perform all fault injections. The time constant of the rise and fall of the current pulse was set to 0.1 and 3.0 ps, respectively [21]. The injected charge was up to 25fC. In all simulations, the Synopsys HSPICE tool was used with an advanced 22nm CMOS library from GlobalFoundries under room temperature and a supply voltage VDD of 0.8V.

IV. Comparison and Evaluation Results

To make a fair comparison with the state-of-the-art typical SRAM cells, such as the 6T, ST10T [4], NASA13T [6], NS10T [7], RHD12T [8], RSP14T [9], RH12T [10] and DNUSRM [11], the same simulation conditions described in the above section were used for SRAM implementations. Table I shows the reliability and overhead comparison results among the unhardened/hardened SRAMs in terms of SNU recoverability, DNU recoverability, write access time (WAT), read access time (RAT), average power dissipation (dynamic and static), and silicon area which is measured with the method in [22].

We first discuss the reliability comparison. It can be seen from Table I that RH12T, DNUSRM and the proposed SESRS cell can provide complete SNU self-recoverability from all possible SNUs. For DNUs, DNUSRM and the proposed SESRS cell can also provide complete DNU self-recoverability from all possible DNUs while the other SRAM cells cannot provide complete DNU self-recoverability. To summarize, the proposed SESRS cell can provide better reliability than the other hardened cells, or equal reliability level when compared to the DNUSRM cell.

Next, we discuss the qualitative overhead comparison. For WATs and RATs, it can be seen from Table I that the 6T cell has the smallest WAT. This is mainly because the 6T cell has less current competition when executing the write operation. Conversely, the NASA13T has the largest WAT due to more current competition when executing the write operation. It can also be seen from Table I that the proposed SESRS cell has a comparable WAT and an even small RAT compared with the other hardened cells (except DNUSRM). This is mainly because the proposed SESRS cell has more access transistors. The NASA13T has the largest RAT due to its special read operation (slow current flow through read transistors). Indeed, the intrinsic charge/discharge of cell-nodes through access transistors can affect WATs and RATs.

For power and area, we generally consider that a cell having fewer transistors has smaller area and less power dissipation. It can be seen from Table I that the 6T cell has the smallest power and area due to the use of only 6 transistors. It can also be seen from Table I that the proposed SESRS cell needs moderate area and power overhead to ensure the self-recoverability from all possible SNUs and all possible DNUs. Note that, the DNUSRM cell consumes the largest power mainly due to the large current competition in its feedback loops and the use of special access

TABLE I
Reliability and Overhead Comparison Results among the Unhardened/Hardened SRAM Cells.

	6T	ST10T	NASA13T	RHD12T	NS10T	RSP14T	RH12T	DNUSRM	SESRS
Ref.	-	[4]	[6]	[7]	[8]	[9]	[10]	[11]	Proposed
SNU Recoverable	×	×	×	×	×	×	√	√	√
DNU Recoverable	×	×	×	×	×	×	×	√	√
Power (nW)	5.24	5.77	18.92	10.38	7.51	7.48	9.74	20.83	10.46
10^{-3}×Area (nm^2)	4.35	7.30	9.70	8.27	7.30	10.65	9.28	17.42	16.04
WAT (ps)	3.65	5.39	16.39	5.06	3.88	4.87	3.85	4.17	5.09
RAT (ps)	25.88	35.97	128.67	25.72	36.76	25.69	37.72	6.63	10.33

transistors. Therefore, the high reliability and optimized speed of the proposed SESRS cell are mainly achieved at the cost of indispensable area and power overhead compared with the other hardened SRAM cells. Compared to the DNUSRM cell, our proposed SESRS cell consumes less area and power.

$$PRC_{WAT} = \frac{WAT_{\mathbf{compared}}(i) - WAT_{\text{proposed}}}{WAT_{\text{compared}}(i)} \times 100\% \quad (1)$$

$$PRC_{WAT}^{\text{average}} = \frac{1}{n}\sum_{i=1}^{n} \frac{WAT_{\text{compared}}(i) - WAT_{\text{proposed}}}{WAT_{\text{compared}}(i)} \times 100\% \quad (2)$$

The *percentages of reduced costs* (*PRCs*) of the proposed SESRS cell compared with the other cells were calculated. The PRC of the WAT was calculated with Eq. (1). Similarly, the PRCs of the RAT, power dissipation, and silicon area can be calculated. The average PRCs were calculated with Eq. (2). Due to page limitation, only the average PRCs are discussed in this paper. Compared with other typical existing hardened cells, the average PRCs of the WAT, RAT, power dissipation, and silicon area are -2.68%, 61.93%, -12.34%, and -85.72%, respectively. In addition, compared with the existing SRAM cell (i.e., DNUSRM) that can self-recover from all possible DNUs, the average PRCs of power dissipation and silicon area are 49.78% and 7.92%. In other words, compared with all typical existing hardened cells, the proposed SESRS cell achieves an approximate 62% RAT reduction at the cost of 3% WAT, 12% power dissipation and 86% silicon area on average to ensure high reliability. However, compared with the only existing SRAM cell that can also self-recover DNUs (i.e., DNUSRM), the proposed SESRS can achieve an approximate 50% power dissipation and 8% silicon area reduction.

Moreover, it is reported in [22] that *process, voltage and temperature* (*PVT*) variations have increasing impacts on storage cells. It is reported in [9] that *static noise margin* (*SNM*) is an important metric to analyze stability of storage cells for normal operations. However, due to page limitation, the PVT and SNM issues will be discussed in our further work.

V. Conclusions

Aggressive technology scaling makes modern advanced SRAM cells increasingly sensitive to soft errors, such as SNUs and DNUs. Based on the RHBD approach, a highly reliable SRAM cell, namely SESRS, has been proposed in this paper. The proposed SESRS cell can self-recover from all possible SNUs and DNUs. The proposed SESRS cell has moderate access time overhead due to the use of four parallel access transistors and small current competition in its feedback loops, compared with the existing SRAM cells. However, compared with the unique SRAM cell that can self-recover from all possible DNUs, the proposed SESRS cell has less power dissipation and silicon area. The proposed SESRS cell can be effectively applied to fields where high reliability and cost-effectiveness are indispensable.

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