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***Abstract*—To meet the requirements of both cost-effectiveness and high reliability for safety-critical terrestrial applications, this paper proposes a novel radiation hardened latch design, namely HLCRT. The HLCRT latch mainly consists of a single-node-upset self-recoverable cell, a 3-input C-element, and an inverter. If any two inputs of the C-element suffer from a double-node-upset (DNU), or if one node inside the cell together with another node outside the cell suffer from a DNU, the latch still has correct values on its output node, i.e., the latch is effectively DNU hardened. Simulation results demonstrate the DNU tolerance of the proposed latch. Moreover, due to the use of fewer transistors, clock gating technologies, and a high-speed path, the proposed latch saves about 444.80% delay, 150.50% power, 72.66% area, and 2029.63% delay-power-area product on average, compared with state-of-the-art DNU hardened latch designs.**

I. Introduction

As the advancement of the manufacturing technology of *integrated circuits* (*ICs*) into the deep nano-scale era, the integration and performance of circuits have significantly improved. Meanwhile, the operational voltage of a circuit is correspondingly lowered so as to reduce power dissipation. However, as the critical charge of circuit nodes decreases with technology scaling, the radiation induced reliability issues of even terrestrial safety-critical applications are becoming more and more serious. That is, even low-energy particles in the terrestrial environment can also cause soft errors [1]. Soft errors are transient errors caused by radioactive particles. Statistical evidences are abundant that soft errors caused by the various types of particles have become a severe problem for advanced ICs [2-3].

Soft errors behave as *single-node-upsets* (*SNUs*), *double-node-upsets* (*DNUs*), *single-event-transients* (*SETs*), *single-event-latchups* (*SELs*), and so on. Among them, SNUs and DNUs are dominating causes for soft errors [4]. When a particle strikes a sensitive node in a storage element such as a latch or a flip-flop, the generated carriers can be collected by the source drain diffusion area, causing a voltage perturbation on the affected node. If the amount of injected charge exceeds that of the critical charge of the affected node, the stored value on the node can be flipped to an invalid value. This phenomenon is called an SNU. Furthermore, in the nano-scale CMOS technology, a single-particle striking may affect two adjacent nodes due to the charge-sharing mechanism, causing voltage perturbations on the two nodes. This phenomenon is called a DNU. Since SNUs and/or DNUs can lead to system-level soft errors in the worst case, many effective schemes to improve circuit reliability against SNUs and DNUs have been proposed using the popular *radiation hardening by design* (*RHBD*) technologies.

The design targets of radiation hardening mainly include memory cells [2, 5], flip-flops [6, 7], and latch designs [8-18]. In recent years, many hardened latch designs have been proposed to mitigate SNUs, including the *High-Performance SNU Tolerant* (*HPST*) [8], *High-Performance Low-cost Robust* (*HLR*) [9], and *FEedback Redundant Soft error Tolerant* (*FERST*) [10] latch designs. These latch designs either employ the RHBD technologies, such as *dual-modular redundancy* (*DMR*), *feedback loops interlocking* (*FLI*), and guard gates or introduce delays in feedback mechanisms to robustly retain values against SNUs. However, most of these latch designs cannot tolerate DNUs, making them inapplicable to the safety-critical terrestrial applications that require high reliability.

To effectively mitigate DNUs, many novel latch designs have been proposed [3, 19-30], including the *DNU self-Recoverable* (*DNURL*) [3], *Circuit and Layout Combination Technique* (*CLCT*) [23], *Double Node Charge Sharing SNU Tolerant* (*DNCSST*) [24], and *Delta Dual-Interlocked-Cell* (*DeltaDICE*) [25] latch designs. These latch designs mainly employ such techniques as increasing transistor feature sizes for weak nodes, *triple-modular redundancy* (*TMR*), and layout solutions such as wider node spacing, well isolation, and guard rings. However, the DNURL, CLCT, DNCSST, and DeltaDICE latch designs have large overhead in terms of transmission delay, power dissipation, silicon area, and *delay-power-area product* (*DPAP*) (calculated through multiplying delay, power, and area), making them unsuitable for safety-critical terrestrial applications that also require cost-effectiveness. Moreover, some advanced latch designs that can tolerate both DNUs and *triple-node-upsets* (*TNUs*) have been proposed recently [31-33]. However, these latch designs are mainly used for space applications that require very high reliability and can tolerate extra redundancies induced large overhead.

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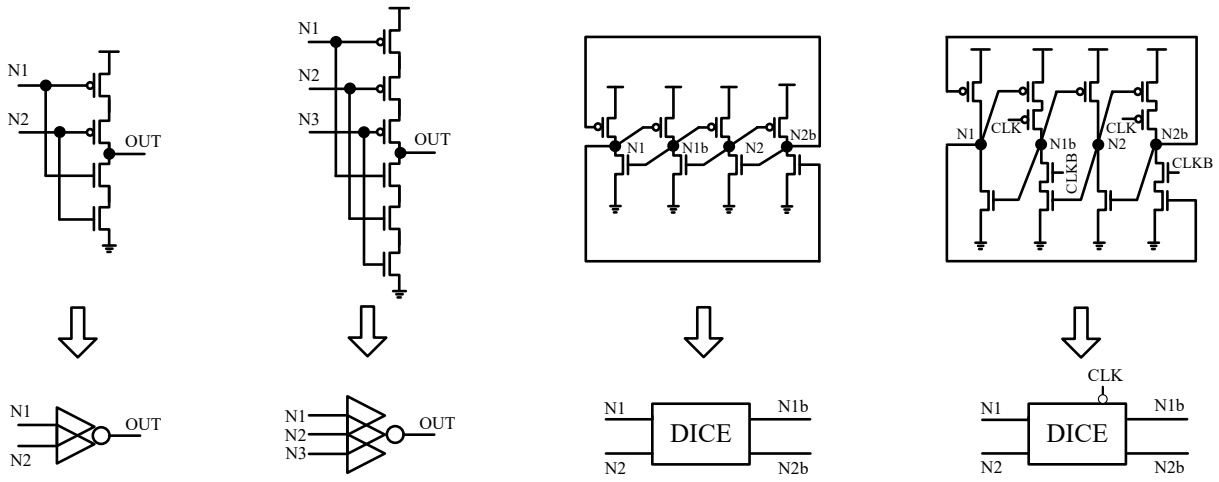

Fig. 1. Schematics and symbols of the widely used components (C-elements and DICE cells) in hardened latch designs. (a) 2-input C-element, (b) 3-input C-element, (c) DICE cell, (d) Clock-gating based DICE cell.

In this paper, a novel radiation Hardened Latch design is proposed for low-Cost and Reliable Terrestrial applications, namely HLCRT. The HLCRT latch is mainly constructed from a *Dual-Interlocked-Cell* (*DICE*) [34], a 3-input *C-element* (*CE*), and an inverter. When one node inside the DICE cell together with another node outside the DICE cell are affected by a DNU, or any two inputs of the CE are affected by a DNU, the latch still has a correct value on its output node. Simulation results demonstrate the DNU tolerance and cost-effectiveness for the proposed HLCRT latch design compared with state-of-the-art DNU hardened latch designs, indicating that the latch can be applied to safety-critical terrestrial applications that require not only high reliability but also cost-effectiveness.

The rest of the paper is organized as follows. Section II introduces the implementation, working principles, and reliability verifications of the proposed latch design. Section III presents comparison and evaluation results. Section IV concludes the paper.

II. Proposed HLCRT Latch Design

Among many hardened latch designs, such as the HPST [8], HLR [9], FERST [10], CLCT [23], DNCSST [24], DeltaDICE [25], and DNURL [3], CEs and DICE cells are widely used as important components. Their circuit schematics and symbols are shown in Fig. 1. A CE behaves as an inverter if its inputs have the same value but goes into *high-impedance state* (*HIS*) if its inputs become different. This means that a CE can temperately retain the previous correct value. A DICE cell can self-recover to the correct value when any of its nodes suffers from an SNU [34]. In the proposed HLCRT latch design, both a CE and a DICE cell are employed.

A. Circuit Schematic and Behavior

The schematic and layout of the proposed HLCRT latch design are presented in Fig.2. The HLCRT latch is constructed from a DICE cell that can self-recover from any possible SNU, a 3-input CE with *clock-gating* (*CG*) that can intercept errors, an inverter with CG, i.e., INV in Fig. 2, and four *transmission gates* (*TGs*), i.e., TG1, TG2, TG3, and TG4 in Fig. 2. In the latch structure, D is the input, Q is the output, and CLK and CLKB are the system clock and negative system clock signals, respectively.

The HLCRT latch has two operation modes, i.e., transparent mode and hold mode. In transparent mode, CLK is high and CLKB is low. As a result, TG1, TG2, and TG3 are ON. In the case of D = 0, since N1 and N2 are directly driven by D through

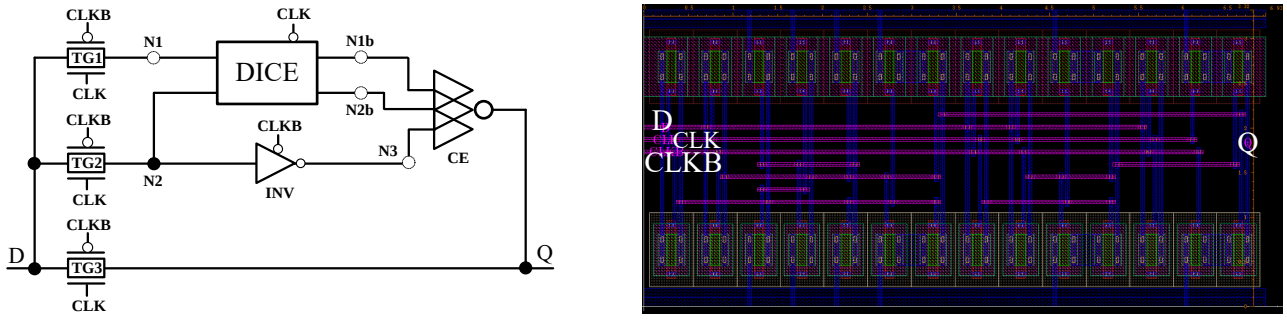

Fig. 2. Proposed HLCRT latch design. (a) Schematic, (b) Layout.

TG1 and TG2, respectively, it is clear that N1 = N2 = 0. This means that the inputs of the DICE cell can be determined. However, the DICE cell will not output values on N1b and N2b, due to the OFF states of the transistors with CG in the DICE cell. This means that the feedback loops are not constructed in the DICE cell in transparent mode, resulting in reduced current competition on nodes to save power dissipation. At the same time, all transistors in INV are ON, and thus N3 = 1. Therefore, not all inputs of the CE can be determined and then the CE enters into the HIS, outputting no value. Furthermore, TG3 is ON, and thus the output node Q is directly driven by D through TG3 (Q = D = 0), instead of being driven by the inputs of the CE since only some of the inputs of the CE are determined. This can avoid current competition on Q to reduce both power dissipation and transmission delay for the latch. It can be seen that all the critical transistors of the latch are correctly pre-charged in transparent mode. In the case of D = 1, a similar scenario can be observed.

When CLK is low and CLKB is high, the latch operates in hold mode. In this case, TG1, TG2, TG3, and the transistors with CG in INV are OFF, and the transistors with CG in the DICE cell are ON. This means that the pre-charged N1 and N2 can drive N1b and N2b, and then all inputs of the CE have values since the DICE cell outputs values on N1b and N2b and N3 still has its previous correct value, making the latch output the stored value. In other words, the latch can effectively hold the stored value.

In the following, the fault-tolerance mechanism of the proposed latch in hold mode is described. Here we still consider the example of holding 0 of the latch (i.e., Q = N1 = N2 = 0). First, the SNU tolerance of the latch is discussed. Since it is well known that the DICE cell is self-recoverable from any possible SNU, the SNU tolerance of the nodes in the DICE cell is omitted (related details can be found in [34]). Note that, when N2 is affected by an SNU, the error cannot propagate to N3 due to the node isolation using INV with CG. Therefore, only N3 and Q need to be discussed for SNU tolerance. In the case where N3 is affected by an SNU, N3 is flipped from 0 to 1. In this case, since the inputs of the CE become different, the CE will still has its previous value on Q (i.e., Q = 0) although N3 cannot self-recover from the SNU. In the case where Q is affected by an SNU, Q is temporally flipped from 0 to 1. In this case, since the inputs of the CE still have the original correct value (i.e., N1b = N2b = N3 = 1), the CE will still output the correct value (i.e., Q = 0, and Q can self-recover from the SNU). Therefore, the proposed HLCRT latch can tolerate any possible SNU. Note that for Q = N1 = N2 = 1, a similar scenario can be observed.

Next, the DNU tolerance of the latch is discussed. It is well known that the DICE cell cannot provide any-possible-DNU self-recoverability. This means that we have to consider the worst case where all nodes in the DICE cell are flipped when a node-pair in the DICE cell suffers from a DNU. It is obvious that the DICE cell has 6 node-pairs, i.e., <N1, N2>, <N1, N1b>, <N1, N2b>, <N2, N1b>, <N2, N2b>, and <N1b, N2b>. In the case where any of these node-pairs suffers from a DNU, N3 is not affected. In other words, all inputs of the CE are not simultaneously affected. Therefore, the CE can still have its previous value on Q although many of these node-pairs cannot self-recover from DNUs. Therefore, the latch is DNU tolerant for all above mentioned node-pairs.

Finally, we consider the case where one node inside the DICE cell together with another node outside the DICE cell are affected by a DNU. It is obvious that, outside the DICE cell, we only need to consider two nodes, i.e., N3 and Q. In the case where N3 together with any single node inside the DICE cell are affected by a DNU, the single node inside the DICE cell can self-recover to the correct state. However, N3 will still retain its flipped value. This means that the inputs of the CE become different. In this case, however, the CE still has its previous value on Q. Furthermore, in the case where Q together with any single node inside the DICE cell are affected by a DNU, the single node inside the DICE cell can self-recover to the correct state. This means that the inputs of the CE will still have their previous values, making the CE still output its previous value on Q. In other words, any above mentioned node-pair can tolerate DNUs. In summary, the latch can tolerate DNUs and SNUs.

B. Verification Results

The HLCRT latch was implemented in the 32nm CMOS technology, the working voltage was set to 0.9V, and pertinent simulations using Synopsys HSPICE were performed. The transistor sizes employed in the latch design are listed in the following. (a) At TG1 and TG2 for driving both the DICE cell and the inverter when the latch operates in transparent mode, including the normal input-split inverters inside the DICE cell and the CG-based inverter, the pMOS transistor had W/L = 128/32nm while the nMOS transistor had W/L = 45/32nm, (b) at the CG-based input-split inverters inside the DICE cell, including the 3-input CE, the pMOS transistors had W/L = 180/32nm while the nMOS transistors had W/L = 100/32nm, and (c) at TG3 for driving Q when the latch operates in transparent mode, the pMOS transistors had W/L =128/32nm while the nMOS transistors had W/L = 65/32nm.

Fig. 3 shows the simulation waveforms for the proposed HLCRT latch. In Fig. 3-(a), the error-free case (without fault injections) capturing input D and feeding output Q at operational supply-voltage 0.9V is shown. It can be seen from the simulation result that, the latch can correctly operate in transparent mode (D = Q) when CLK was high; the latch can correctly operate in hold mode (the previous D was kept on Q) when CLK was low. In other words, the operation of the HLCRT latch in normal modes is similar to that of a conventional unhardened latch.

In the following simulations, a controllable double exponential current source model was employed to simulate fault injections [24]. The worst case injected charge was chosen to be up to 45fC for a single node, which is large enough since we aim to validate the circuit operation under extreme DNU conditions that disturb the nodes of the latch. The time constant of the rise and fall of the current pulse was set to be 0.1 and 3 ps, respectively. Fig. 3-(b) to (d) show the DNU injection

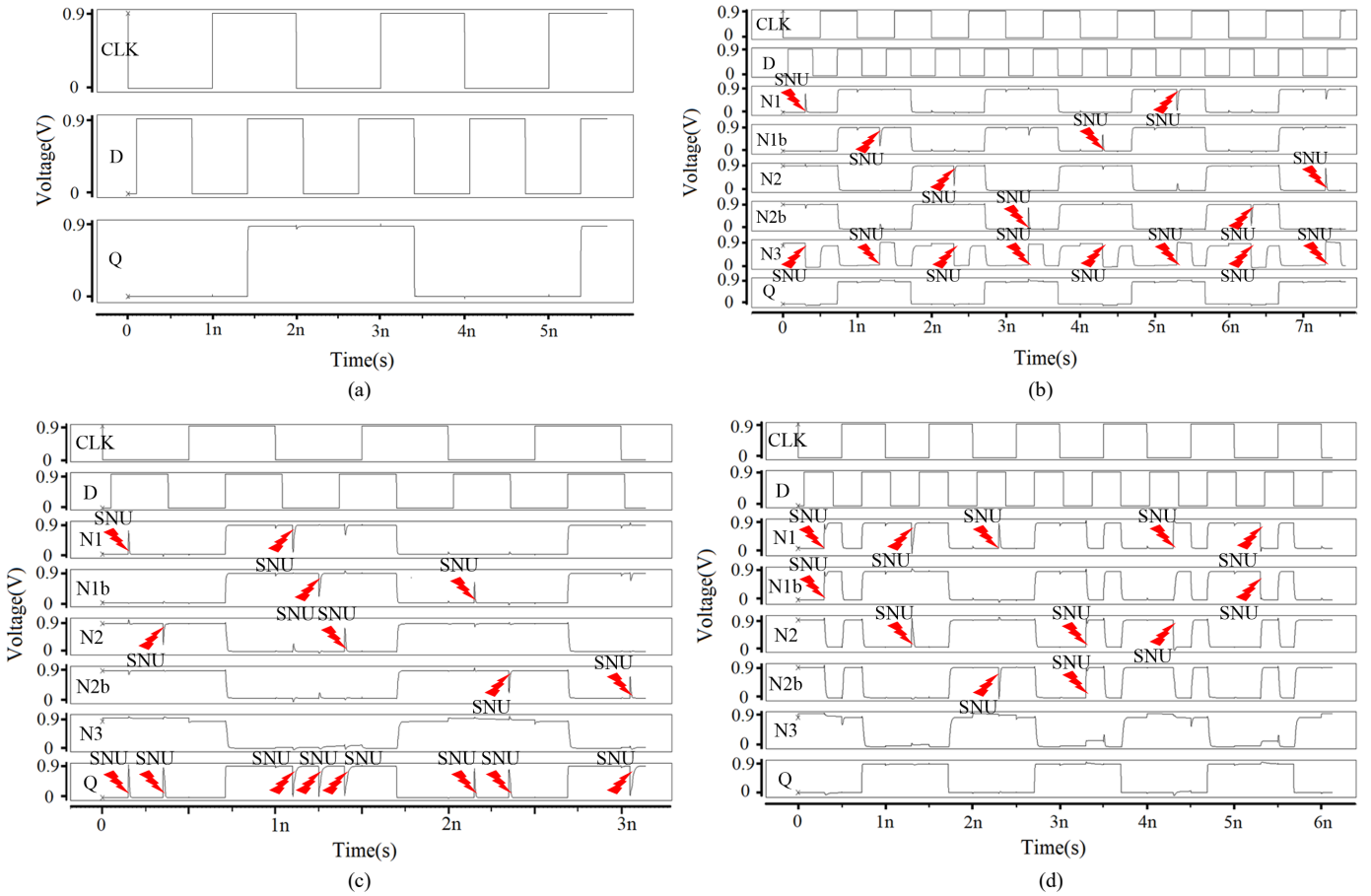

Fig. 3. Simulation waveforms for the proposed HLCRT latch design. (a) Error-free case (without fault injections), (b) DNU case with injections to N3 and an internal node of the DICE cell, (c) DNU case with injections to Q and an internal node of the DICE cell, (d) DNU case with injections to node-pairs in the DICE cell.

simulation results for the HLCRT latch.

Fig. 3–(b) shows the simulation waveform of the proposed HLCRT latch with DNU injections when the latch operates in hold mode. In the DNU node-pairs, one node is N3 and another is an internal node of the DICE cell. At 0.3ns, 1.3ns, 2.3ns, and 3.3ns, a DNU with large enough charge was injected on the node-pairs <N1, N3>, <N1b, N3>, <N2, N3>, and <N2b, N3>, respectively. To ensure that any node was injected with an error no matter its original correct value is high or low, at 4.3ns, 5.3ns, 6.3ns, and 7.3ns, the supplemental injections on the node-pairs <N1b, N3>, <N1, N3>, <N2b, N3>, and <N2, N3> were performed, respectively. It can be seen from Fig. 3–(b) that, only N3 inside these node-pairs cannot restore back from DNUs; however, the error is respectively blocked by the 3-input CE, resulting in nearly no any effect on Q, i.e., the latch still has its previous value on Q.

Fig. 3–(c) shows the simulation waveform of the proposed HLCRT latch with new DNU injections when the latch operates in hold mode. In the DNU node-pairs, one node is Q and another is an internal node of the DICE cell. All of the four single nodes inside the DICE cell were selected for fault injections. As shown in Fig. 3–(c), at 0.15ns, 1.25ns, 1.40ns, and 2.35ns, a DNU with large enough charge was injected on the node-pairs <N1, Q>, <N1b, Q>, <N2, Q>, and <N2b, Q>, respectively. To ensure that any node was injected with an error no matter its original correct value is high or low, at 0.35ns, 1.10ns, 2.15ns, and 3.10ns, the supplemental injections on the node-pairs <N2, Q>, <N1, Q>, <N1b, Q>, and <N2b, Q> were performed, respectively. It can be seen from Fig. 3–(c) that, all of these nodes can restore back from the DNUs, i.e., the latch still has its previous values on all nodes.

Fig. 3–(d) shows the simulation waveform of the proposed HLCRT latch with the last type of DNU injections when the latch operates in hold mode and each DNU node-pair is inside the DICE cell. As previously described, there are 6 node-pairs inside the DICE cell, i.e., <N1, N1b>, <N1, N2>, <N1, N2b>, <N1b, N2>, <N1b, N2b>, and <N2, N2b>. The four key/indicative node-pairs <N1, N1b>, <N1, N2>, <N1, N2b>, and <N2, N2b> were selected for fault injections. At 0.3ns, 1.3ns, 2.3ns, and 3.3ns, a DNU with large enough charge was injected on the node-pairs <N1, N1b>, <N1, N2>, <N1, N2b>, and <N2, N2b>, respectively. To ensure that any node was injected with an error no matter its original correct value is high or low, at 4.3ns and 5.3ns, the supplemental injections on the node-pairs <N1, N2> and <N1, N1b> were performed,

TABLE I
COMPARISON RESULTS FOR THE SNU AND/OR DNU HARDENED LATCH DESIGNS

Latch	Ref.	SNU Tolerant?	DNU Tolerant?	Delay (ps)	Power (μW)	Area (UST)	10^{-3}× DPAP
HPST	[8]	Yes	No	2.14	0.51	106.41	0.12
HLR	[9]	Yes	No	2.12	0.38	88.91	0.07
FERST	[10]	Yes	No	85.65	1.41	103.84	12.54
CLCT	[23]	Yes	Yes	31.98	0.70	111.19	2.49
DNCSST	[24]	Yes	Yes	69.71	1.65	142.97	16.44
DeltaDICE	[25]	Yes	Yes	10.08	0.85	175.28	1.50
DNURL	[3]	Yes	Yes	5.47	1.81	259.28	2.57
HLCRT	Proposed	Yes	Yes	5.38	0.50	99.72	0.27

TABLE II
RELATIVE OVERHEAD OF THE DNU HARDENED LATCH DESIGNS COMPARED WITH THE PROPOSED LATCH DESIGN

Latch	Ref.	ΔDelay (%)	ΔPower (%)	ΔArea (%)	ΔDPAP (%)
CLCT	[23]	494.42	40.00	11.50	822.22
DNCSST	[24]	1195.72	230.00	43.37	5988.89
DeltaDICE	[25]	87.36	70.00	75.77	455.56
DNURL	[3]	1.67	262.00	160.01	851.85
Average	N/A	444.80	150.50	72.66	2029.63

respectively. It can be seen from Fig. 3–(d) that, most of these nodes cannot restore back from the injected DNUs. However, the retained errors can be blocked by the 3-input CE, resulting in nearly no any effect on Q, i.e., the latch still has its previous value on Q. Therefore, the above mentioned simulation results have validated the ability of the proposed HLCRT latch to provide the fault tolerance against DNUs.

III. COMPARISON AND EVALUATION

To make a fair comparison, the typical latch designs HPST [8], HLR [9], FERST [10], CLCT [23], DNCSST [24], DeltaDICE [25], and DNURL [3] were implemented/designed under the same conditions as that of the proposed HLCRT latch. Table I shows the detailed comparison results for these above mentioned SNU and/or DNU hardened latch designs including the proposed HLCRT latch in terms of D to Q transmission delay, the average of power dissipation (dynamic and static), silicon area, and *delay-power-area product* (*DPAP*) calculated through multiplying delay, power, and area. As in [19], the silicon area of these latch designs was also measured in equivalent *unit size transistors* (*USTs*) for a fair comparison. It is obvious that, a smaller DPAP is better as for the same type of latch designs (e.g., the DNU hardened type), since the comprehensive overhead of this type of latch designs is small.

It can be seen from Table I that, compared with the SNU hardened latch designs, i.e., the first three designs (HPST, HLR, and FERST), the transmission delay of the proposed HLCRT latch is not as small as that of the HPST and HLR, the power dissipation and silicon area of the proposed HLCRT latch are not as small as that of the HLR. However, the HPST, HLR, including the FERST latches are not DNU hardened at all. Furthermore, compared with the 4th to 7th DNU tolerant latches, i.e., the CLCT, DNCSST, DeltaDICE, and DNURL, the overhead of the proposed HLCRT latch is the smallest for the transmission delay, power dissipation, silicon area, and DPAP product, which can effectively validate the cost-effectiveness of the proposed HLCRT latch.

To make a further detailed quantitative comparison, the relative overhead in terms of delay (ΔDelay), power (ΔPower), area (ΔArea), and DPAP (ΔDPAP) among the DNU hardened latches compared with the proposed HLCRT latch has been calculated with Eq. (1). Table II shows the relative overhead of the DNU hardened latches compared with the proposed HLCRT latch.

$$\Delta = [(\text{Compared} - \text{Proposed}) / \text{Proposed}] \times 100\% \quad (1)$$

It can be seen from Eq. (1) that, the positive percentages in Table II mean that the overhead of the proposed HLCRT latch is smaller than that of the compared latches. Reversely, the negative percentages mean that the overhead of the proposed HLCRT latch is larger than that of the compared latches.

It can be seen from Table II that, all the percentages are positive, which means that the overhead of the proposed HLCRT latch is small for all aspects of overhead. Furthermore, it can also be seen from Table II that, the proposed HLCRT latch can save about 444.80% transmission delay, 150.50% power dissipation, 72.66% silicon area, and 2029.63% DPAP on average. Therefore, the proposed HLCRT latch is cost-effective compared with the same type of latches. In other words, the compared DNU hardened latches can operate robustly; however, they suffer from large cost penalties. Therefore, the proposed latch HLCRT is not only reliable but also cost-effective, and thus it is suitable for safety-critical terrestrial applications that require both high reliability and

cost-effectiveness.

IV. Conclusions

The aggressive technology scaling significantly improves the performance and integration for ICs; however, it also brings about some more serious challenges to the reliability of ICs and systems, especially soft errors coming from SNUs and DNUs in storage elements. Without radiation hardening, the applications of ICs in terrestrial applications (e.g. communication, healthcare, automobile, etc) will likely suffer from soft errors in advanced technologies. Especially in the safety-critical terrestrial applications, both high reliability and cost-effectiveness requirements are critical. In this paper, a cost-effective and radiation hardened reliable latch has been proposed and designed in the nano-scale CMOS technology. Using the error masking mechanism of the C-element, the proposed latch is effectively DNU hardened. Employing fewer transistors, transistors with clock-gating, and a high-speed path from the input to the output, the latch has low overhead. Simulation results have demonstrated the DNU tolerance and cost-effectiveness of the proposed latch, making the latch widely applicable to safety-critical terrestrial applications that require both high reliability and cost-effectiveness.

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