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Aibin Yan, Zhelong Xu, Jie Cui, Zuobin Ying, Zhengfeng Huang, et al.. Dual-Interlocked-Storage-Cell-Based Double-Node-Upset Self-Recoverable Flip-Flop Design for Safety-Critical Applications. ISCAS 2020 - IEEE International Symposium on Circuits and Systems, Oct 2020, Sevilla (virtual), Spain. pp.1-5, 10.1109/ISCAS45731.2020.9181135 . lirmm-03035619

HAL Id: lirmm-03035619
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Submitted on 2 Dec 2020

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Dual-Interlocked-Storage-Cell-Based Double-Node-Upset Self-Recoverable Flip-Flop Design for Safety-Critical Applications

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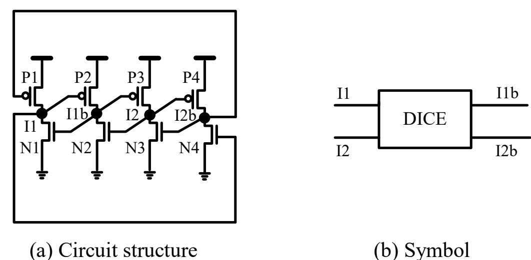
***Abstract*—This paper presents a novel dual-interlocked storage-cell (DICE)-based double-node-upset (DNU) self-recoverable, namely DURI-FF, in the nano-scale CMOS technology. The master latch of the DURI-FF cell consists of three transmission gates (TGs) and three interlocked DICEs with three common nodes. The common nodes are connected to TGs for value initialization. The slave latch of the DURI-FF cell comprises six TGs, six inverters and three interlocked DICEs. The outputs of the inverters respectively feed the internal nodes of the slave latch. The interlocked DICEs make the master latch and the slave latch DNU self-recoverable. Simulation results validate the DNU self-recoverability of the proposed DURI-FF cell. Moreover, compared with the state-of-the-art hardened flip-flop cells, the proposed DURI-FF cell achieves roughly 43% delay reduction at the cost of moderate silicon area and power dissipation.**

I. INTRODUCTION

With CMOS technologies aggressively scaling down, integrated circuits are becoming more and more vulnerable to radiation-induced errors commonly known as *soft errors.* This is because the amount of critical charge stored at a node in a circuit decreases due to the smaller node capacitance as well as lower supply voltages in advanced nano-scale CMOS technologies. As a result, the values of circuit nodes can be easily disturbed by radiation effects. The striking of radiative high-energy particles, such as neutrons, alpha particles, protons, heavy ions, electrons, and muons as well as the irradiation of high-energy X-ray and laser, etc., can easily cause soft errors to modern advanced CMOS circuits [1-2]. Soft errors can cause potential data corruptions, execution errors, and even system crashes. Therefore, there is a strong need for highly-robust circuit design techniques to effectively construct highly reliable circuits and systems.

Single-event transients (*SETs*), *single-node upsets* (*SNUs*), and *double-node upsets* (*DNUs*) are typical soft errors. When a particle with enough linear-energy-transfer hits the diffusion region of an OFF-state transistor, a voltage change in the node connected to the drain-terminal of the affected transistor will occur since the particle allows a faulty / undesired current to temporarily flow through the affected transistor. In a combinational logic circuit, such a particle-striking can cause a transient pulse, i.e., an SET, at the output of the affected logic gate. If there is at least one sensitized-path from the affected gate to a downstream storage element, the SET may propagate to the storage element [3]. If the SET duration is large enough and matches the input-value-sampling window of the storage element, the SET will cause invalid value-retention in the storage element. In the same context, if the particle directly hits an OFF-state transistor in a storage element, it will cause an SNU. Moreover, aggressively scaled CMOS technologies make node-spacing smaller and smaller. As a result, through charge sharing between a primary node and an adjacent secondary node, one striking-particle may simultaneously affect two nodes in a storage element, causing a DNU [4]. SETs, SNUs, and DNUs can lead to invalid value-retention in storage elements causing potential data corruptions, execution errors, and even crashes of circuits and systems. Therefore, reliability design against such soft errors is required especially for safety-critical applications.

SET-filtering designs of storage elements usually introduce performance degradation and extra overhead. Thus, this paper mainly considers hardening against SNUs and DNUs. To mitigate SNUs and DNUs, *radiation hardening by design* (*RHBD*) is a widely employed approach. Using RHBD, many novel storage elements, such as latches [5-8], *static random access memories* (*SRAMs*) [9-12], and *flip-flops* (*FFs*) [13-19, 23] have been proposed. Among them, *dual-interlocked storage-cells* (*DICEs*) are widely used [20]. Fig. 1 shows the circuit structure and the symbol of the DICE. A DICE has two important features: (1) it is self-recoverable from any possible SNU; (2) it is only partially self-recoverable from some DNUs, i.e., only some of its node-pairs can self-recover from DNUs (for other node-pairs, a DNU can result in flips of all its nodes). Note that, in Fig. 1, I1b and I2b have the reversed values of I1 and I2, respectively.



(a) Circuit structure (b) Symbol

Fig. 1. Widely used dual-interlocked storage-cell (DICE).

This paper mainly focuses on the hardening for FFs based on DICEs. It is well-known that the *traditional unhardened FF* (*TUFF*) comprises a master *traditional unhardened latch* (*TUL*)

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and a slave TUL [23]. Since a TUL cannot tolerate SNUs, a TUFF cannot tolerate SNUs. To improve reliability, many hardened FFs protected against SNUs have been proposed. Typical SNU-hardened FFs include the designs in [13-19, 23], and so on. Similarly, to achieve high reliability, many hardened FFs protected against DNUs have been proposed. Typical DNU-hardened FFs include the designs in [16-19], and so on. However, these FFs still suffer from the following problems.

(1) For DNU hardening, they have to use extra layout techniques such as increasing spacing between adjacent nodes. Moreover, most of the DNU-hardened FFs have at least a counterexample that they cannot tolerate a DNU [16-18] especially in their master or slave latches.

(2) They are not SNU/DNU-self-recoverable, except the DICE-FF in [17] that is SNU-self-recoverable. To the best of our knowledge, there is no DNU-self-recoverable FF.

(3) They suffer from large overhead especially in terms of transmission delay, except the DICE-FF in [17].

To address the above-mentioned problems, this paper presents a novel interlocked-DICE-based *DNU-self-Recoverable and layout-Independent flip-flop* (*DURI-FF*) cell designed in an advanced 22nm CMOS technology. The master latch and the slave latch of the proposed DURI-FF cell are constructed from three interlocked DICEs that have three common nodes to achieve DNU-self-recoverability regardless of the energy of striking-particles. In the master latch, the common nodes are also used for value initialization from the input of the cell. In the slave latch, a common node is also used for outputting the stored values of the cell. The not-common-nodes of the master latch and the slave latch are connected through *transmission gates* (*TGs*) and inverters for correct logic function and timing. Simulation results demonstrate the correct working ability and DNU self-recoverability of the proposed DURI-FF cell at the cost of moderate power dissipation and silicon area. Moreover, compared with the state-of-the-art hardened FFs, the delay of the proposed DURI-FF cell is reduced.

The rest of this paper is organized as follows. Section II presents the schematic, normal working principles, and self-recoverability verifications of the proposed DURI-FF cell. Section III presents the comparison results for FFs. Section IV concludes the paper.

II. Proposed Flip-Flop Cell

A. Schematic, Normal Working Principles and Verifications

Fig. 2 shows the schematic of the proposed interlocked-DICEs-based *DNU-self-Recoverable Flip-Flop* (*DURI-FF*) cell, where the switches are TGs. For the clock-signal connections to a TG, for example, if it is marked with the *negative system clock* (*NCK*) signal, the gate-terminal of the PMOS transistor is connected to NCK and the gate-terminal of the NMOS transistor is connected to the *system clock* (*CLK*) signal. It can be seen from Fig. 2 that the DURI-FF cell comprises a master latch and a slave latch, each comprising three interlocked DICEs (i.e., DICEs A1 to C1 or A2 to C2) so as to achieve DNU self-recoverability. The common nodes (i.e., I1 to I3) of any pair of DICEs in the master latch are also used for value initialization of the DURI-FF cell through three TGs. The internal nodes (i.e., I1b1 to I3b1 as well as I1b2 to I3b2) of the master latch feed the coordinate internal nodes (i.e., Q, I5b1, I6b1, I4b1, I5b2, and I6b2) of the slave latch through serially-connected TG-and-inverters, respectively. In the slave latch, the internal nodes (i.e., I4 to I6) are used to connect any pair of its employed DICEs, respectively. D and Q are the input and the output of the DURI-FF cell, respectively.

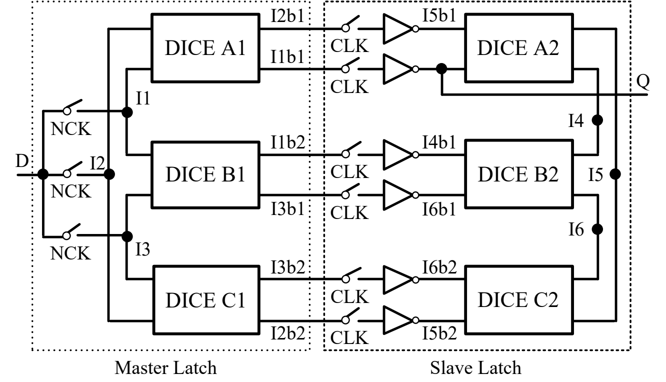

Fig. 2. Schematic of the proposed DURI-FF cell.

The normal operations of the proposed DURI-FF cell are as follows.

(1) Initially, when CLK = 1, the master latch of the cell works in transparent mode. Thus, the master latch can be initialized through three TGs. The slave latch has no values since the data-paths are blocked through the six TGs in itself.

(2) When CLK switches to 0, the master latch of the cell switches into hold mode. At this time, the slave latch enters into transparent mode and the six TGs in the slave latch are ON. Thus, the master latch stores the D-value and the slave latch receives and outputs the D-value of the master latch.

(3) When CLK switches to 1, the master latch receives the new D-value until the cell switches to the state in step (4) and the slave latch stores and outputs the previous D-value.

(4) When CLK switches to 0, the master latch stores the final new D-value in step (3) and the slave latch receives and outputs this D-value of the master latch.

Fig. 3 shows the simulation results for the normal operations of the proposed DURI-FF cell. Note that, for all simulations in this paper, the Synopsys HSPICE tool was used with an advanced 22nm CMOS library under the room temperature and the supply voltage VDD was set to 0.8V. From Fig. 3, the following cases can be observed.

(1) Initially, when CLK = 1, D = I1 = I2 = I3 and the values of all nodes in the master latch are pre-charged.

(2) Secondly, CLK switches to 0, the master latch stores the D-value (i.e., 0) and the slave latch receives and outputs the stored D-value of the master latch.

(3) Subsequently, CLK switches to 1, and thus the master latch receives the new D-value (I1 = I2 = I3 = D and they are changed from 0 to 1) and the slave latch stores and outputs the previous D-value (i.e., 0).

(4) Finally, When CLK switches to 0, the master latch stores the final new D-value (i.e., 1) in step (3) and the slave latch receives and outputs this D-value (i.e., 1) of the master latch. Therefore, only at the falling edge of the CLK signal can the

value of Q be changed to the value of D. The simulation results clearly demonstrate that the normal operations of the proposed DURI-FF cell are correct.

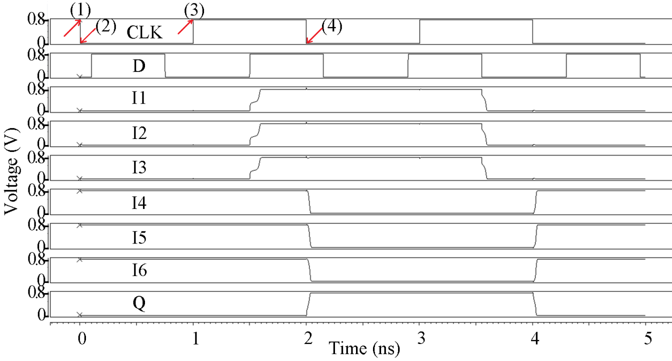

Fig. 3. Simulation results for normal operations of the proposed DURI-FF cell.

B. *Self-Recovery Principles and Verifications*

The SNU and DNU self-recovery principles of the proposed DURI-FF cell are described as follows. Since DICEs are self-recoverable from any possible SNU, the interlocked DICEs in either the master latch or the slave latch are still self-recoverable from any possible SNU. Therefore, the proposed DURI-FF cell can self-recover from SNUs.

Let us now describe the DNU self-recovery principles. Obviously, both the master latch and the slave latch should be considered in DNU self-recovery discussions in hold mode. It can be seen from Fig. 2 that the constructions of the master latch and the slave latch are equivalent when any of them works in hold mode. Thus, only the slave latch is considered in discussing the DNU self-recovery principles in hold mode. In this scenario, the TGs in the slave latch are OFF. Note that, the node-upset sensitivity of the input and the output of any inverter in the slave latch is equivalent. This is because whether the input of an inverter is affected or not, the affected/unaffected results can be observed in the output of the inverter. Therefore, only the output nodes of the inverters and the common nodes of DICEs A2 to C2 need to be considered in discussing the DNU self-recovery principles. Since the DICEs in the slave latch are equivalently constructed, there are only the following five cases that need to be discussed for DNU self-recovery.

Case 1: A DNU affects two inputs of a DICE. The indicative node-pair is only <I5b1, Q>.

In this case, it is clear that the outputs of DICE A2 are respectively the single-nodes of the SNU-self-recoverable DICEs B2 and C2 that are not affected. Thus, the outputs of DICE A2 are always correct due to the SNU-self-recoverability of DICEs B2 and C2. Note that the inputs and outputs of a DICE are reversible. Therefore, the correct outputs of DICE A2 can remove the errors in its inputs. In other words, <I5b1, Q> of the proposed DURI-FF cell can self-recover from the DNU.

Case 2: A DNU affects two single-inputs of two DICEs. The indicative node-pair is only <I5b1, I4b1>.

In this case, only the single-nodes of the SNU-self-recoverable DICEs A2 and B2 are respectively affected. Therefore, DICEs A2 and B2 can remove the errors caused by the DNU. In other words, <I5b1, Q> of the proposed DURI-FF cell can self-recover from the DNU.

Case 3: A DNU affects two common nodes of DICEs. The indicative node-pair is only <I4, I5>.

In this case, only the single-nodes of the SNU-self-recoverable DICEs B2 and C2 are respectively affected. Therefore, DICEs B2 and C2 can remove the errors caused by the DNU. In other words, <I4, I5> of the proposed DURI-FF cell can self-recover from the DNU.

Case 4: A DNU affects one input and one output of a DICE (or one output of another DICE since the output is a common node). The indicative node-pair is only <I4, Q>.

In this case, as for the SNU-self-recoverable DICE B2, only a single-node in it is affected. Thus, DICE B2 can remove its error on I4 caused by the DNU, and then DICE A2 can remove its error on Q caused by the DNU. In other words, <I4, Q> of the proposed DURI-FF cell can self-recover from the DNU.

Case 5: A DNU affects one input of one DICE and one output of another DICE (or one output of the third DICE since the output is a common node). The indicative node-pair is only <I6b2, I4>.

In this case, only the single-nodes of the SNU-self-recoverable DICEs A2 to C2 are respectively affected. Therefore, the DICEs can remove the errors caused by the DNU. In other words, <I6b2, I4> of the proposed DURI-FF cell can self-recover from the DNU.

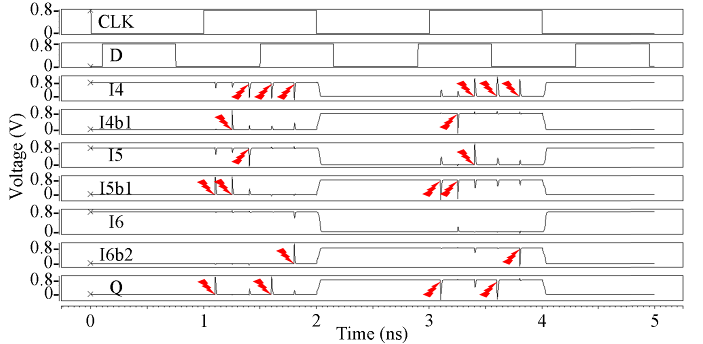

Fig. 4. Simulation results of all indicative DNU injections for the slave latch of the proposed DURI-FF cell.

Fig. 4 shows the simulation results of all indicative DNUs for the above-mentioned Cases 1 to 5 for the slave latch of the proposed DURI-FF cell. Note that, a popular and flexible double-exponential current-source model was also used for all fault-injections in this paper [21]. The time constant of the rise and fall of the current pulse was set to 0.1 ps and 3 ps, respectively. It can be seen from Fig. 4 that, at 1 ns to 2 ns, when Q = 0, a DNU was respectively injected to node-pairs <I5b1, Q>, <I5b1, I4b1>, <I4, I5>, <I4, Q>, and <I6b2, I4>. It can be seen from Fig. 4 that these node-pairs can self-recover from the injected DNUs. Moreover, at 3 ns to 4 ns, when Q = 1, a DNU was also respectively injected to node-pairs <I5b1, Q>, <I5b1, I4b1>, <I4, I5>, <I4, Q>, and <I6b2, I4>. It can be seen from Fig. 4 that these node-pairs can also self-recover from the injected DNUs. To summarize, the above introduced DNU self-recovery principles and simulations demonstrate that the proposed DURI-FF cell can self-recover from DNUs. Therefore, the DURI-FF cell can also self-recover from SNUs.

III. Comparison Results

To make a fair and comprehensive comparison with such typical state-of-the-art FFs, including the unhardened TUFF [23], the *triple-modular-redundancy* (*TMR*)-based TMR-FF

[14], the *triple-modular-redundancy-latch* (*TMRL*)-based TMRL-FF, the DRRH-FF [14], the Quatro-FF [15], the DNUR-FF [16], and the DICE-FF [17], the same simulation conditions described above were also used. Note that, the TMR-FF includes three TUFFs and a voter, but the TMRL-FF includes three TULs and a voter both for its master latch and slave latch. Tables I and II show the reliability and overhead comparison results among the unhardened and hardened FFs in terms of SNU/DNU tolerance and recoverability, CLK-to-Q delay, average power dissipation, and silicon area measured with the method in [21].

TABLE I
RELIABILITY COMPARISON RESULTS AMONG THE UNHARDENED AND HARDENED FLIP-FLOPS

Flip-Flops	SNU Tolerant	SNU Recoverable	DNU Tolerant	DNU Recoverable
TUFF [23]	×	×	×	×
TMR-FF [14]	√	×	×	×
TMRL-FF	√	×	×	×
DRRH-FF [14]	√	×	×	×
Quatro-FF [15]	√	×	×	×
DNUR-FF [16]	√	×	×	×
DICE-FF [17]	√	√	×	×
DURI-FF (Proposed)	√	√	√	√

TABLE II
OVERHEAD COMPARISON RESULTS AMONG THE UNHARDENED AND HARDENED FLIP-FLOPS

Flip-Flops	Delay (ps)	Power (μW)	10^2×Area (μm^2)
TUFF [23]	17.23	1.06	2.97
TMR-FF [14]	45.41	3.01	9.80
TMRL-FF	55.02	3.55	14.26
DRRH-FF [14]	43.01	1.58	5.94
Quatro-FF [15]	38.99	4.95	6.14
DNUR-FF [16]	42.39	2.71	11.29
DICE-FF [17]	17.19	1.72	5.64
DURI-FF (Proposed)	20.17	4.59	11.58

Reliability comparison results are shown in Table I. It can be seen that the TUFF cannot provide node-upset tolerance when suffering from an SNU or a DNU. This is because there is at least one counterexample that the TUFF [23] will output an invalid value if one of its single-nodes/node-pairs is affected by an SNU/DNU. The TMR-FF [14], TMRL-FF, DRRH-FF [14], and Quatro-FF [15] can tolerate SNUs. However, they cannot self-recover from SNUs due to the existence of at least one counterexample. The DNUR-FF [16] is SNU tolerant, but not SNU-self-recoverable. Moreover, although it is hardened, there is still at least one counterexample that it cannot tolerate a DNU. The DICE-FF [17] is not only SNU tolerant, but also SNU-self-recoverable. However, it cannot provide complete DNU tolerance although it is partially DNU hardened (see the second feature of DICEs on Page 1). It can be seen from Table I that only the proposed DURI-FF cell can provide the SNU/DNU tolerance and self-recoverability. Therefore, the proposed DURI-FF has the highest robustness.

Qualitative delay overhead comparison results are shown in Table II. For delay comparison, it can be seen that the TUFF, DICE-FF, and the proposed DURI-FF have a smaller delay. This is mainly because there are fewer devices/transistors from the transmission gate(s) of the slave latch to the output node Q for them. Note that only at the falling edge of CLK (i.e., when CLK is changing from high to low) Q can possibly be changed along with the stored D-value in the master latch. This is because CLK = 0 can make the slave latch to work in transparent mode and output the stored D-value in the master latch (Q may change). The other FFs have a larger delay since there are many devices/transistors in their CLK-to-Q paths. Especially for the TMR based FFs, the stored D-value has to pass through a voter to Q, resulting in a large delay.

Power and area comparison results are also shown in Table II. It can be seen that the TUFF and the DRRH-FF have lower power dissipation. This is mainly because these FFs use clock-gating to reduce current competition for power reduction. Another reason is that they use fewer transistors to reduce silicon area, resulting in lower power dissipation. Generally, an FF with fewer transistors/area consumes less power. It can be seen from Table II that, the DICE-FF has the smallest area among the hardened FFs, and thus it consumes less power as well. Note that, the Quatro-FF has the highest power dissipation. This is mainly because it respectively uses a Quatro SRAM cell as a storage part of its master/slave latch and an SRAM cell usually consumes more power due to much current competition. Moreover, it can be seen from Table II that the proposed DURI-FF has to use extra power/area to achieve its SNU/DNU self-recoverability. Clearly, its higher power dissipation is mainly due to the current competition and extra area. However, its power and area are not the largest. It can be seen from Table II that, the TMRL-FF consumes the largest area due to the use of the largest amount of transistors, but its power dissipation is not the highest since it has less current competition. Therefore, the high reliability of the proposed DURI-FF is mainly achieved at the cost of moderate silicon area and power dissipation compared with the other state-of-the-art hardened FFs.

Quantitative area overhead comparison results are not shown in Table II. However, the percentages of the reduced overhead of the proposed DURI-FF compared with the other FFs can be easily calculated. Due to the page limitation, detailed quantitative comparisons are omitted. The average-percentage of the reduced overhead of the proposed DURI-FF compared with the other SNU/DNU hardened FFs in term of the delay is 42.56%. In other words, the proposed DURI-FF can reduce approximately 43% delay at the cost of moderate power dissipation and silicon area. To summarize, the novel DNU (as well as SNU) self-recoverability of the proposed DURI-FF is achieved at the costs of extra indispensable power dissipation and silicon area, compared with the existing hardened FFs.

IV. CONCLUSION

This paper has proposed a novel DNU self-recoverable flip-flop, namely DURI-FF, at the cost of moderate silicon area and power dissipation. The interlocked DICEs in either the master latch or the slave latch make the DURI-FF self-recoverable from any possible SNU and DNU. The high-speed CLK-to-Q path leads to a smaller delay. The proposed DURI-FF can be effectively applied to safety-critical applications, such as aerospace, medical devices, autonomous cars, etc., where reliability is required.

References

[1] M. Hashimoto, K. Kobayashi, J. Furuta, et al., "Characterizing SRAM and FF Soft Error Rates with Measurement and Simulation," *Integration, the VLSI Journal*, under publication, pp. 1-19, 2019. DOI: 10.1016/j.vlsi.2019.03.005

[2] M. Gadlage, A. Roach, A. Duncan, et al., "Soft Errors Induced by High-Energy Electrons," *IEEE Trans. on Device & Materials Reliability,* vol. 17, no. 1, pp. 157-162, 2017.

[3] S. Cai, W. Wang, F. Yu, et al., "Single Event Transient Propagation Probabilities Analysis for Nanometer CMOS Circuits," *Journal of Electronic Testing - Theory and Applications*, vol. 35, no. 2, pp. 163-172, 2019.

[4] J. Black, P. Dodd, and K. Warren, "Physics of Multiple-Node Charge Collection and Impacts on Single-Event Characterization and Soft Error Rate Prediction," *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1836-1851, 2013.

[5] C. Liu, N. Liu, Z, Lin, et al., "A Single Event Upset Tolerant Latch with Parallel Nodes," *IEICE Electronics Express*, vol. 16, no. 11, pp. 1-6, 2019.

[6] Z. Huang, H. Liang, and S. Hellebrand, "A High Performance SNU Tolerant Latch," *Journal of Electronic Testing*, vol. 31, no. 4, pp. 349-359, 2015.

[7] R. Rajaei, M. Tabandeh, and M. Fazeli, "Single Event Multiple Upset (SEMU) Tolerant Latch Designs in Presence of Process and Temperature Variations," *Journal of Circuits, Systems and Computers*, vol. 24, no. 1, pp. 1-3, 2015.

[8] N. Eftaxiopoulos, N. Axelos, G. Zervakis, et al., "Delta DICE: A Double Node Upset Self-Recoverable Latch," *IEEE International Midwest Symposium on Circuits and Systems*, Fort Collins, USA, pp. 1-4, 2015.

[9] C. Peng, J. Huang, C. Liu, et al., "Radiation-Hardened 14T SRAM Bitcell with Speed and Power Optimized for Space Application," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 2, pp. 407-415, 2019.

[10] R. Rajaei, B. Asgari, M. Tabandeh, et al., "Design of Robust SRAM Cells Against Single-Event Multiple Effects for Nanoscale Technologies," *IEEE Transactions on Device and Materials Reliability*, vol. 15, no. 3, pp. 429-436, 2015.

[11] N. Yadav, A. Shah, and S.Vishvakarma, "Stable, Reliable and Bit-Interleaving 12T SRAM for Space Applications: A Device Circuit Co-Design," *IEEE Transactions on Semiconductor Manufacturing*, vol. 30, no. 3, pp. 276-284, 2017.

[12] C. Peng, Z. Chen, J. Zhang, et al., "A Radiation Harden Enhanced Quatro (RHEQ) SRAM Cell," *IEICE Electronics Express*, vol. 14, no. 18, pp. 1-12, 2017.

[13] K. Kobayashi, K. Kubota, M. Masuda, et al., "A Low-Power and Area-Efficient Radiation-Hard Redundant Flip-Flop, DICE ACFF, in a 65 nm Thin-BOX FD-SOI," *IEEE Transactions on Nuclear Science*, vol. 61, no. 4, pp. 1881-1888, 2014.

[14] G. Jaya, S. Chen, and S. Liter, "A Dual Redundancy Radiation-Hardened Flip-Flop Based on C-element in 65nm Process," *IEEE International Symposium on Integrated Circuits (ISIC2016)*, Singapore, pp. 1-4, 2016.

[15] Y. Li, H. Wang, R. Liu, et al., "A Quatro-Based 65 nm Flip-Flop Circuit for Soft-Error Resilience," *IEEE Transactions on Nuclear Science*, vol. 64, no. 6, pp. 1554-1561, 2017.

[16] F. Alghareb and R. DeMara, "Design and Evaluation of DNU-Tolerant Registers for Resilient Architectural State Storage," *ACM Great Lakes Symposium on VLSI (GLSVLSI2019)*, Washington D. C., USA, pp. 1-4, 2019.

[17] R. Yamamoto, C. Hamanaka, J. Furuta, et al., "An Area-Efficient 65 nm Radiation-Hard Dual-Modular Flip-Flop to Avoid Multiple Cell Upsets," *IEEE Transactions on Nuclear Science*, vol. 58, no. 6, pp. 3053-3059, 2011.

[18] S. Campitelli, M. Ottavi, S. Pontarelli, et al., "F-DICE: A Multiple Node Upset Tolerant Flip-Flop for Highly Radioactive Environments," *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT2013)*, pp. 107-111, 2013.

[19] B. Xia, J. Wu, H. Liu, et al., "Design and Comparison of High-Reliable Radiation-Hardened Flip-Flops Under SMIC 40nm Process," *Journal of Circuits, Systems, and Computers*, vol. 25, no. 12, pp. 1-19, 2016.

[20] T. Calin, M. Nicolaidis, and R. Velazco, "Upset Hardened Memory Design for Submicron CMOS Technology," *IEEE Transactions on Nuclear Science*, vol. 43, no. 6, pp. 2874-2878, 1996.

[21] A. Yan, L. Lai, Y. Zhang, et al, "Novel Low Cost, Double-and-Triple-Node-Upset-Tolerant Latch Designs for Nano-scale CMOS," *IEEE Transactions on Emerging Topics in Computing*, vol. 99, pp. 1-14, 2018.

[22] H. Li, L. Xiao, J. Li, et al, "High Robust and Cost Effective Double Node Upset Tolerant Latch Design for Nanoscale CMOS Technology," *Microelectronics Reliability*, vol. 93, pp. 89-97, 2019.

[23] X. She, N. Li and J. Tong, "SEU Hardened Flip-Flop Based on Dynamic Logic," *IEEE Transactions on Nuclear Science*, vol. 60, no. 5, pp. 3932-3936, 2013.