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***Abstract*—In this paper, we propose a sextuple cross-coupled SRAM cell, namely SCCS18T, protected against double-node upsets. Since the proposed SCCS18T cell forms a large feedback loop for value retention and error interception, the cell can self-recover from all possible single-node upsets (SNUs) and a part of double-node upsets (DNUs). Moreover, the proposed cell has optimized operation speed due to the use of parallel access transistors. Simulation results demonstrate that the proposed SCCS18T cell can approximately save 65% read access time at the cost of 49% power dissipation and 50% silicon area on average, compared with the state-of-the-art hardened SRAM cells.**

I. Introduction

With the aggressive CMOS technology scaling, circuit integration is becoming much higher and the sizes of SRAMs are becoming much smaller. Meanwhile, the amount of critical charge stored on a node in a circuit is reducing because of the decrease of supply voltages and node capacitances. As a result, modern advanced SRAMs become more sensitive to the strike of particles, such as protons, neutrons, heavy ions, electrons, muons, and alpha particles [1-2]. The strike of particles may lead to soft errors and even system failures that give circuit designers a challenge on reliability problems. Therefore, it is crucial to propose hardened SRAM cells protected against soft errors. The recent adoption of FinFET technologies can reduce the soft error rate at transistor or cell level [3]. However, this feature of FinFET-based circuits is insufficient to exempt designers to provide valuable and scalable solutions for soft error tolerance, especially for safety-critical applications in harsh environments.

When a particle strikes a sensitive region (drain) of a transistor in a combinational circuit, the collected charge can be transported by drift and causes a transient current pulse, i.e., a *single event transient* (*SET*) [4]. On the other hand, the particle may directly strike an OFF-state transistor in a storage element, causing a *single-node upset* (*SNU*). Moreover, the distance between storage nodes is becoming much closer due to higher circuit integration and smaller transistor sizes. Once a particle hits the circuit, two OFF-state transistors may be affected simultaneously, resulting in a *double-node upset* (*DNU*). Indeed, SNUs and DNUs can cause invalid value-retention in SRAM cells, which becomes a serious concern in modern advanced circuits and systems.

In order to mitigate SNUs and/or DNUs, a series of novel designs of latches [5-7], flip-flops [8-10], and SRAMs [11-16] have been proposed based on the *radiation hardening by design* (*RHBD*) approach. The conventional 6T cell mainly consists of a couple of cross-coupled inverters. Since the 6T cell is more vulnerable to soft errors, researchers have proposed many radiation hardened SRAM cells to improve robustness. Typical SNU and/or even DNU hardened cells include NASA13T [11], RHPD12T [12], RHBD10T [13], RHM12T [14], RHD12T [15], and Lin12T [16]. However, these SRAMs still suffer from the following problems.

(1) Some SRAMs have large overhead especially in terms of read access time such as NASA13T [11], RHBD10T [13], RHM12T [14], and Lin12T [16]. Moreover, some SRAMs also have large write access time and power dissipation, such as NASA13T [11].

(2) Some SRAMs cannot provide complete SNU self-recoverability, such as NASA13T [11], RHPD12T [12], RHBD10T [13], RHM12T [14], and RHD12T [15].

(3) They are not effectively DNU hardened, such as NASA13T [11], RHPD12T [12], RHBD10T [13], RHM12T [14], RHD12T [15], and Lin12T [16].

Our previously proposed SRAM cell in [17], although it has small overhead, still suffers from the problem that it cannot provide complete self-recoverability from SNUs. Our previously proposed so-called DNUSRM SRAM cell in [18] can provide self-recoverability from SNUs and DNUs, but it suffers from large area and power overhead. To balance self-recoverability and overhead, based on the RHBD approach, this paper proposes a reliable SRAM cell which only consists of six PMOS and 12 NMOS transistors. Owing to the use of a special feedback mechanism, the proposed cell can self-recover from all possible SNUs and a part of DNUs. In addition, the proposed cell has less overhead especially in terms of read/write access time by using six parallel access-transistors. Simulation results demonstrate the reliability and cost-effectiveness of the proposed cell.

The rest of this paper is organized as follows. Section II describes the schematic and working principles of the proposed SRAM cell. Section III presents the comparison and evaluation results. Section IV concludes the paper.

II. Proposed SRAM Cell

A. Schematic and Normal Operations

The schematic of the proposed SCCS18T cell is shown in Fig. 1. The SCCS18T cell consists of six PMOS transistors (P1-P6) and 12 NMOS transistors (N1-N12). The access transistors N7 to N12, which are controlled by the word-line (WL), connect the bit-lines (BL and BLN) to the main storage

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nodes I1, I2, I3, I4, I5, and I6, respectively. When WL = 1, the access transistors are ON, allowing read/write operations to be executed. When WL = 0, the cell keeps the stored value.

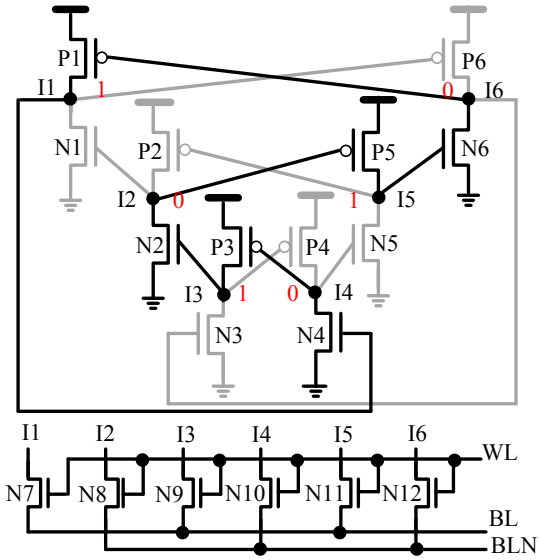

Fig. 1. Schematic of the proposed SCCS18T cell.

The normal operations of the proposed SCCS18T cell are described as follows. When WL = 0, the proposed SCCS18T works in hold mode and the access transistors are OFF. In this mode, let us assume that the SCCS18T cell previously stores 0, i.e., I1 = I3 = I5 = 0 and I2 = I4 = I6 = 1. Now, let us consider a write operation. Before the operation of writing a 1, BL = 1 and BLN = 0. When WL = 1, transistors P1, N4, P3, N2, P5 and N6 are ON while the other transistors are OFF, as shown in Fig. 1. Thus, a large feedback loop (I1 → I4 → I3 → I2 → I5 → I6 → I1) is constructed in the cell and a value 1 is written into the SCCS18T cell successfully. Next, let us consider a read operation. Before the operation of reading a 1, BL and BLN are precharged to logic 1. When WL = 1, the voltage of BLN is discharged to logic 0 through N8, N10, N12, and the voltage of BL remains logic 1. The resulting differential voltage between BL and BLN is detected by the sense amplifier and the value is read out. For writing/reading 0, a similar behavior can be observed.

The cell was implemented using a 22nm commercial CMOS technology under room temperature and a supply voltage of 0.8V. Fig. 2 shows the simulation results for normal operations of the proposed SCCS18T cell. It can be seen that a series of write 0, read 0, write 1, and read 1 operations were correctly executed and these written values were correctly retained in the proposed cell.

The fault-tolerance principles of the proposed SCCS18T cell are described as follows. Here, we use the case of 1 being stored (I1 = I3 = I5 = 1 and I2 = I4 = I6 = 0) for illustration. First, we discuss the SNU self-recovery principle.

B. SNU Self-Recovery Principle

First, let us discuss the case where node I1 is affected by an SNU. When node I1 is temporarily flipped to 0 from 1, transistor N4 will be temporarily OFF, and transistor P6 will be temporarily ON. Obviously, nodes I2, I3, and I5 are not affected immediately, so that transistor P4 still remains OFF. Thus, I4 still remains at the original correct value 0, and transistor N5 still remains OFF. Hence, I5 still remains at the original correct value 1, so that transistor P2 still remains OFF (I2 still remains the original correct value 0, and transistor N1 still remains OFF), and transistor N6 still remains ON (I6 still outputs 0, i.e., strong 0). Meanwhile, the fact that I1 is temporarily flipped to 0 from 1 can cause P6 to be ON temporarily and I6 outputs 1 (weak 1). However, the strong 0 of I6 can neutralize this weak 1, and hence I6 is still correct (I6 = 0), so that transistor N3 still remains OFF (I3 still remains at the original correct value 1), and transistor P1 still remains ON. As mentioned above, transistor N1 still remains OFF. Thus, I1 can self-recover to 1, so that transistor P6 returns to be OFF and transistor N4 returns to be ON. Therefore, all transistors can return to their original states.

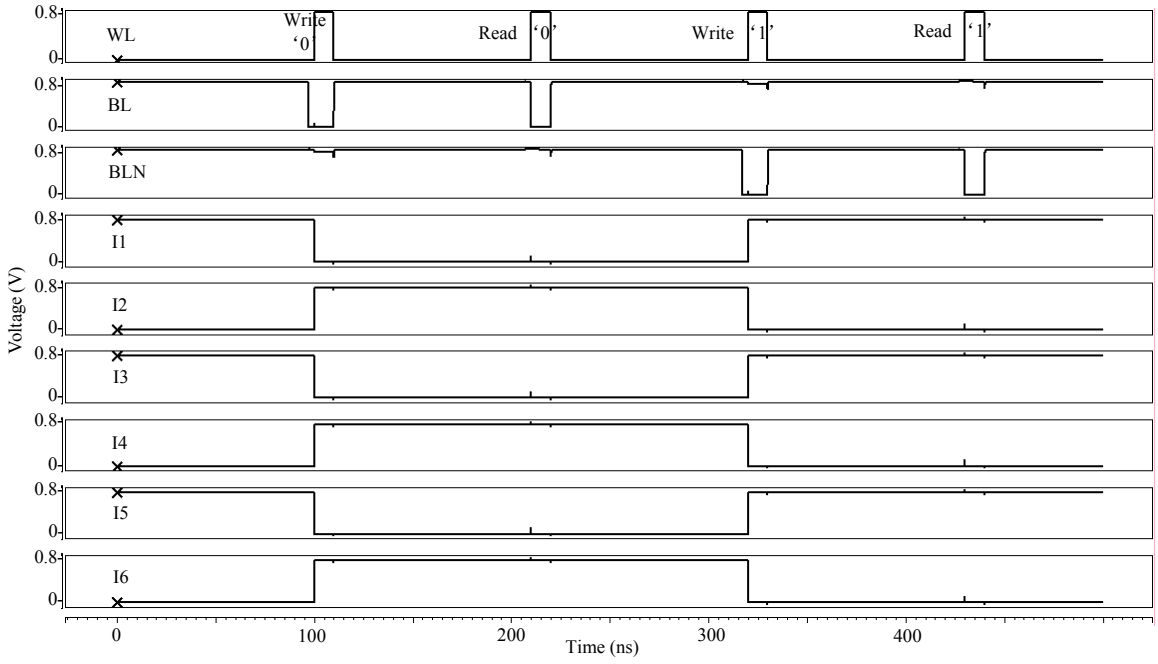

Fig. 2. Simulation results for normal operations of the proposed SCCS18T cell.

Clearly, I1 can self-recover from the SNU.

Next, let us discuss the case where node I2 is affected by an SNU. When node I2 is temporarily flipped to 1 from 0, transistor P5 will be temporarily OFF, and transistor N1 will be temporarily ON, so that I1 outputs 0 (weak 0). Obviously, nodes I3, I4 and I6 are not affected immediately, so that transistor P1 still remains ON, I1 still outputs 1 (strong 1). The strong 1 of I1 can neutralize this weak 0, and hence I1 is still correct (I1 = 1), so that transistor P6 still remains OFF. Thus, I6 still remains at the original correct value 0, and transistor N3 still remains OFF. Thus, I3 still remains at the original correct value 1, so that transistor N2 still remains ON and transistor P4 still remains OFF. Thus, I4 still remains at the original correct value 0, so that transistor N5 still remains OFF. Thus, I5 still remains at the original correct value 1, so that transistor P2 still remains OFF. As mentioned above, transistor N2 still remains ON. Thus, I2 can self-recover to 0, so that transistor N1 returns to be OFF and transistor P5 returns to be ON. Therefore, all transistors can return to their original states. Clearly, I2 can self-recover from the SNU. As for any other single-node, the similar SNU self-recovery principle can be observed. In summary, the proposed cell can self-recover from SNUs.

Figure 3 shows the simulation results for SNU self-recovery on nodes I1, I2, I3, I4, I5, and I6 of the proposed SCCS18T cell. As shown in Fig. 3, when I1 = 1, SNUs were respectively injected on nodes I1, I2, I3, I4, I5, and I6 at 40 ns, 80 ns, 340 ns, 380 ns, 420 ns, and 460 ns, respectively. When I1 = 0, SNUs were respectively injected on nodes I1, I2, I3, I4, I5, and I6 at 260 ns, 300 ns, 120 ns, 160 ns, 200ns, and 240ns, respectively. It can be seen from Fig. 3 that the proposed SCCS18T cell can self-recover from SNUs.

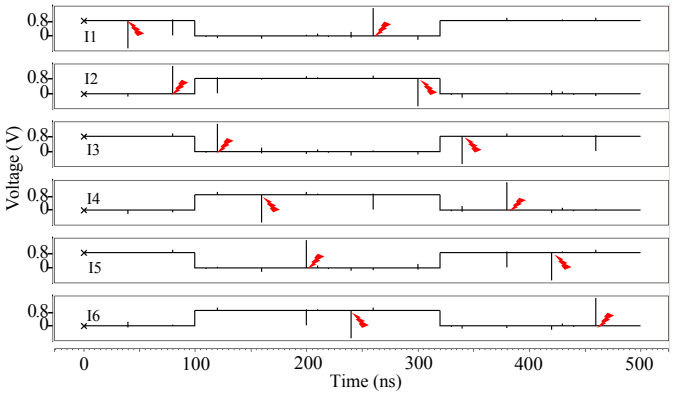

Fig. 3. Simulation results for SNU self-recovery of the proposed SCCS18T cell.

C. DNU Self-Recovery Principle

First, let us discuss the case where <I1, I2> suffers from a DNU. In this case, I1 is temporarily changed to 0 from 1 and I2 is temporarily changed to 1 from 0. Thus, transistors N4 and P5 become temporarily OFF and transistors P6 and N1 become temporarily ON. Obviously, node I3 is not affected immediately, so that transistor P4 still remains OFF. Thus, I4 still remains at the original correct value 0, so that transistor N5 still remains OFF. Thus, I5 still remains at the original correct value 1, transistor P2 still remains OFF, transistor N6 still remains ON, and I6 outputs 0 (strong 0). Meanwhile, the fact that I1 is temporarily flipped to 0 from 1 can cause P6 to be ON temporarily and I6 outputs 1 (weak 1). However, the strong 0 of I6 can neutralize this weak 1, and hence I6 is still correct (I6 = 0), so that transistor P1 still remains ON and transistor N3 still remains OFF. Thus, I3 still remains at the original correct value 1, so that transistor N2 still remains ON. As mentioned above, transistor P2 still remains OFF. Thus, I2 can self-recover to 0, so that transistor P5 returns to be ON and transistor N1 returns to be OFF. As mentioned above, transistor P1 still remains ON and transistor N1 returns OFF. Thus, I1 can self-recover to 1, so that transistor N4 returns to be ON and transistor P6 returns to be OFF. Therefore, all transistors return to their original states. Clearly, <I1, I2> of the proposed SCCS18T cell can self-recover from the DNU. Due to the symmetry of the proposed SCCS18T cell, <I5, I6> has a similar DNU self-recovery principle, i.e., <I5, I6> can also self-recover from the DNU.

Next, let us discuss the case where <I3, I6> suffers from a DNU. In this case, I3 is temporarily changed to 0 from 1 and I6 is temporarily changed to 1 from 0. Thus, transistors N2 and P1 become temporarily OFF and transistors P4 and N3 become temporarily ON. Obviously, node I5 is not affected immediately, so that transistor P2 still remains OFF. Thus, I2 still remains at the original correct value 0, so that transistor N1 still remains OFF. Thus, I1 still remains at the original correct value 1, transistor P6 still remains OFF, transistor N4 still remains ON, and I4 outputs 0 (strong 0). Meanwhile, the fact that I3 is temporarily flipped to 0 from 1 can cause P4 to be ON temporarily and I4 outputs 1 (weak 1). However, the strong 0 of I4 can neutralize this weak 1, and hence I4 is still correct (I4 = 0), so that transistor P3 still remains ON and transistor N5 still remains OFF. Thus, I5 still remains at the original correct value 1, so that transistor N6 remains ON. As mentioned above, transistor P6 still remains OFF. Thus, I6 can self-recover to 0, so that transistor P1 returns to be ON and transistor N3 returns to be OFF. As mentioned above, transistor P3 still remains ON. Thus, I3 can self-recover to 1, so that transistor N2 returns to be ON and transistor P4 returns to be OFF. Therefore, all transistors return to their original states. Clearly, <I3, I6> of the proposed SCCS18T cell can self-recover from the DNU. Due to the symmetry of the proposed SCCS18T cell, <I1, I4> has a similar DNU self-recovery principle, i.e., <I1, I4> can also self-recover from the DNU.

Finally, let us discuss the case where <I4, I5> suffers from a DNU. In this case, I4 is temporarily changed to 1 from 0 and I5 is temporarily changed to 0 from 1. Thus, transistors P3 and N6 become temporarily OFF and transistors N5 and P2 become temporarily ON. Obviously, node I1 is not affected immediately, so that transistor P6 still remains OFF. Thus, I6 still remains at the original correct value 0, so that transistor N3 still remains OFF. Thus, I3 still remains at the original correct value 1, transistor P4 still remains OFF, transistor N2 still remains ON, and I2 outputs 0 (strong 0). Meanwhile, the fact that I5 is temporarily flipped to 0 from 1 can cause P2 to

be ON temporarily and I2 outputs 1 (weak 1). However, the strong 0 of I2 can neutralize this weak 1, and hence I2 is still correct (I2 = 0), so that transistor P5 remains ON and transistor N1 remains OFF. Thus, I1 still remains at the original correct value 1, so that transistor N4 remains ON. As mentioned above, transistor P4 still remains OFF. Thus, I4 can self-recover to 0, so that transistor P3 returns to be ON and transistor N5 returns to be OFF. As mentioned above, transistor P5 still remains ON. Thus, I5 can self-recover to 1, so that transistor N6 returns to be ON and transistor P2 returns to be OFF. Therefore, all transistors return to their original states. Clearly, <I4, I5> of the proposed SCCS18T cell can self-recover from the DNU. Due to the symmetry of the proposed SCCS18T cell, <I2, I3> has a similar DNU self-recovery principle, i.e., <I2, I3> can also self-recover from the DNU.

To summarize, when the proposed SCCS18T cell stores 1, node pairs <I1, I2>, <I3, I6>, and <I4, I5> of the cell can self-recover from a DNU; when the proposed SCCS18T cell stores 0, node pairs <I1, I4>, <I2, I3>, and <I5, I6> of the cell can self-recover from a DNU, namely, up to 6 node pairs of the proposed cell can self-recover from DNUs.

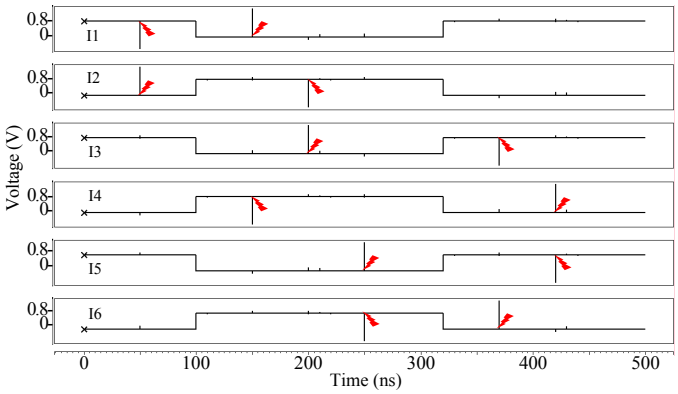

Fig. 4. Simulation results for DNU self-recovery of the proposed SCCS18T cell.

Figure 4 shows the simulation results for DNU self-recovery of the proposed SCCS18T cell. As shown in Fig. 4, when I1 = 1, DNUs were respectively injected on three node pairs <I1, I2>, <I3, I6>, and <I4, I5> at 50 ns, 370ns, and 420 ns. When I1 = 0, DNUs were respectively injected on three node pairs <I1, I4>, <I2, I3>, and <I5, I6> at 150 ns, 200 ns, and 250 ns. It can be seen from Fig. 4 that the proposed cell can self-recover from the DNUs.

In the above-mentioned fault-injections, a popular and flexible double-exponential current-source model was used, and the time constant of the rise and fall of the current pulse was set to 0.1 and 3.0 ps, respectively [19]. All simulations were performed using the Synopsys HSPICE tool with the 22nm CMOS library under room temperature and a supply voltage of 0.8V.

III. Comparison and Evaluation

To make a fair comparison, the state-of-the-art SRAM cells described in Section I were also implemented under the same simulation conditions as for the proposed SCCS18T cell. Table I shows the reliability and overhead comparison results among the unhardened/hardened SRAM cells in terms of *SNU recoverability* (*SNUR*), *number of DNU-hardened node-pairs* (*#DHNPs*), *read access time* (*RAT*), *write access time* (*WAT*), average power dissipation (dynamic and static), and silicon area measured with the method in [19].

First, let us describe the reliability comparison. It can be seen from Table I that the proposed SCCS18T cell can self-recover from all possible SNUs as validated in Section II, while the other SNU hardened cells except the Lin12T cannot provide a complete SNU self-recoverability from SNUs. For DNUs, it can be seen from Table I that, the 6T, NASA13T, RHPD12T, and RHBD10T cells have no DHNP, the RHM12T and RHD12T cells have one DHNP, and the Lin12T cell has two DHNPs. Clearly, the proposed SCCS18T cell has the largest number of DHNPs which is 6. In summary, the proposed SCCS18T cell is more reliable than the other cells.

Next, let us describe the qualitative overhead comparison for the hardened SRAMs listed in Table I. For RATs, Table I shows that the proposed SCCS18T cell has the smallest RAT due to the use of six parallel access transistors for reading a value. In comparison, the NASA13T cell has the largest RAT because it has specified extra read transistors. For WATs, Table I shows that the RHPD12T, RHBD10T, RHM12T, and Lin12T cells have a comparatively small WAT, mainly because these cells have less current competition when executing write operation. Conversely, the NASA13T cell has the largest WAT because of more current competition when executing write option. Compared with the other hardened cells, the proposed SCCS18T cell has a small WAT.

TABLE I
Reliability and Overhead Comparison Results among the Unhardened/Hardened SRAM Cells.

	6T	NASA13T	RHPD12T	RHBD10T	RHM12T	RHD12T	Lin12T	SCCS18T
Ref.	-	[11]	[12]	[13]	[14]	[15]	[16]	Proposed
SNUR	×	×	×	×	×	×	√	√
#DHNPs	0	0	0	0	1	1	2	6
RAT (ps)	25.88	128.67	17.34	21.09	38.11	13.46	37.68	8.64
WAT (ps)	3.65	16.39	3.51	3.05	4.28	4.80	3.78	4.50
Power (nW)	5.24	18.92	9.35	11.75	7.89	10.43	9.74	15.63
10^{-3}×Area (nm^2)	4.35	9.07	9.72	6.86	9.28	8.71	9.28	13.07

For power and area, Table I shows that the 6T cell has the smallest power and area due to the use of only six transistors.,The NASA13T has the largest power mainly due to the large current competition in its feedback loop. The RHPD12T, RHD12T, and Lin12T cells have similar power dissipation mainly due to their identical amount of used transistors and similar cell constructions. It can be seen from Table I that the proposed SCCS18T cell has larger power and area mainly due to the use of extra transistors to improve the self-recoverability from all possible SNUs and a part of DNUs as well as optimized access operations. In other words, the high reliability and optimized access operations of the proposed SCCS18T cell are mainly achieved at the cost of extra indispensable silicon area and power dissipation compared with the other hardened SRAM cells.

$$PRC_{RAT}=\frac{RAT_{\text{compared}}(i)-RAT_{\text{proposed}}}{RAT_{\text{compared}}(i)}\times 100\% \quad (1)$$

$$PRC_{RAT}^{\text{average}}=\frac{1}{n}\sum_{i=1}^{n}\frac{RAT_{\text{compared}}(i)-RAT_{\text{proposed}}}{RAT_{\text{compared}}(i)}\times 100\% \quad (2)$$

Finally, we describe the quantitative overhead comparison. The *percentages of reduced costs* (*PRCs*) were calculated to quantitatively discuss the overhead comparison for SRAMs. The PRC of the RAT was calculated with Eq. (1). The PRCs of the WAT, power dissipation, and silicon area can be calculated similarly,. The average PRCs of the RAT was calculated with Eq. (2). Here, we only discuss the average PRCs for the brevity of the paper. Compared with the other typical hardened cells, the average PRCs of the RAT, WAT, power dissipation, and silicon area are 65.45%, -3.52%, -48.54%, and 50.14%, respectively. In other words, the proposed SCCS18T cell achieves a 65.45% RAT reduction mainly at the cost of 48.54% power dissipation and 50.14% silicon area on average, compared with the state-of-the-art hardened cells.

IV. Conclusions and Further Work

As CMOS technology scaling down, the conventional memory cells are more susceptible to soft errors such as SNUs and DNUs. A novel so-called SCCS18T SRAM cell with high reliability and optimized operation speed has been proposed in this paper. Compared with the state-of-the-art radiation hardened SRAM cells, the proposed SCCS18T cell is not only self-recoverable from all possible SNUs and a part of DNUs, but also has better circuit performance (due to the use of six parallel access transistors). Therefore, the proposed SCCS18T cell can be effectively applied to safety-critical applications, such as aerospace, where high reliability and better performance is indispensable.

It is reported in [20] that *static noise margin* (*SNM*) is an important metric to analyze stability of SRAM cells for normal operations. In our further work, efforts will be done to perform SNM simulations, and analyze the results.

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