Deliverable D4.1 – State of the art on performance and power estimation of embedded and high-performance cores

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CONTINUUM

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Executive Summary

The goal of the CONTINUUM project is to define a new energy-efficient compute node model, which will benefit from a suitable combination of efficient compilation techniques, emerging memory, and communication technologies together with heterogeneous cores. The originality of the solution promoted by the project is to consider the core technology of the Cortus partner.

The current deliverable presents a number of candidate core technologies, mainly from Cortus and ARM. Performance and power consumption numbers are given as an assessment of all these technologies. The outcome of the present survey will serve in choosing the suitable core technologies in the expected heterogeneous architecture.

1 Introduction

In embedded computing, while the systems power budget is still confined to a few watts, the performance demand is growing. This comes from the continuous integration of new functionalities in systems, e.g. in mobile computing. To address this demand, the number of cores in systems has been increasing. At the same time, in the HPC domain, supercomputers are expected around 2020 to achieve 10^{18} floating-point operations per second (FLOPS) also referred to as exascale computing, within a power budget of 20MW [6]. With current technologies, such a supercomputer would require a similar power budget to that of a European mid-size city, therefore calling for new design solutions. These observations from both embedded and HPC domains draw their convergence towards finding the best ratio between performance and power consumption, i.e., energy-efficiency.

One solution consists in using embedded technologies in HPC systems in order to take advantage of their inherent low power consumption. This is the vision considered in the European MontBlanc project [38]. The project developed a prototype of large-scale HPC architecture integrating ARM embedded cores for energy-efficiency. In [34], the scalability and energy-efficiency of three multiprocessor-on-chip (MPSoCs) within compute clusters are evaluated. These MPSoCs are PandaBoard, Snowball and Tegra. They all contain ARM Cortex-A9 processors. In [5], a similar study is reported, which aims to assess the possible benefits of ARM core-based clusters compared to those relying on commodity processors such as x86, for HPC.

Another study [33] compared ARM-based clusters against Intel X86 workstation, by evaluating both their energy-efficiency and cost-efficiency. The reported experiments showed that the ARM clusters enable a better energy-efficiency ratio against the Intel workstation, e.g. up to 9.5 for in-memory database, and around 1.3 for Web server application. Note that the relevant measurement of the power consumption in the addressed systems highly depends on the reliability of the applied data collection tools. In [35], a platform-independent tool is devoted to this aim while targeting both homogeneous and heterogeneous systems. Such a tool a worth-mentioning for our forthcoming studies.

This deliverable presents an assessment of selected candidate core technologies, with relevant features to be explored for the compute node architecture targeted in the CONTINUUM project. Usual design assessment techniques rely on flexible system descriptions at different abstraction levels for a comfortable design space exploration [29, 30]. The techniques can follow general modeling paradigms, e.g. UML [19, 16, 37, 4], analytical modeling [11, 3, 2], transaction-level modeling[39, 27, 28, 31], cycle-accurate or cycle-approximate modeling [7, 10, 8, 9], and ultimately hardware prototyping [45].

In this work, we consider hardware prototypes as a baseline to evaluate the identified key metrics. As stated in the project proposal, the core technologies from the Cortus partner are given high attention in this project, as they are inherently energy-efficient. They offer a set of cores with different capabilities in terms of performance and power consumption tradeoff. This opens an interesting opportunity for building multicore heterogeneous architectures in which cores can be selected for execution depending on workload nature, so as to reduce as much as possible the dissipated energy while meeting the performance requirements [44, 26].

An existing similar heterogeneous multicore architecture is ARM big.LITTLE [22]. It basically consists of two clusters of cores as illustrated in Figure 1.

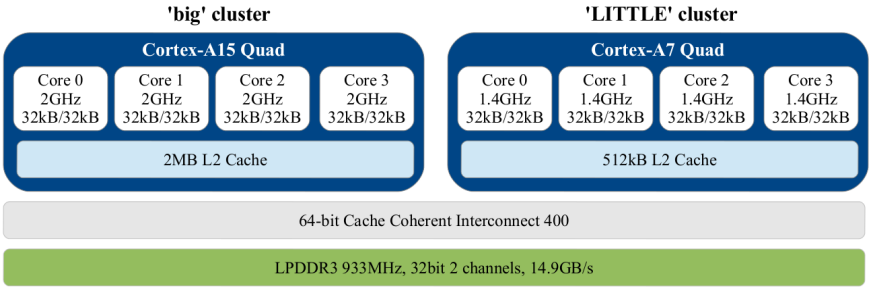


Figure 1: Sketch of the big.LITTLE technology integrated in the Exynos 5422 System-on-Chip.

The "big" cluster is composed of high-performance cores while the "LITTLE" cluster contains low power cores. The main idea behind this design is to select a suitable cluster according to the performance and power demand of executed workloads. While the traditional big.LITTLE configurations rely on application processors only, such as ARM Cortex-A7 or Cortex-A15, the CONTINUUM project aims to integrate also ultra-compact cores, such as Cortus cores which belong to the micro-controllers class. The target compute node architecture should be capable of supporting a full operating system, basically running on application processors. The presence of Cortus cores in the resulting heterogeneous architecture will increase its energy-efficiency. As there is not yet heterogeneous multicore architectures based on Cortus cores, we will consider some existing compute nodes integrating ARM big.LITTLE technology to carry out our preliminary investigations in the CONTINUUM project. The gained insights will serve in designing our solution with Cortus cores.

Outline. The rest of this deliverable is organized as follows. First, an overview of Cortus low power cores is given, together with a comparison against similar ARM low power cores in Section 2. Then, the energy-efficiency of a specific ARM big.LITTLE multicore system is evaluated based on the HPL and Rodinia benchmarks in Section 3. This case study gives some preliminary assessment of what one could expect from such a technology. A quick survey of some popular multi/manycore architectures is presented in Section 4. Finally, a few concluding remarks are provided in Section 5.

2 Very low power cores: Cortus versus ARM

We evaluate some selected CPU cores developed by the Cortus Company. The cores are compared with equivalent well-known ARM cores in order to provide the reader with a convenient comparison basis.

2.1 Overview

A possible design option investigated by the CONTINUUM project for energy-efficient compute nodes is a heterogeneous multicore architecture composed of many low power cores and a few high-performance cores. The candidate core technologies are those developed by the Cortus[1] partner. The current section briefly introduces the current processor families proposed by Cortus (Section 2.2). A comparison with similar ARM processors is also discussed (Section 2.3).

2.2 Cortus core technologies

The Cortus range of processors is all modern advanced 32-bit RISC processors, featuring the same core architecture and instruction set. However, they differ in silicon footprint and performance. Generally speaking, systems that are silicon and power-sensitive will find the APS processor family ideal. Applications demanding more performance and floating-point operations will find the high throughput FPS processors more suitable.

As illustrated in Table 1, within each family, one can distinguish processors that are designed so as to provide an *optimized core size* without compromising the performance. Other processors are designed in a way that increases their *code density*, therefore their instruction memory size. The increased code density comes at the expense of a slightly more complex processor core.

Table 1: Two families of Cortus processors (**typical area in 90 nm technology node**).

Family 1: optimized core size		**Family 2: optimized code density**	
APS1	0.039 mm2		
APS3R	0.043 mm2	APS23	0.049 mm2
APS3RP	0.079 mm2	APS23P	0.084 mm2
APS5	0.095 mm2	APS25	0.103 mm2
FPS6	0.185 mm2	FPS26	0.192 mm2

A typical architecture: APS25. The APS25 processor architecture depicted in Figure 2 is a fully 32-bit high-performance general purpose CPU, with an excellent code density (and a marginal increase in silicon area compared to APS5), designed specifically to meet the demands of embedded systems.

It relies on a Harvard architecture with 2 $\times$ 4 GB address space. The instructions are 16, 24 and 32 bits in length. Most of them are single cycle, including load and store. The 5-7 stage pipeline ensures ultra low power consumption and high-performance while retaining a reasonable maximum

[1] `http://www.cortus.com/overview.php`

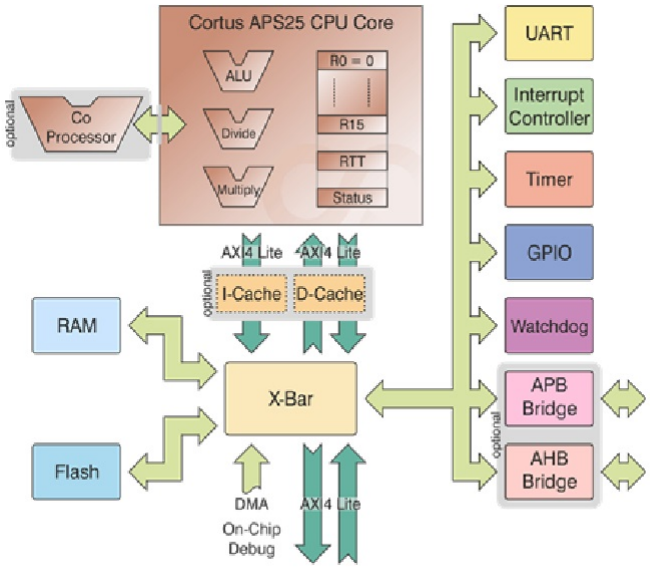


Figure 2: APS25 subsystem architecture

clock frequency. Out-of-order completion enables nearly all instructions to execute in a single cycle, including loads and stores. Interrupts are fully vectored and the architecture ensures a minimum of software overhead in task switches. The processor was designed to execute high level languages such as C. The entire GNU GCC toolsuite has been ported to this architecture.

Several standard peripherals are available. An optional trace buffer is also made available to make debugging rapid and simpler.

The Cortus APS bus is a simple and efficient synchronous bus that interfaces easily to synchronous memories (SRAM). It has a minimal number of signals that simplifies the interconnect reducing logic costs. With a sufficiently high-performance memory subsystem, it can offer zero latency memory accesses, with back-to-back reads and writes. The AXI 4 Lite bus is a high-performance bus that is compatible with other IP and interfaces easily with the APS bus. Efficient bridges between these bus interfaces, and to other popular standards such as AHB-Lite and APB are available.

Table 2 summarizes typical maximum operating frequencies of Cortus processor families. Here, the APS25 processor operates at the highest possible frequency.

Table 2: Maximum frequencies of APS and FPS processors in 90 nm.

Maximum frequency in UMC90			
APS1	307 MHz		
APS3R	312 MHz	APS23	235 MHz
APS3RP	285 MHz	APS23P	217 MHz
APS5	425 MHz	APS25	425 MHz
FPS6	400 MHz	FPS26	392 MHz

Table 3 provides a range of typical power consumption numbers for Cortus cores according to frequency scale.

Table 3: Power consumption per MHz in 90 nm.

Power consumption per frequency scale in UMC90	
Core type	Power per frequency scale (μW / MHz)
APS3R	10.42
APS3RP	11.42
FPS6	37.16
APS23	11.62
FPS5	17.56
FPS23P	12.66

The diversity of Cortus cores in terms of performance and power capabilities makes them attractive for usage in heterogeneous multicore systems, such as those explored in the CONTINUUM project. Typically, a system composed of a mix of such cores can run while its high-performance cores are in deep sleep mode in order to save power (e.g., running a network stack). Whenever an event requiring high-performance processing occurs, the high-performance subsystem is taken out of sleep mode in order to process the data already prepared by the low power companion cores. After all required data get processed, the high-performance cores can go back to sleep mode and the low power companion cores tidy up.

The ARM big.LITTLE technology [22] follows a similar principle by combining low power Cortex-A7 cores with high-performance Cortex-A15 cores so as to enable the adequate core selection depending on the nature of the executed workloads.

2.3 ARM core technologies

The Advanced RISC Machine (ARM) offers a family of Reduced Instruction Set Computing (RISC) architectures for computer processors, configured for various environments. A characteristic feature of ARM processors is their low electric power consumption. Almost all modern mobile phones and personal digital assistants contain ARM CPUs, making them one of the most widely used 32-bit microprocessor family in the world. The ARMv7-A cores, which rely on this 32-bit architecture will be evaluated in Section 3.

The Cortus processor technology introduced in the previous section is comparable to ARM microcontroller class processors, also known as Cortex-M class. Tables 4 and 5 compare both the size (in terms of gates count) and the maximum operating frequency for the two processor technology providers. The Cortus processors consume smaller area while providing higher frequency levels.

Table 4: Number of gates in core design: ARM Cortex-M versus Cortus APS.

Number of gates in ARM and Cortus cores			
Cortex M0	12 kgate	Cortus APS23	9 kgate
Cortex M3	33 kgate	Cortus APS5	17.4 kgate
Cortex M4	50 kgate	Cortus APS23P	15.3 kgate

Finally, Table 6 reports a comparison of both technologies in terms of Dhrystone Million Instruction per Second (DMIPS). The performance obtained with Cortus processor technology is generally higher than that of ARM Cortex-M class.

Table 5: Maximum core frequencies in 90 nm : ARM Cortex-M versus Cortus APS.

Maximum core frequencies			
Cortex M0	180 MHz	Cortus APS23	235 MHz
Cortex M3	180 MHz	Cortus APS5	425 MHz
Cortex M4	204 MHz	Cortus APS23P	217 MHz

Table 6: Performance comparison: APS/FPS versus Cortex-M cores.

DMIPS values			
APS3R	2.76 DMIPS/MHz	Cortex M0	1.27 DMIPS/MHz
APS3RP	2.76 DMIPS/MHz	Cortex M3	1.89 DMIPS/MHz
APS5	2.33 DMIPS/MHz	Cortex M4	1.91 DMIPS/MHz
FPS6	2.33 DMIPS/MHz		
APS23P	2.79 DMIPS/MHz		
APS25	2.52 DMIPS/MHz		

2.4 Summary

This section briefly introduced the Cortus processor families, which are envisioned as major building blocks in the heterogeneous multicore architecture explored by the CONTINUUM project for energy-efficient compute nodes. The massive usage of small embedded cores (such as those from Cortus) as promoted in the project proposal can provide an interesting compromise expected for energy-efficiency and cost-effectiveness. These small embedded cores are highly energy and silicon efficient offering more MIPS/mm2 or MIPS/μW of energy consumed than bigger application cores.

3 Evaluation of a big.LITTLE technology

Among the recent ARM-based technologies, big.LITTLE is certainly a very popular and promising solution that is worth-mentioning in our vision. Indeed, the CONTINUUM project aims at system designs with similar features as ARM big.LITTLE.

3.1 Introduction

We explore the potential of a state-of-the-art ARM-based computer board named Odroid XU3 for building energy-efficient many- and multicore systems. This board integrates the Samsung Exynos 5422 chip relying on ARM big.LITTLE technology [22] that enables to dynamically migrate applications between two different clusters of ARM cores: a low-power cluster composed of four Cortex-A7 cores *versus* a high-performance cluster composed of four Cortex-A15 cores. It also includes a GPU and further peripherals. The migration of applications between the 4-core clusters depends on their workload, i.e. it is steered by performance needs. Our study provides insightful performance and energy results in typical compute-intensive benchmarks.

3.2 Evaluated system setup information

3.2.1 Hardware characteristics

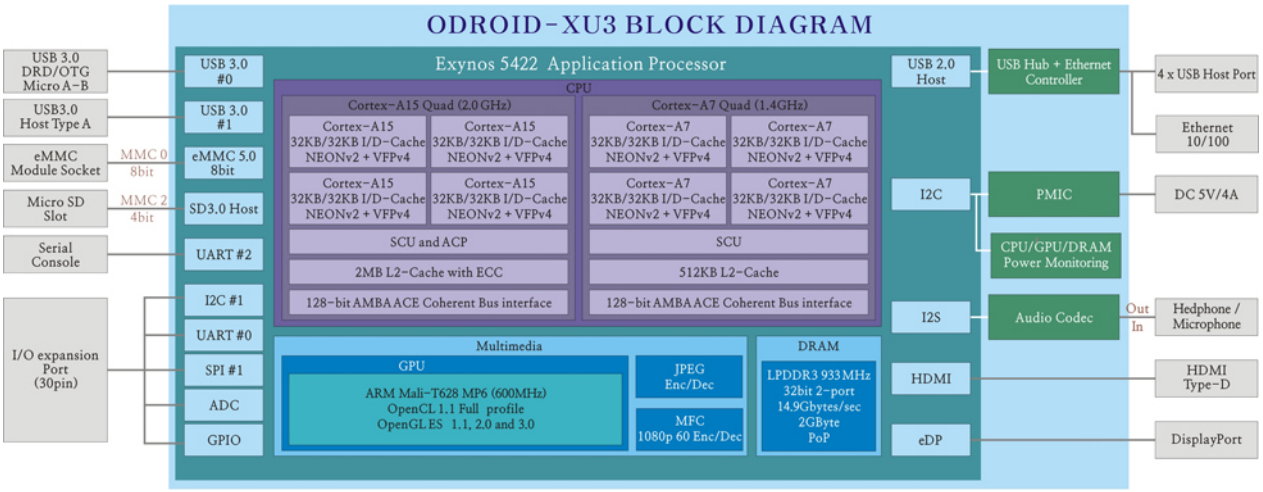


Figure 3: ODROID XU3 block diagram

To explore the capabilities of the Exynos 5422 chip, we consider the Odroid XU3 embedded board, developed by Hardkernel company[2]. This board embeds useful power and thermal sensors that facilitate the evaluation of the energy consumed by its relevant hardware components. Its block diagram is shown in Figure 3. The board is a complete embedded system featuring several components among which:

[2] `http://www.hardkernel.com`.

- Samsung Exynos 5422 chip with big.LITTLE processor, characterized by the following parameters:

Table 7: Exynos 5 Octa (5422) SoC specification.

Parameters		LITTLE	big
Architecture model			
Core type		Cortex-A7 (in-order)	Cortex-A15 (out-of-order)
Number of cores		4	4
Core clocks		200 MHz - 1.4 GHz	200 MHz - 2 GHz
L1	Size	32 kB	32 kB
	Assoc.	2-way	2-way
	Latency	3 cycles	4 cycles
L2	Size	512 kB	2 MB
	Assoc.	8-way	16-way
	Latency	15 cycles	21 cycles

- CCI-400 64-bit interconnect
- PowerVR SGX544MP3 GPU,
- 2 GB LPDDR3 RAM (933 MHz, 14.9 GB/s, 32-bit, 2 channels),
- eMMC 4.5 Flash Storage (64GB),
- Current and voltage sensors to measure power consumed by the two quad-core clusters, RAM memory and GPU.

3.2.2 Software parameters

To run the Odroid board we use the following software:

- Operating system: xUbuntu 13.10[3],
- Compilation: GCC 4.8.1,
- Libraries: OpenMPI 1.6.4 and automatically tuned linear algebra software (ATLAS) 3.10.1-2.

The first benchmark we consider is high-performance Linpack (HPL) [1]. It solves random dense linear systems in double-precision arithmetic (64 bits). The Top500 ranking of the most powerful supercomputers relies on this benchmark. The performance numbers obtained with HPL provide a good correction of theoretical peak performance. In our case, the Odroid board is evaluated according to the following setup: on each quad-core cluster, four MPI tasks (one task per core) will be executed;

[3] `http://www.odroid.in/Ubuntu_XU` – Linux 3.4.67 #5 SMP PREEMPT Sun Nov 24 19:25:46 KST 2013 armv7l armv7l armv7l GNU/Linux

the benchmark data fills around 1.2 Gbits of the LPDDR3 RAM memory; there is no SWAP and the GPU will not be used in all our experiments.

The second benchmark suite is Rodinia [13]. It is composed of applications and kernels of different nature in terms of workload, from domains such as bioinformatics, image processing, data mining, medical imaging and physics simulation. It also includes classical algorithms like LU decomposition and graph traversal. For our experiments, the following setup is considered: for each quad-core cluster, each application and kernel is executed through its OpenMP implementation configured with 4 threads (except for the *kmeans_serial* kernel which is executed with a single thread).

3.3 Energy-efficiency evaluation based on HPL

We evaluate the performance, power and energy-efficiency by considering the entire Odroid board at core peak performance level with HPL.

3.3.1 Performance and energy-efficiency of Odroid-XU3

The peak performance is evaluated in terms of Giga FLoating point Operations Per Second (GFLOPS) for both Cortex-A15 and Cortex-A7 quad-core clusters. The power consumption of the different components is monitored via on-board sensors. Results given in the following rely on an average of 10 iterations of HPL execution. Table 8 shows the HPL score for different cluster frequencies. As expected, at similar frequencies (i.e., 1.4Ghz, 0.8GHz and 0.2GHz) the Cortex-A15 cluster provides a higher performance than the Cortex-A7 cluster. The peak performance of Cortex-A15 cluster at 1.4GHz is around 4.96 GFLOPS, which is around 3 times higher than that of the Cortex-A7 cluster at the same frequency.

	A15				A7		
Freq. (GHz)	2.0	1.4	**0.8**	0.2	1.4	0.8	0.2
HPL score (GFLOPS)	4.7	4.96	**3.42**	0.96	1.68	1.04	0.26
Average Power (W)	12.5	7.5	**4.6**	2.76	3.46	2.58	2.18
EtoS (J)	221.7	127.7	**113.1**	240	172.1	206.4	710
Energy eff. (GFLOPS/W)	0.376	0.662	**0.746**	0.347	0.484	0.404	0.118

Table 8: HPL results for different frequencies of Odroid board.

Now, let us consider the energy-efficiency of the system in terms of GFLOPS per Watt (GFLOPS/W), which is computed from the HPL score, execution time and average power consumption. The corresponding results are given in the last row of Table 8. From the entire board level, the most energy efficient configuration corresponds to the Cortex-A15 cluster running at 800 MHz. Despite the fact that Cortex-A7 core consumes less power than Cortex-A15 core, the extremely compute-intensive feature of the HPL benchmark makes the Cortex-A15 quad-core cluster more energy-efficient than the Cortex-A7 one.

3.3.2 Comparison with other computer systems

Let us consider the most energy-efficient board-level configuration of the Odroid board identified previously, i.e. the Cortex-A15 cluster at 800 MHz. Now, we compare it with other systems running the HPL benchmark [24, 5, 34] in Table 9. In [34], the scalability and energy-efficiency of three multiprocessor-on-chip (MPSoCs) in a cluster are evaluated. These MPSoCs are PandaBoard, Snowball and Tegra. They all contain ARM Cortex-A9 processors. The obtained results show that Snowball is the most energy-efficient while Tegra 2 is the most scalable. In [5], a similar study is reported, which assesses the benefits of ARM core clusters compared to those relying on commodity processors such as x86. Compared to mentioned works using Cortex-A9, our identified configuration is more energy-efficient. This is explained by two reasons: first, the Cortex-A15 processor belongs to the third generation of Cortex-A family, which is more optimized than the second generation to which belongs the Cortex-A9 processor; second, the number of cores available in a system appears proportional to the energy-efficiency of that system.

In Table 9, the Viridis system contains four Cortex-A9 cores while both PandaBoard and Tegra 2 systems contain only two Cortex-A9 cores. The two AMD dual-core systems are less energy-efficient than all mentioned ARM-based systems. The only system that proves better than Odroid is composed of four i7 cores. However, the cost of such a node ($1000 each) is around 5 times higher than the Odroid XU3 board.

	i7 [24]	Atom64 [24]	amdf [24]	viridis[24]	Pandaboard [5]	Tegra 2 [34]	Odroid XU3
CPU	Intel Core i7-3615	Intel Atom N2600	AMD Fusion G-T40N	Cortex-A9	Cortex-A9	Cortex-A9	Cortex-A15
Num. of cores	4(8 threads)	2	4	2	2	2	4
HPL score (GFLOPS)	39.63	0.9575	1.609	3.218	1.601	0.9206	3.42
Energy eff. (MFLOPS/W)	1059	69	85	593	291	161	746

Table 9: Energy efficiency of single system node for HPL benchmark

3.4 Evaluation of the board using Rodinia

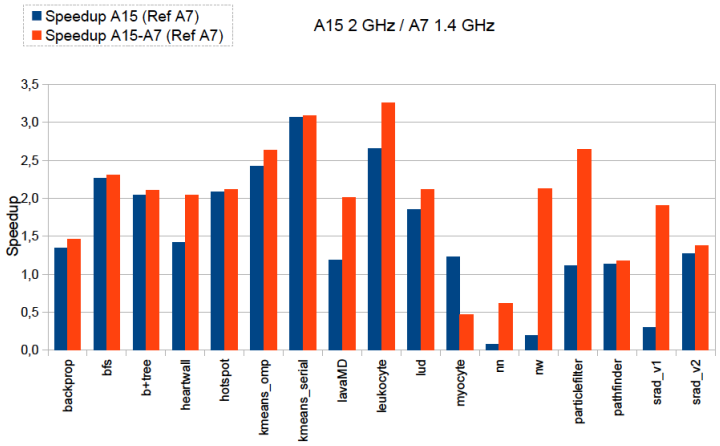
In this section, we evaluate the performance and energy-efficiency of the Odroid board when executing the Rodinia benchmark suite.

3.4.1 Evaluation scenarios

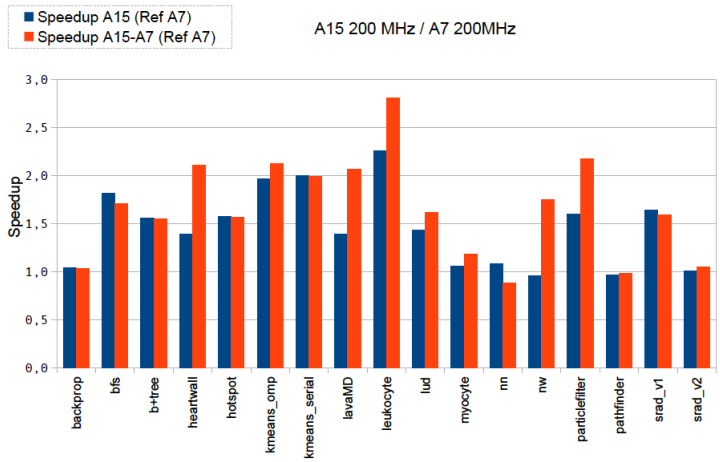
In the considered experiments, three execution configurations are considered: *i) execution only performed on the Cortex-A7 cluster, ii) execution only performed on the Cortex-A15 cluster, and iii) execution performed on both clusters, i.e., HMP mode*. Typically, for applications with low workloads, i.e. which are not performance-demanding, the Cortex-A7 cluster is generally preferable for low power execution. The Cortex-A15 cluster will be preferred for applications with high workloads. In the next paragraphs, for all experiments, the results are normalized regarding the configuration (i).

Figures 4 and 5 show the average speedup of configurations ii) and iii) *versus* configuration i). In the former case, all cores simultaneously operate either at their maximum or minimum frequency levels. In the latter case, cores simultaneously operate at different frequency levels.

While the two configurations always provide a better speedup than the reference configuration, the observed gains vary with the application kernels. The best speedup results are provided in the scenario captured by Figure 5. More generally, the HMP mode appears as the best, except for a few scenarios (e.g., Lud and Myocyte kernels in Figure 5).



(a) At maximum core operating frequencies

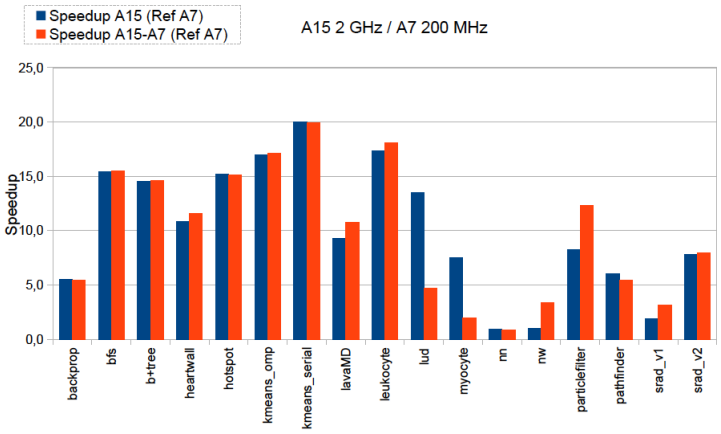


(b) At minimum core operating frequencies

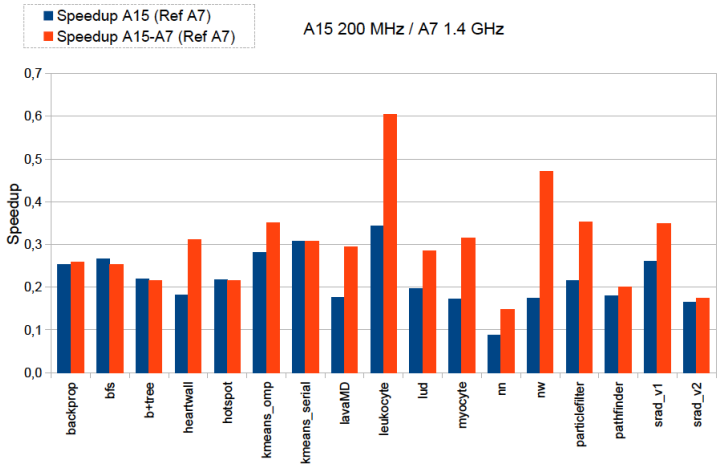
Figure 4: Speedup of A15 cluster and HMP execution modes vs. A7 cluster for Rodinia: all cores operating simultaneously at maximum/minimum frequency levels.

Figures 6, 7 and 8 details the energy consumption for each evaluated Rodinia kernel or application. The energy-to-solution measured when only using the Cortex-A7 cluster is globally less than that obtained with other configurations, i.e., when using only the Cortex-A15 cluster or the HMP mode. Contrarily to HPL, this evaluation shows that for a large part of Rodinia applications and kernels the Cortex-A7 mode appears more energy-efficient at board level.

This suggests that application nature has an impact on the energy consumption induced in the different clusters at board level: HPL permanently exploits the peak performance of available cores during execution while Rodinia applications and kernels, due to their irregular computational nature, imply a load fluctuation on cores.



(a) At maximum A15 and minimum A7 core operating frequencies



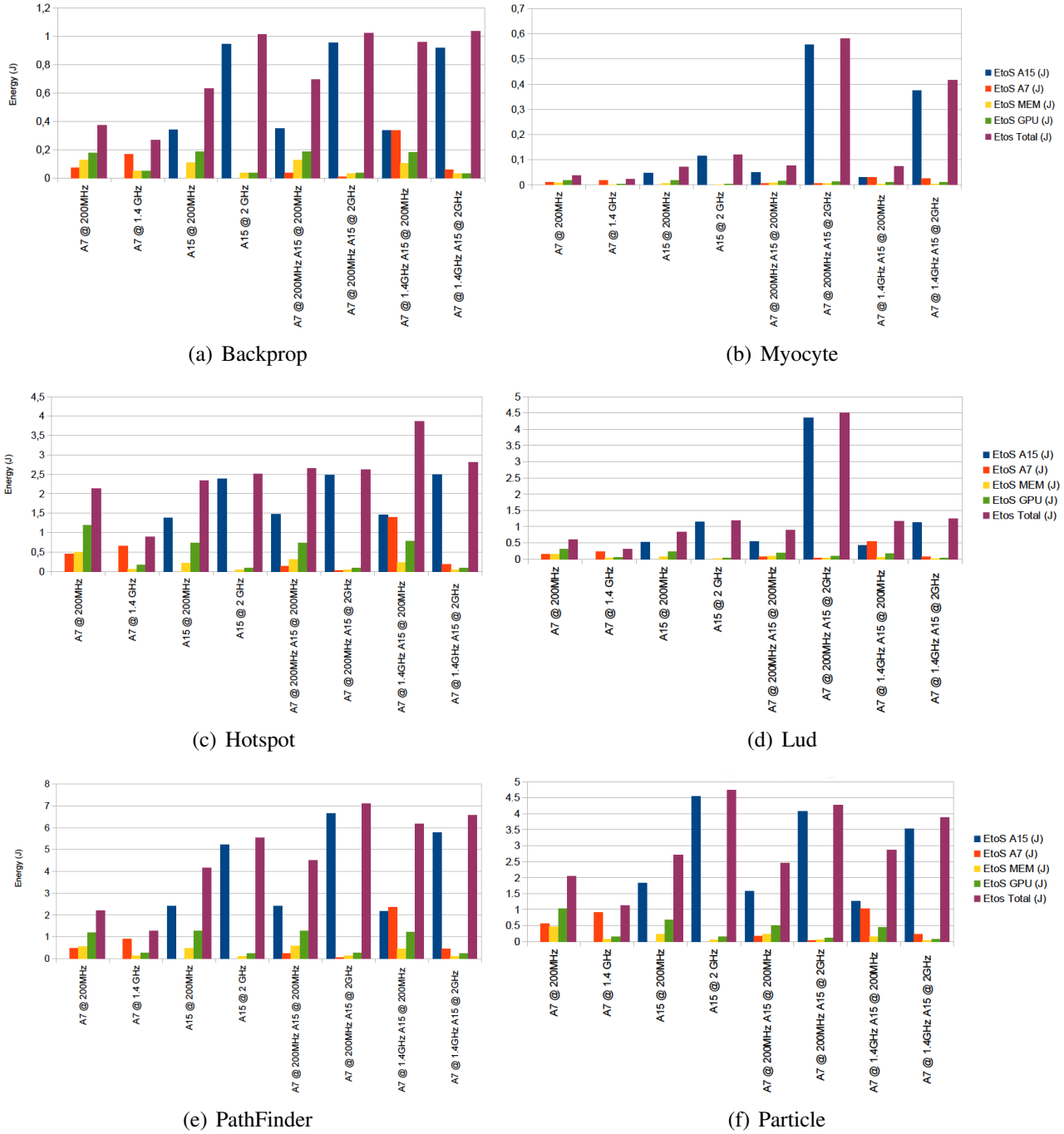
(b) At minimum A15 and maximum A7 core operating frequencies

Figure 5: Speedup of A15 cluster and HMP execution modes vs. A7 cluster for Rodinia: all cores operating simultaneously at different frequency levels.

3.5 Summary and remarks

This chapter presented an evaluation of opportunities and limitations of state-of-the-art and reasonable cost embedded multicore computer systems, integrating ARM big.LITTLE technology for energy-efficient mini-clusters. It provided insightful performance and energy-efficiency results based on two compute-intensive benchmarks, high-performance Linpack and Rodinia. The performance scalability of a mini-cluster composed of these boards has been analyzed.

These results showed that the big.LITTLE architecture of the considered Odroid board calls for adequate migration policies, which are capable of adequately addressing heterogeneous application workloads. A characterization of applications/tasks/threads is required, e.g., regular vs. irregular, computation-intensive vs. memory-intensive. This information can be used either offline or online together with data monitoring (power and energy consumption, CPU workload, etc.) to exploit as much as possible the energy-efficiency of clusters.

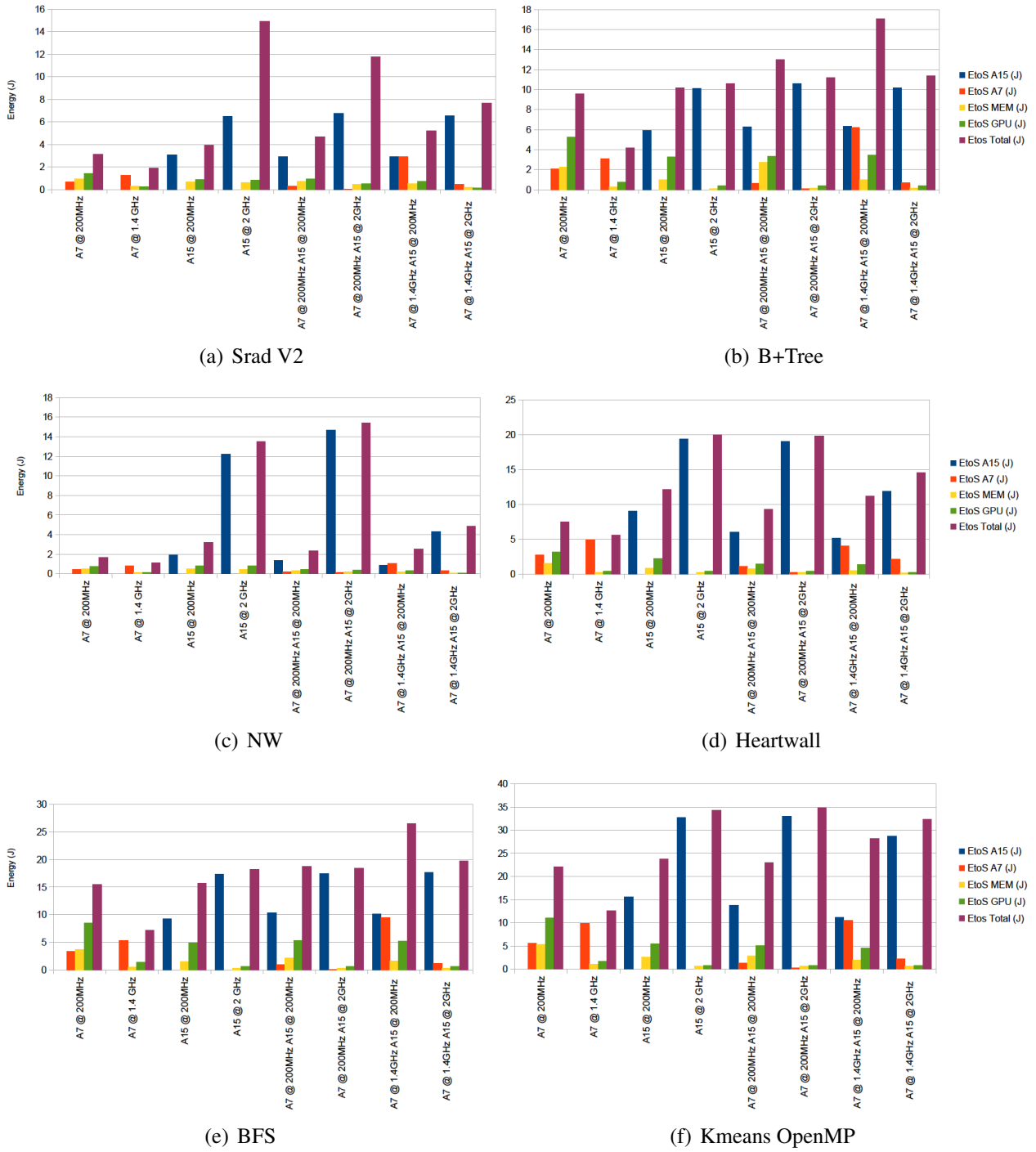


(a) Backprop (b) Myocyte

(c) Hotspot (d) Lud

(e) PathFinder (f) Particle

Figure 6: Energy-to-Solution of Rodinia kernels according different clustering modes and operating frequencies.

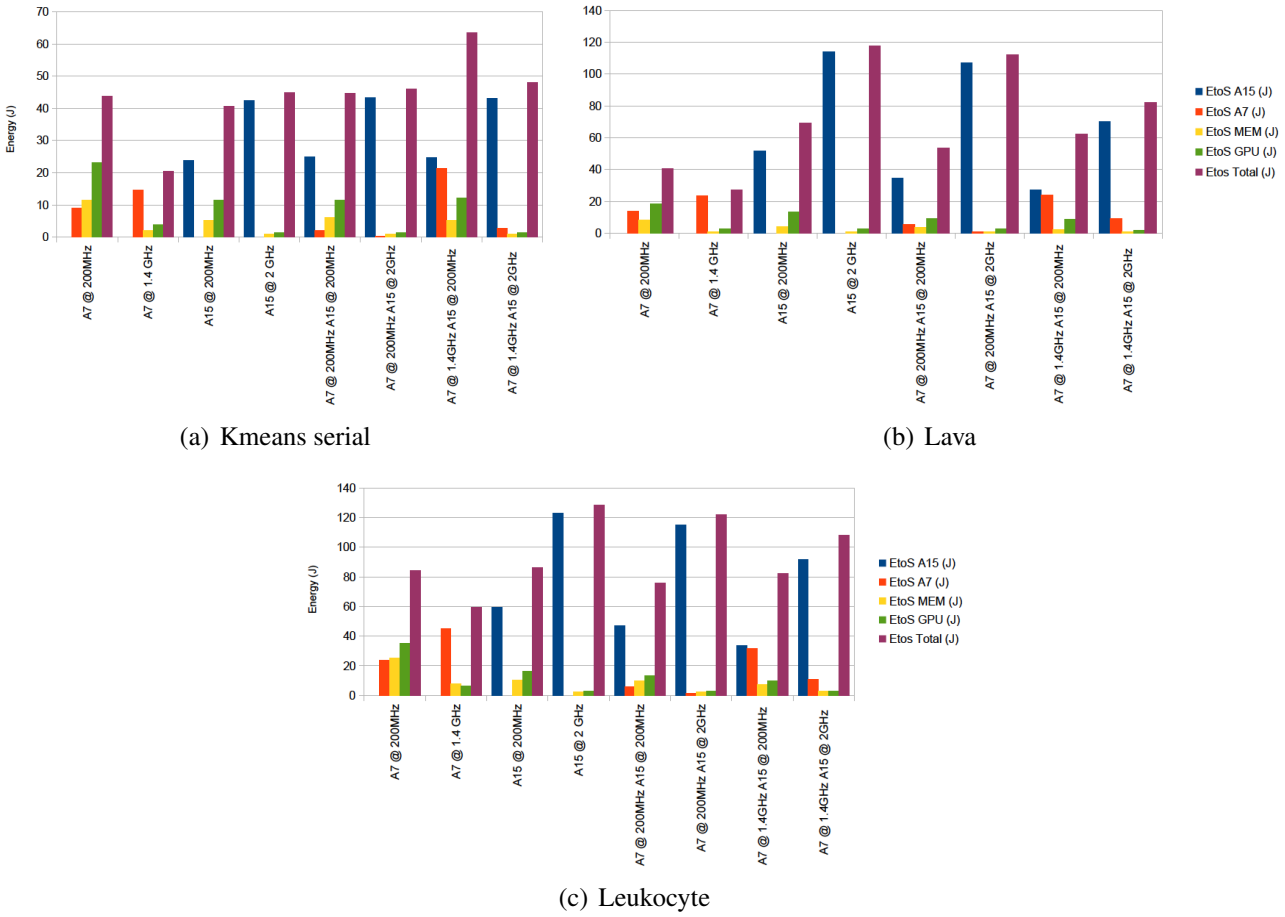


(a) Srad V2 (b) B+Tree

(c) NW (d) Heartwall

(e) BFS (f) Kmeans OpenMP

Figure 7: Energy-to-Solution of Rodinia kernels according different clustering modes and operating frequencies.



(a) Kmeans serial

(b) Lava

(c) Leukocyte

Figure 8: Energy-to-Solution of Rodinia kernels according different clustering modes and operating frequencies.

4 Further multicore architectures

Beyond the big.LITTLE technology evaluated in the previous section, there are further manycore architectures that can deserve attention. These architectures have different characteristics that could be considered in the design of the compute node architecture investigated in the CONTINUUM project. Thanks to their high number of cores, they represent interesting compute accelerators adopted in a number of execution infrastructures. In the next sections, we survey some of these architectures.

4.1 Graphical Processing Units of Nvidia

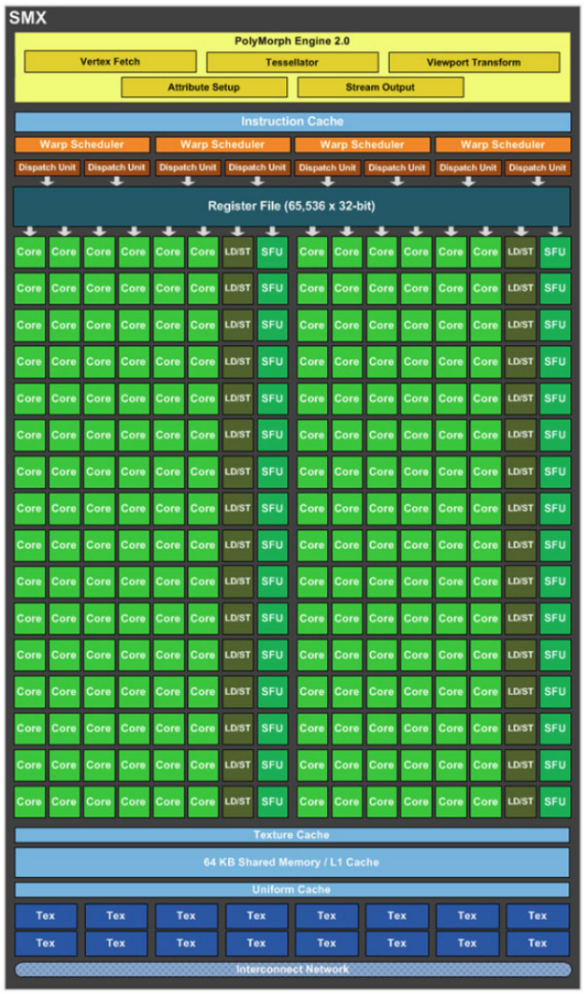


Figure 9: Kepler SMX architecture (source: `http://www.bit-tech.net`).

Graphical Processing Units (GPUs) such as Kepler[4] can have upto 15 streaming multiprocessors (SMX), each able to handle 192 single-precision cores and 64 double-precision units. Figure 9 illustrates a massively parallel architecture of an SMX. Each core has fully pipelined floating-point

[4] `http://www.nvidia.com/object/nvidia-kepler.html`

and integer arithmetic logic units. Threads are scheduled in SMX by groups of 32 parallel lightweight threads called warps. All these features make GPUs powerful compute accelerators able to provide high performance per watt, especially for regular data-parallel computations as found in graphics and scientific computing applications. Their main limitation comes when dealing with irregular applications, e.g. with conditional branches. In addition, when using an SMX for all its corresponding cores become active, thus energy-consuming. This means that to have an energy-efficient execution on the SMX, all its cores must be used.

4.2 Intel Many Integrated Core Architecture

Many Integrated Core Architecture (MIC)[5] [18] is the architecture adopted by Intel Xeon Phi co-processors, used as compute accelerators in the second ranked world's fastest[6] supercomputer (Thiane-2) in 2014. It is composed of 61 cores interconnected by a bi-directional ring network (see Figure 10). Intel Xeon Phi co-processors provide power gating of cores, L2 cache and memory controllers for leakage power reduction. Compared to GPUs for which performance optimization requires to run lightweight threads maximizing parallelism, the MIC architecture maximizes core performance through coarse-grained parallelism. However, a study indicated that the ring network and the ECC memory overhead are performance bottlenecks in MIC architecture, showing poor scalability beyond 32 cores [25].

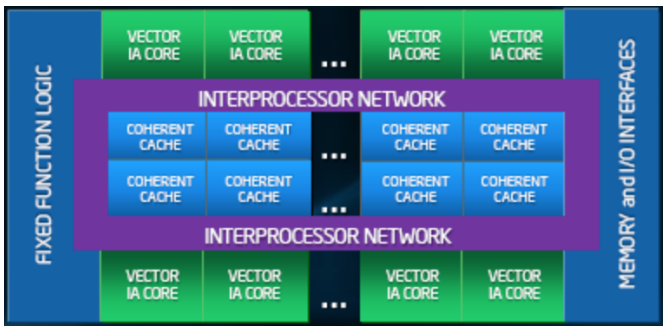


Figure 10: Intel MIC architecture (source: `http://wiki.expertiza.ncsu.edu`).

4.3 Tile-Gx of Tilera

TILE-Gx[7] architecture is another multicore processor, which comprises up to 72 cores interconnected by a 2D mesh NoC using wormhole routing packets. Figure 11 depicts a Tile-Gx architecture composed of 36 cores. From a global point of view, TILE-Gx processor in composed of a two-dimensional array

[5] `http://www.intel.com/content/www/us/en/architecture-and-technology/many-integrated-core/intel-many-integrated-core-architecture.html?_ga=1.31218297.751580311.1426595792`

[6] `https://www.top500.org/lists/2016/06`

[7] `http://www.mellanox.com/repository/solutions/tile-scm/docs/UG130-ArchOverview-TILE-Gx.pdf`

of identical so-called "tiles". Each tile consists of a core, 64KB L1 cache, 256 L2 cache and a non-blocking switch connecting tiles to the NoC. A shared address space with cache coherence maintained by hardware is considered. A study [32] showed that such a processor has a well-balanced architecture for achieving an excellent ratio of performance per watt. This makes TILE-Gx a good candidate for building energy-efficient compute accelerators. But, the weak point of its architectures mainly lies in the lack of floating point units (FPUs) required for compute-intensive applications.

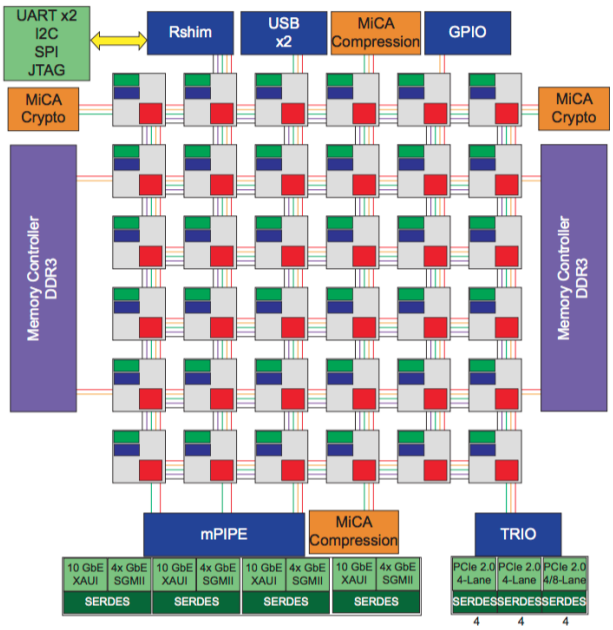


Figure 11: Tile-Gx36 block diagram (source `http://www.mellanox.com/repository/solutions/tile-scm/docs/UG130-ArchOverview-TILE-Gx.pdf`).

4.4 Multi-Purpose Processor Array of Kalray

Multi-Purpose Processor Array (MPPA)[8] [14] is a manycore architecture that integrates 256 cores, where cores are distributed across 16 compute clusters (see Figure 12). Each compute cluster has a private local memory and cache coherence is enforced by software. Communication and synchronization between compute clusters are ensured by a proprietary NoC using a 2D torus topology with a wormhole routing. A recent study [15] compares three accelerators: (i) MPPA, Intel i7-3820 quad-core, and Nvidia Tesla C2075 GPU. It showed that although MPPA has a lower peak performance than Intel i7-3820 and GPU for double precision floating-point arithmetic, for irregular application it outperforms Intel i7-3820 by a factor of 2.4 and only twice worse than the GPU. When comparing energy consumption, MPPA is over 20 and 6 times more efficient than Intel i7-3820 and GPU respectively. Indeed in a study [12] authors showed that a single thread execution on a cluster dissipates 3.73watts while 16 threads require 3.98watts. This suggests that a partial exploitation of the 16 cores available in a cluster leads to low energy-efficiency as with GPUs.

[8] `http://www.kalrayinc.com/kalray/products/#processors`

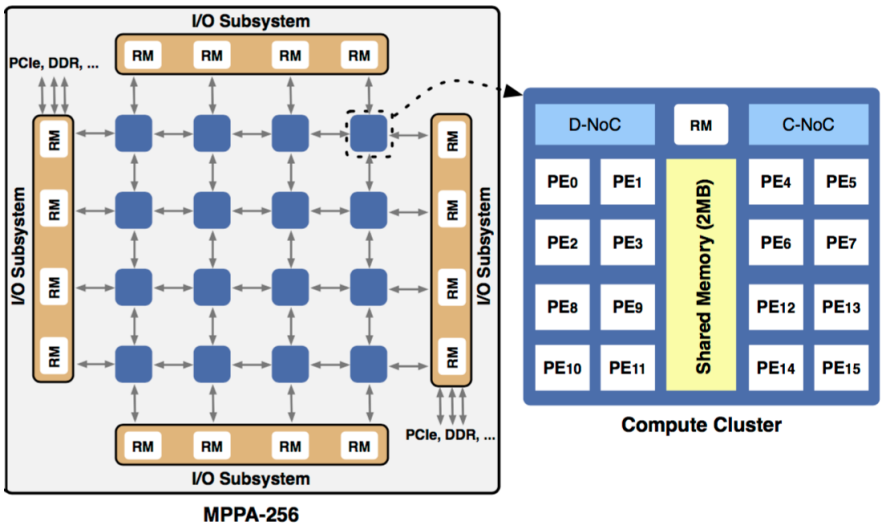


Figure 12: MPPA - 256 block diagram (source: [12]).

4.5 Tera-Scale ARchitecture

Tera-Scale ARchitecture (TSAR) [23, 20] is a scalable general-purpose cache-coherent globally asynchronous locally synchronous (GALS) multicore architecture. It consists of a set of clusters (see Figure 13) interconnected by a 2D mesh NoC. Each cluster is composed of 32 bits RISC cores without superscalar features. TSAR architecture aims to solve two major technical issues: i) scalability by targeting up to 4096 cores and ii) power consumption by using small cores to obtain the best MIPS/microwatt ratio. TSAR architecture physically implements MMU in the L1 cache controller. This creates an overhead in terms of silicon area and increased latency communication to maintain cache coherency. Therefore, network latency of distributed MMU may be very sensitive to the growth of the system.

A recent multicore architecture proposal [21] adopting distributed-memory design, shows promising performance, area and energy consumption improvements. This is enabled by the scalability of the architecture.

4.6 Summary

This section presented a number of existing compute accelerator architectures from which some interesting features could be borrowed for the compute node architecture explored in CONTINUUM. For instance, the cluster-based design of the TSAR architecture with low power cores certainly deserves to be considered as it shares a number of characteristics in the foreseen compute node architecture. However, an important innovation expected in CONTINUUM is the integration of emerging non-volatile memory technologies in the memory hierarchy, while exploiting core heterogeneity so as to achieve the best compromise in terms of performance and power consumption.

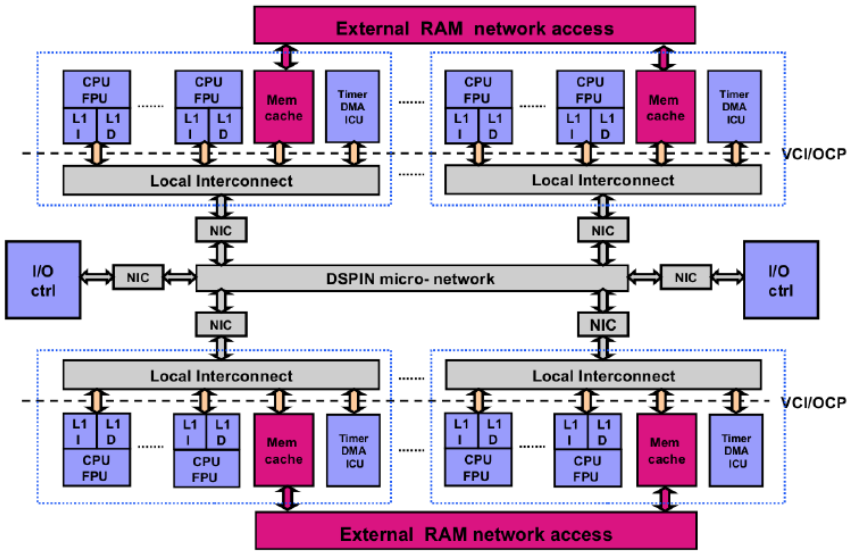


Figure 13: TSAR architecture (source [23]).

5 Conclusions and future work

In this deliverable, we presented a number of candidate core technologies for the compute node architecture studied in the CONTINUUM project. The core technologies from the Cortus partner are central building blocks in the definition of the expected architecture. Indeed, they appear as good candidates for offering the required capabilities in terms of performance and power consumption trade-off in order to conveniently reach energy-efficiency. The foreseen design solution shares several points with the ARM big.LITTLE technology, which consists of heterogeneous cores that can be selected according to the performance and power demand of executed workloads, for energy-efficiency purposes. The energy-efficiency of a system-on-chip integrating this technology has been evaluated in this deliverable. On the other hand, some complementary manycore architectures have been surveyed, as a possible inspiration basis for the compute node targeted in our project.

From this preliminary study on relevant candidate technologies about cores, we can properly now address the design of our target compute node based on all interesting features identified from the state-of-the-art. In particular:

- as big.LITTLE design paradigm shows several benefits in terms of performance and power consumption trade-off, we would like to focus on its heterogeneous feature by considering the ultra-compact core technology from Cortus, which are more energy-efficient than traditional big.LITTLE configurations;

- further interesting design paradigms identified from the reviewed literature, e.g., mesh interconnects and cluster-based partitioning [23, 21], deserve high attention as part of the design options to be considered in the next steps of the project;

- emerging non-volatile memories [43], such as magnetic memories integrated in last-level caches [41, 40, 36, 42, 17], are other design ingredients to take into account for an aggressive energy reduction.

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