Méthode Itérative pour l'Amélioration de la Prédiction des Performances des Circuits Intégrés

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Iterative Method for Performance Prediction Improvement of Integrated Circuits

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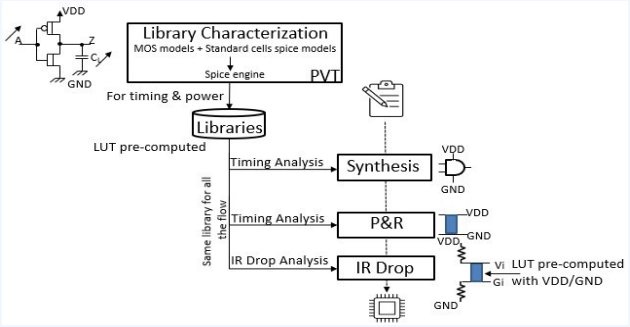
Context

- Design flow based on the use of **pre-characterized** libraries
- **Operation** of the circuit checked at each stage
- Calculation model more complex with each step
- Use of libraries **do not** consider power supply contexts.

Model complexity → Inacurracy in the use of libraries



The different stages of the actual design flow

Problem

Innacuracy in actual design flow

Poor estimation of circuit performances

Design flow

Resistivity of the power grid

Voltage drop

Timing errors

Pessimistic solution

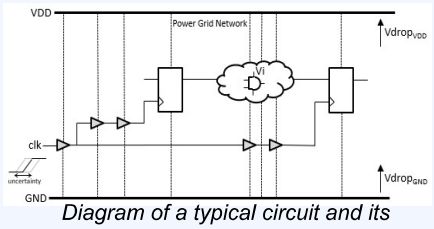


Diagram of a typical circuit and its power supply grid

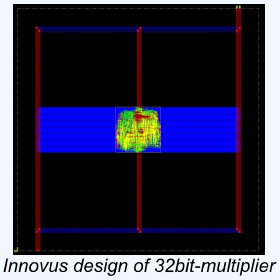
Pessimistic solution:
If IR Drop value > 10% of the external power supply voltage

Iterative approach

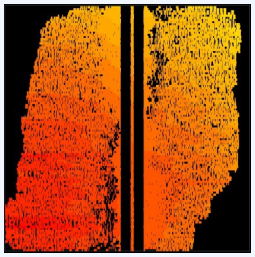
a) Initialization

- Circuit designed in the usual way
- Libraries power supply values cover 100 mV of power supply with a step of 2.5mV:

Vi_{min} , Vi_{min}+2.5mv , ... , V_{DD}



Innovus design of 32bit-multiplier



IR Drop analysis

b) IR Drop analysis

IR Drop analysis performed as usual

Vi calculated for each standard-cell

Tcl command file

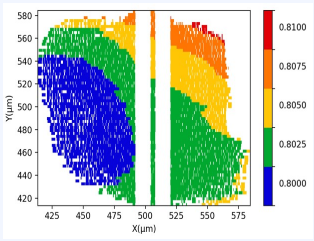
c) Change Cell

Tcl command file example:

```
EcoChangeCell -cell NAND2_0.802.5 -inst g1516
```

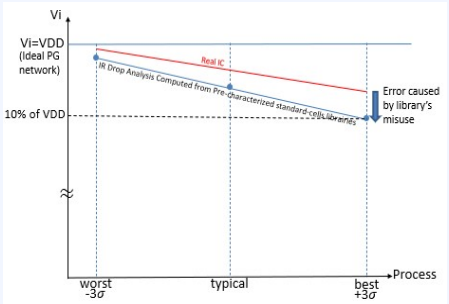
New rounded power suplly value — Instance name

For each standard-cell



Supply voltage of the library assigned to each standard cell for fist iteration

The misuse of libraries



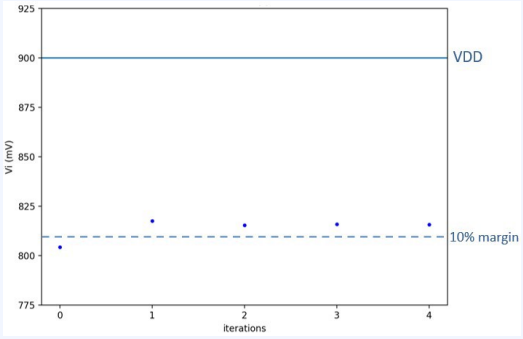
Impact of the misuse of libraries on IR Drop calculation

- Libraries are made **out of any context**
- **Performance & consumptions** described in libraries can't be reached

Misuse of libraries

Over-estimation of the IR Drop

Results

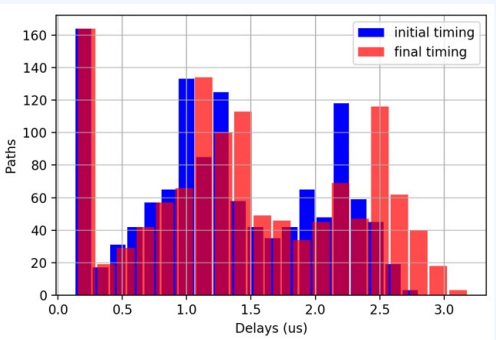


Evolution of Vi with iteration for one standard-cell in the middle of the circuit

- Only **3 iterations** to stabilize Vi to the nearest mV
- Final value of Vi for all standard-cell's libraries
- Allows to perform **IR-aware** timing analysis

Conclusion & Perspectives

- IR Drop values decreased to 9.3% of V_{DD}. With actual design flow the operation of the circuit was not guaranteed. With the iterative method, the value of IR Drop is correct.
- IR-aware delays are 12% slower. But the gain in precision could allow to estimate real delay margin and use it to optimize the design.



Final IR-aware delays obained by iterative method compared to initial delays