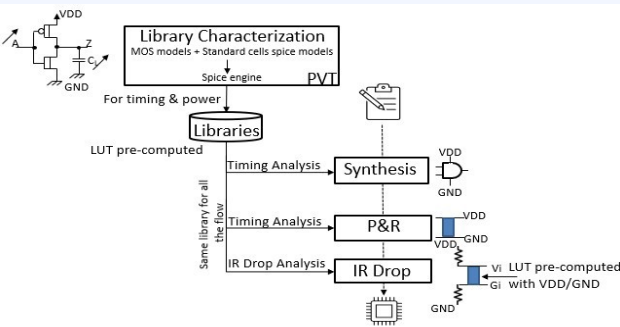


# Iterative Method for Performance Prediction Improvement of Integrated Circuits

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## Context

- Design flow based on the use of **pre-characterized** libraries
- **Operation** of the circuit checked at each stage
- Calculation model more complex with each step
- Use of libraries **do not** consider power supply contexts.

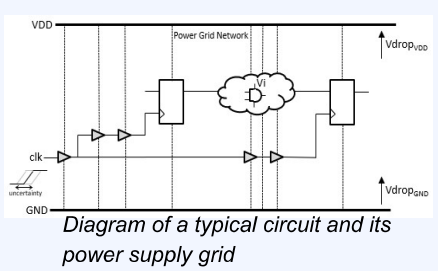
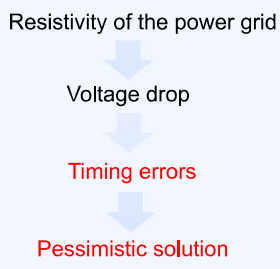


The different stages of the actual design flow

## Problem

**Inaccuracy** in actual design flow  
 ↓  
**Poor estimation** of circuit performances

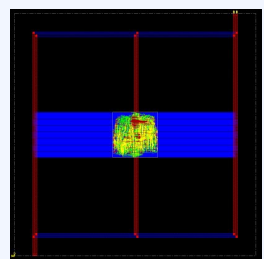
## Design flow



## Iterative approach

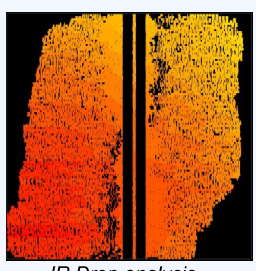
### a) Initialization

- Circuit designed in the usual way
- Libraries power supply values cover 100 mV of power supply with a step of 2.5mV:  
 $V_{min}, V_{min}+2.5mV, \dots, V_{DD}$



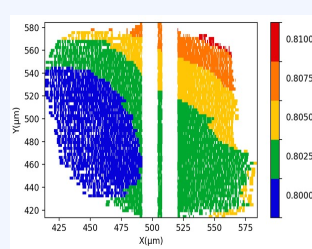
### b) IR Drop analysis

IR Drop analysis performed as usual  
 ↓  
 $V_i$  calculated for each standard-cell  
 ↓  
 Tcl command file



### c) Change Cell

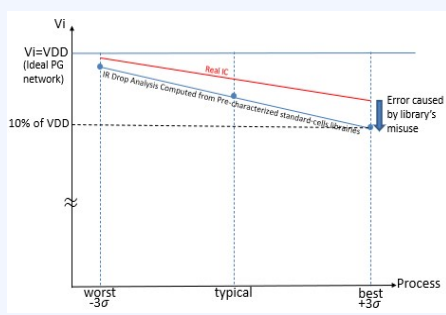
Tcl command file example:  
`EcoChangeCell -cell NAND2_0.802.5 -inst g1516`  
 New rounded power supply value Instance name  
 For each standard-cell



## The misuse of libraries

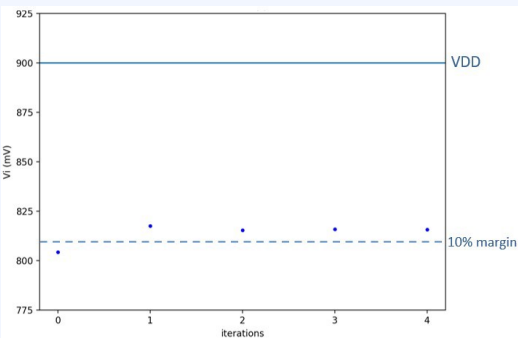
• Libraries are made **out of any context**

• **Performance & consumptions** described in libraries can't be reached



**Pessimistic solution:**  
 If IR Drop value > 10% of the external power supply voltage

## Results



- Only **3 iterations** to stabilize  $V_i$  to the nearest mV
- Final value of  $V_i$  for all standard-cell's libraries
- Allows to perform **IR-aware** timing analysis

## Conclusion & Perspectives

- IR Drop values decreased to 9.3% of  $V_{DD}$ . With actual design flow the operation of the circuit was not guaranteed. With the iterative method, the value of IR Drop is correct.
- IR-aware delays are 12% slower. But the gain in precision could allow to estimate real delay margin and use it to optimize the design.

