

Stuck and Weakened Bits in SDRAM from a Heavy-Ion Microbeam

Daniel Söderström, Lucas Matana Luza, Alexandre Bosser, Thierry Gil, Kay-Obbe Voss, Heikki Kettunen, Arto Javanainen, Luigi Dilillo

▶ **To cite this version:**

Daniel Söderström, Lucas Matana Luza, Alexandre Bosser, Thierry Gil, Kay-Obbe Voss, et al.. Stuck and Weakened Bits in SDRAM from a Heavy-Ion Microbeam. RADECS 2019 - 30th European Conference on Radiation and Its Effects on Components and Systems, Sep 2019, Montpellier, France. lirmm-03359010

HAL Id: lirmm-03359010

https://hal-lirmm.ccsd.cnrs.fr/lirmm-03359010

Submitted on 29 Sep 2021

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

This is a self-archived version of an original article.
This reprint may differ from the original in pagination and typographic detail.

Title: Stuck and Weakened Bits in SDRAM from a Heavy-Ion Microbeam

Author(s): Daniel Söderström, Lucas Matana Luza, Alexandre Bosser, Thierry Gil, Kay-Obbe Voss, Heikki Kettunen, Arto Javanainen and Luigi Dilillo

DOI:

Published:

Document version: Pre-print version (Final draft)

Please cite the original version:

This material is protected by copyright and other intellectual property rights, and duplication or sale of all or part of any of the repository collections is not permitted, except that material may be duplicated by you for your research use or educational purposes in electronic or print form. You must obtain permission for any other use. Electronic or print copies may not be offered, whether for sale or otherwise to anyone who is not an authorised user.

Stuck and Weakened Bits in SDRAM from a Heavy-Ion Microbeam

Daniel Söderström, Lucas Matana Luza, Alexandre Bosser, Thierry Gil, Kay-Obbe Voss, Heikki Kettunen, Arto Javanainen and Luigi Dilillo

Abstract

Stuck and weakened bits in the ISSI 512 Mb SDRAM was investigated in irradiation experiments with a heavy ion microbeam in the GSI facility. Delidded memories were tested in gold and calcium ion beams at 4.8 MeV/u, and stuck bits in the memory from the irradiation were investigated. To study weakened but not fully stuck bits after irradiation, parameters such as the refresh frequency of the memories was varied. The effect on the number of stuck bits from reading and writing the memory was studied, as well as the effect from waiting a time span between writing and reading the memory. These parameters were found to matter in the observed number of errors in the memory. Data on the findings from the microbeam irradiation from tests with different test modes are presented in this paper regarding suck bits and bit upsets. The test modes include dynamic March test and data retention tests with only refresh operations during irradiation.

Index Terms

Microbeam, radiation effects, SDRAM, stuck bits, weak bits.

I. Introduction

THE phenomenon of stuck bits in Dynamic Random Access Memories (DRAMs) has been studied for many years [1]. Stuck bits have been suggested to originate from microdose effects [2] or from bulk damage [3], [4], with specific discussion of damage to the depletion region of the access transistor as possible cause [4]–[6].

A stuck bit in a DRAM is a bit that is stuck to either the value '0' or '1', so that it always gives the same value when read, no matter the value that was written in the cell. The value that the cell will be stuck to is the value which corresponds to the state in which the cell storage capacitor is discharged. In this work the concept of weakened bits is also discussed. Weak bits are here defined as bits which upon reading might return the correct value which was written to it (both '0' and '1') in some conditions, but in other conditions might appear as stuck.

Intermittently stuck bits have been studied in e.g. [5]–[7]. These are bits which upon consecutive writes and reads in the same conditions might return the correct value which was written to it, or might be stuck to one certain value. These bits stick and unstick sporadically over time.

The investigated memory in this study was the ISSI 512 Mb Synchronous DRAM (SDRAM). It was subject to irradiation at the GSI Helmholtzzentrum für Schwerionenforschung (GSI) facility in Darmstadt, Germany, with a micrometer ion beam with two different ions: gold (Au) and Calcium (Ca). The microbeam allowed to choose specific regions of the die to irradiate. Stuck and upset bits were caused by the irradiation. The weakened cells of the memory were analysed after the ion exposure.

II. Tested Components

Table I shows the different memory specimen that were tested. All models are ISSI 512 Mb Single Data Rate (SDR) SDRAM IS42S16320F-7TL. The memory bits are structured in 16,777,216 32-bit words divided on 4 memory banks, and operates at a frequency up to 143 MHz. The devices operate with a 3.3 V bias and were packaged in 54-pin TSOP-II packages.

The packages of the irradiated devices were opened via chemical etching laying the die bare for the irradiation. The components listed in Table I came from the same production lot and were purchased together. A photograph of an opened device with the zones that were irradiated (one at a time) during the experiments marked on it can be seen in Fig 1. The sizes of the irradiation zones span from $50 \cdot 55$ µm^2 to $550 \cdot 460$ µm^2.

D. Söderström, H. Kettunen and A. Javanainen are with the Department of Physics, University of Jyväskylä, Jyväskylä, Finland.
A. Bosser is with the Department of Electronics and Engineering, School of Electrical Engineering, Aalto University, Espoo, Finland.
T. Gil, L. Dilillo and L. M. Luza are with Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier (LIRMM), Montpellier, France.
K.-O. Voss is with GSI Helmholtzzentrum für Schwerionenforschung, Darmstadt, Germany.
A. Javanainen is also with the Electrical Engineering and Computer Science Department, Vanderbilt University, Nashville, TN 37235 USA.
Contact: daniel.p.soderstrom@jyu.fi.

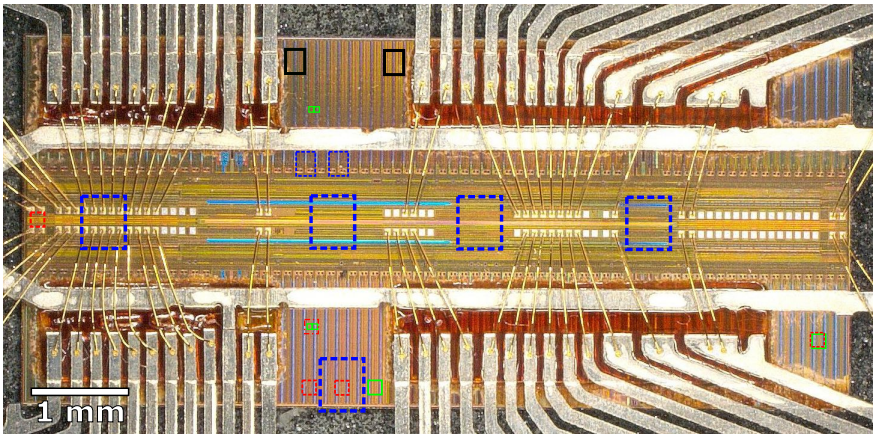


Fig. 1. ISSI 512 Mb SDRAM with opened package. The regions marked in green were irradiated on memory DRA6, the ones marked in red on DRA4, the ones in blue on DRA7 with Au and the ones in black on DRA7 with Ca ions. Zones drawn with solid line were irradiated during retention mode testing, dashed line with modified March C-, and dash-dot line during dynamic stress test (see Section III).

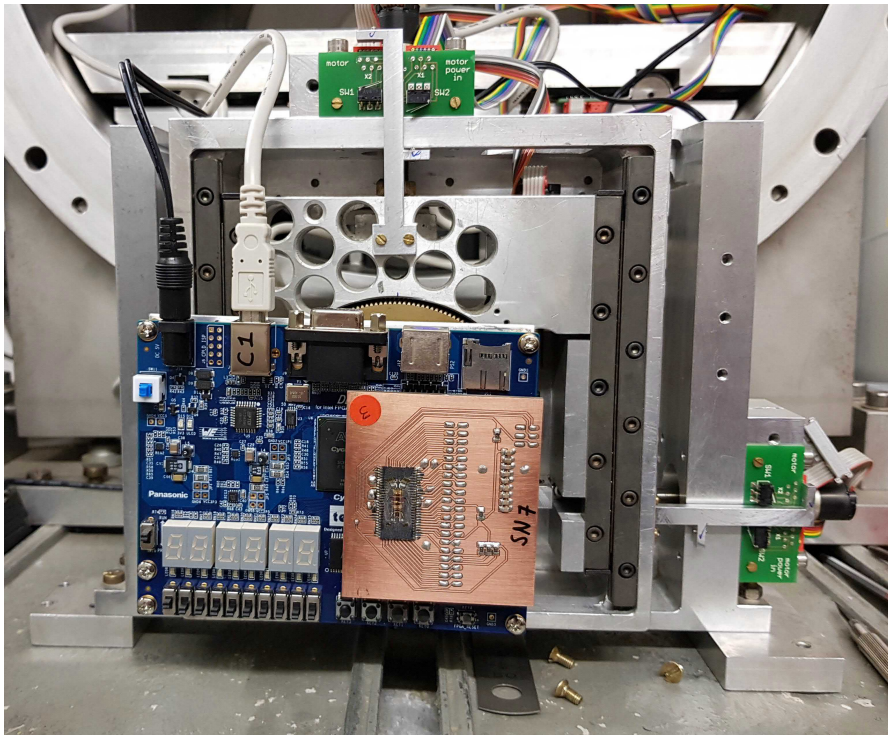


Fig. 2. DUT with daughter and controlling board by the vacuum chamber at the GSI microbeam facility.

III. Experimental set-up and procedure

The tested memories were mounted on separate daughter boards, whith a Terasic DE0-CV FPGA development board used as test controller. The daughter board with the DUT was connected through GPIO pins on the controlling board. Fig 2 shows the mounted test set-up by the test chamber at GSI.

The memory was operated at frequencies (F_{op}) 50 - 100 MHz. The nominal frequency of the memory (143 MHz) could not be reached without issues when using the memory on the daughter board, due to the length of the signal traces on the boards between the FPGA on the control board and DUT.

The refresh frequency F_r of the memory was nominally 128 kHz, so that the data stored in the memory cells was refreshed every 7.8 µs. This nominal frequency was used throughout the tests and analysis in general. The refresh frequency $F_{r,min}$ which was the lowest frequency where all the bits in the memory still managed to retain the data before irradiation was also used during the tests. Values of $F_{r,min}$ is given in Table I for the opened memory devices.

Different test modes were used during the irradiations, with both retention mode and dynamic mode tests as shown

TABLE I
SUMMARY OF SPECIMEN AND IONS USED FOR EACH IN THE EXPERIMENT. VALUES OF THE LOWEST REFRESH FREQUENCY WHERE THE MEMORY BITS RETAINED ALL DATA WRITTEN TO IT ($F_{r,min}$) IS PRESENTED, AND THE OPERATIONAL MODE DURING IRRADIATION.

ID	Ion	$F_{r,min}$ (Hz)	Mode
DRA4	Au	2000	Dynamic
DRA6	Au	2800	Retention
DRA7	Au, Ca	2500	Au: Dynamic Ca: Retention

TABLE II
ION DATA FROM THE TEST CAMPAIGNS.

Ion	Energy (MeV/u)	Energy (MeV)	LET (MeV/(mg/cm^2))
^{197}Au	4.8	945.6	94
^{48}Ca	4.8	230.4	16

in Table I. The retention tests were done writing a pattern of all '1' or all '0' to the memory before irradiation, and then reading the data back after the run.

Dynamic tests were done with either a modified March C- test or dynamic stress test, with read and write operations during irradiation. In the modified March C- test [8] data was written to and read from the memory so that the pattern was alternately all '0' and all '1', and the memory was read (*r*) and written (*w*) with alternately increasing (↑) and decreasing (↓) address access order, see (1). The modification from a normal March C- test compared to what was done here was that the first $\uparrow (w0)$ operation only was performed the first cycle. This was done to eliminate a stand alone write March element, which is useful for cell initialization, but for the following cycles it generates masking effects since only test elements with read operations allow error detection. During consecutive iterations of the test, the operation $\uparrow (r0, w1)$ followed immediately after the test element $\uparrow (r0)$.

Similarly the dynamic stress test schema [8] can be seen in (2), where the first test cycle starts with a $\uparrow (w1)$ operation which is excluded in the following cycles. Here all the operations listed in one row in (2) are performed at one address location at a time, before stepping up or down to the following address location.

$$\begin{aligned} &\uparrow (w0); \{\uparrow (r0, w1); \uparrow (r1, w0); \\ &\downarrow (r0, w1); \downarrow (r1, w0); \uparrow (r0)\} \end{aligned} \tag{1}$$

$$\begin{aligned} \uparrow (w1); \{&\uparrow (r1, w0, r0, r0, r0, r0, r0); \\ &\uparrow (r0, w1, r1, r1, r1, r1, r1); \\ &\uparrow (r1, w0, r0, r0, r0, r0, r0); \\ &\downarrow (r0, w1, r1, r1, r1, r1, r1); \\ &\downarrow (r1, w0, r0, r0, r0, r0, r0); \\ &\uparrow (r0, w1, r1, r1, r1, r1, r1); \} \end{aligned} \tag{2}$$

After irradiation was performed during retention mode testing or dynamic testing, the memory was checked for stuck bits. This was done by writing the memory with first all '0', waiting 60 s, then reading the memory, and then repeated for the pattern all '1'.

IV. TEST FACILITY

The irradiation of the memories was done with accelerated ions from the linear accelerator UNILAC at GSI. The energy per nucleon, total energy, and surface Linear Energy Transfer (LET) of the ions used during the test campaigns can be seen in Table II.

The test board was mounted on a fixture, which was placed inside a vacuum chamber so that the DUT was positioned by the end of the beam line. The user can then determine a zone to irradiate on the DUT (a rectangle with sides up to around 500 µm), as well as the number of ions to send to each point within the chosen zone. The DUT fixture could then be translated vertically and horizontally, as well as be rotated around a central axis, to chose a position for the next irradiation window. The beam spot size was about 0.5 µm^2.

For these tests, the beam was continually scanned over the chosen irradiation zone by magnets, while ions were emitted from the beam line until a pre-set number of ion hits was reached. This created a semi-homogeneous hit pattern of ions within the irradiated area of the memory die (random hits along raster scan lines).

TABLE III
SUMMARY OF THE TEST RESULTS FOR THE DIFFERENT MEMORIES AND TEST MODES WITH NOMINAL OPERATIONAL AND REFRESH FREQUENCIES.

Memory	Mode	LET (MeV/(mg/cm^2))	Ion count	Bit upsets	Stuck bits	Equivalent Fluence (ions/cm^2)
DRA6	Retention	94	6930	11758	285	$1.69 \cdot 10^8$
DRA7	Retention	16	21400	40	1	$3.63 \cdot 10^7$
DRA7	March C- peripheral logic	94	5060	0	0	$5.83 \cdot 10^6$
DRA4	Dynamic stress	94	630	927	21	$2.16 \cdot 10^6$
DRA4	March C-	94	630	938	19	$2.16 \cdot 10^6$

The ion hits on the DUT were registered by a channeltron located beside the end of the beam line. The channeltron detected electrons scattered from the material by the ion strikes on the DUT. The beam position on the DUT was known at the time of the ion hit detection, and thus the amount of ions and their strike positions could be known.

In the channeltron some *dark counts* occurred, with a registered hit by the channeltron without the beam being on. They were few however, and combined with the possibility that some of the actual ion strikes were not being detected, the error of the reported fluence is assumed to be less than 10 %.

V. RESULTS AND DISCUSSION

An overview of the test results can be seen in Table III. The reported bit upsets in the table is the number of bits that were upset during all tests of a certain test mode, indifferent of the test pattern, or if it was part of multiple bits being upset within the same word. All data in Table III are for runs with $F_r = 128$ kHz and $F_{op} = 100$ MHz, and are from irradiation of the bit arrays. The exception is the data for memory DRA7 with Au ions (LET of 94 MeV/(mg/cm^2)) on the peripheral logic of the memory. These data are from the irradiation areas on the central spine of the memory seen in Fig. 1.

A. Retention tests

The number of stuck bits induced by Au ions in memory DRA6 as a function of cumulative number of Au ions can be seen in Fig. 3. In this figure, the reported number of stuck bits is the cumulative number of stuck bits at each measurement point which were not found to be stuck at earlier measurement steps. This to not have the data affected by the recovery of the previously stuck bits. For Fig. 3 this representation does not qualitatively impact the resulting plot, since the number of new stuck bits induced by the Au ions was considerably larger than the ones that had recovered from previous runs. Therefore, the graph would be similar, if the total number of stuck bits in the memory was displayed instead of the cumulative number of newly stuck bits. For the number of stuck bits induced by lower LET Ca ions, this type of representation has a large effect however, as we will show later.

The data given in Fig. 3 was taken from runs with retention mode testing with alternating patterns all ‘1’ and all ‘0’. Each irradiation window (see Fig. 1) was tested with both all ‘1’ and all ‘0’ pattern. One run was excluded from the data set, because the memory was written during the ongoing irradiation. This would have been the third point from the left in the figure. Since the data shows the cumulative number of new stuck bits, and the bits which got stuck in the excluded point were accounted for, the missing data point does not affect the displayed data. A linear trend of the induced number of stuck bits as a function of the ion counts can be seen, as has been previously observed in e.g. [2].

Fig. 4 shows the cumulative number of new stuck bits that were induced in the memory DRA7 upon irradiation with Ca ions. The irradiation was carried out under retention mode testing with alternating patterns of all ‘0’ and all ‘1’, within the same single irradiation zone. In the figure, the number of stuck bits are normalized so that the first measurement point of each refresh frequency has zero stuck bits. This because the memory was previously irradiated with Au ions, and had an initial number of stuck bits. The number of new stuck bits in the memory after a given ion count is increasing more rapidly when F_r is decreased, since the longer the time is between refreshes, the more time the cell storage capacitor has to discharge and lose the stored data.

The number of new stuck bits that are induced by the Ca ions are only 1 at the nominal 128 kHz refresh frequency, and the memory is much less sensitive to the lower LET Ca ions than the Au ions, as can be seen comparing with Fig. 3. In Fig. 4, for the $F_r = 1250$ Hz case especially, the number of new stuck bits increases considerably faster in the beginning of the test than later on after a larger number of ions, where a saturation trend can be seen.

One possible explanation of this is that some of the bits in the memory were weakened during the previous Au irradiation, and the operation of the memory during the test made them get stuck at this refresh frequency. It was

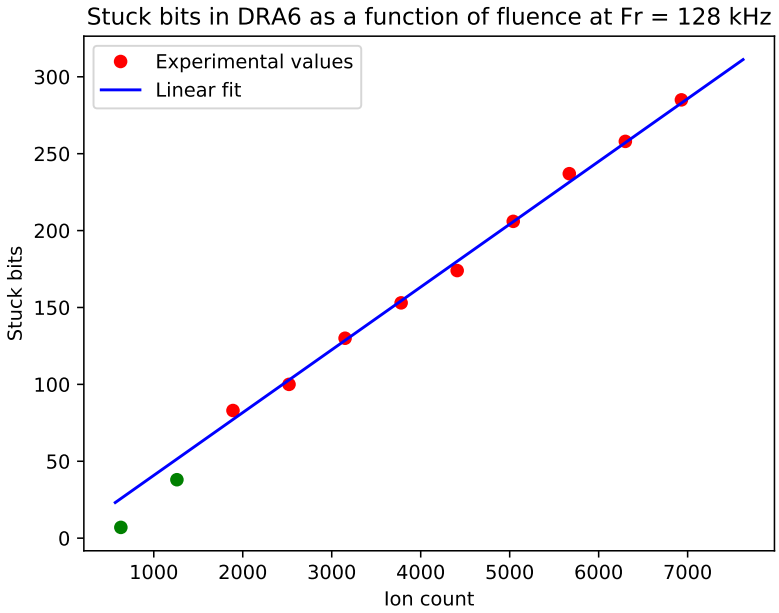


Fig. 3. Number of stuck bits in memory DRA6 as a function of cumulative fluence of Au ions. Irradiation and post irradiation treatment to find the stuck bits was done at $F_{op} = 100$ MHz and $F_r = 128$ kHz. The green points are described later on in the text.

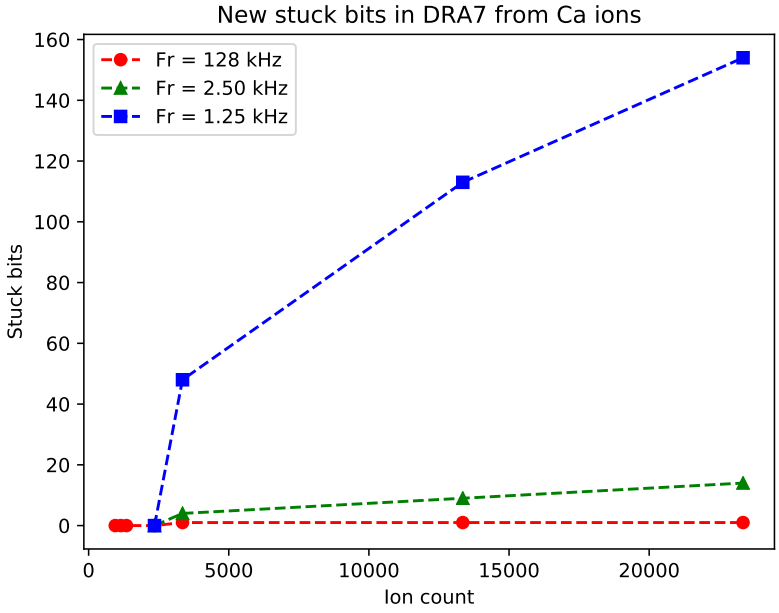


Fig. 4. Number of stuck bits in memory DRA7 as a function of cumulative fluence of Ca ions. Irradiation and post irradiation treatment to find the stuck bits done at $F_{op} = 100$ MHz, and with $F_r = 128$ kHz (red), $F_{r,min} = 2500$ Hz (green), and $F_{r,min}/2 = 1250$ Hz (blue).

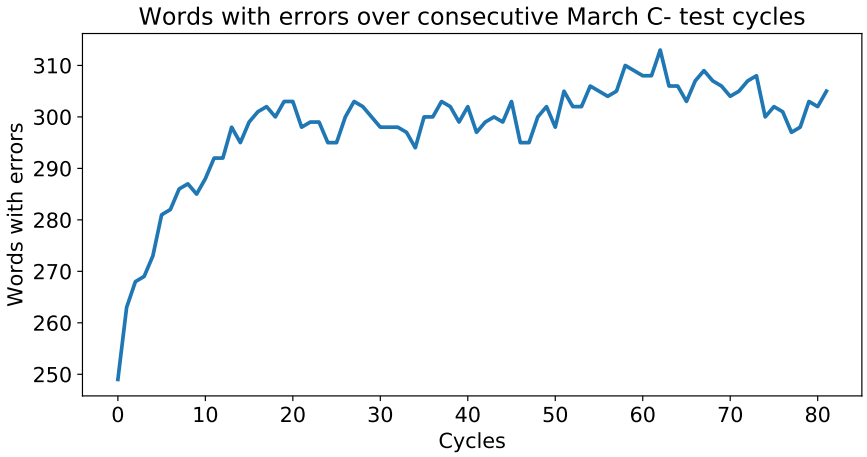


Fig. 5. Increase of the number of observed errors in DRA6 during many cycles of a modified March C- test post irradiation.

observed during dynamic testing of irradiated memories that more and more bits showed up as stuck to a value after previous iterations of the dynamic test loop. An example of this can be seen in Fig. 5. The figure shows the total number of errors found during consecutive cycles of a modified March C- test (one cycle is what is presented in (1)). The number of errors increase from around 250 in the beginning, to stabilize at about 300 errors per cycle after 10-20 cycles have been run. This suggests that even if the memory would seem operational at a certain refresh frequency, reading and writing the memory might cause weakened cells to appear as stuck. In Fig. 4, the measurement points are more tightly spaced for low fluences where the increase in stuck bits is the steepest, which supports that this could have had an effect on the data in Fig. 4.

The number of errors in Fig. 5 goes up and down over consecutive cycles. This suggests that intermittent errors are present, so that certain bits shows errors on some test cycles, and then later returns the correct value on other cycles.

B. Dynamic tests

Dynamic tests with Au ions were performed on memory DRA4 on the cell arrays, and on DRA7 on areas outside the cell arrays where the control logic is located (see irradiation zones in Fig. 1). A comparable number of upsets and stuck bits were induced when irradiating the cell arrays, as with retention mode testing using DRA6. No upsets or SEFI of any kind was observed in the memory when irradiating the control logic and parts of the memory surrounding the cell arrays with Au on DRA7. The memory was irradiated with both modified March C- (see (1)) and dynamic stress test (see (2)).

SEFIs were observed in an earlier version of a similar memory, the ISSI 512 Mb SDRAM IS42S86400B in [9]. That test was however performed in a broad beam so the ion strike locations causing the SEFI in that test can not be readily obtained.

C. Post treatment and weakened bits

Fig. 6 shows how the retention time of the cells grows shorter when they are subject to ion irradiation. The memory that has been subject to the highest fluence of Au ions has the most cells that fail at short refresh intervals (high F_r). The very high fluence of Ca ions on the memory DRA7 had little effect on the retention time distribution, and the small effect of Ca in comparison with the heavier Au ions is seen here as well as in Figs. 3 and 4.

The trends seen in Fig. 6 are similar to what can be seen in e.g. [3] and [10]. An exception to this is due to the fact that the ion irradiation in this work was done on only small parts of the die, so that a smaller population of the cells was shifted to shorter retention times. The other cells are part of a common tail to longer data retention times overlapping with the distribution of the pristine cells.

The recovery of the stuck cells due to an annealing phenomenon was mentioned earlier. The evolution of the amount of stuck bits in DRA7 during and after both irradiation campaigns, with Au and Ca, is proposed in Fig. 7. Below the figure is a time axis showing the number of hours since the Au irradiation, where the irradiations are not to scale to this time-axis. The irradiations follow the top axis, where the number of Au and Ca ions is shown respectively. Many stuck bits are seen to recover, but the behaviour is somewhat erratic and display intermittent errors. Notice also how some bits are becoming stuck and unstuck during the irradiation with Ca ions, now that the

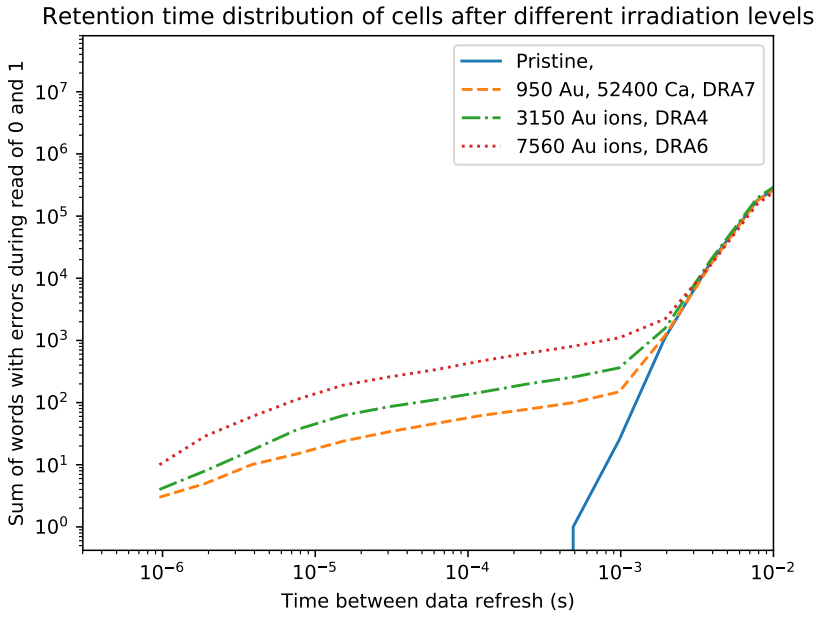


Fig. 6. Number of words containing stuck bits at different values of refresh time. The different curves shows the different memories that has been subject to a different number of ions on the cell arrays.

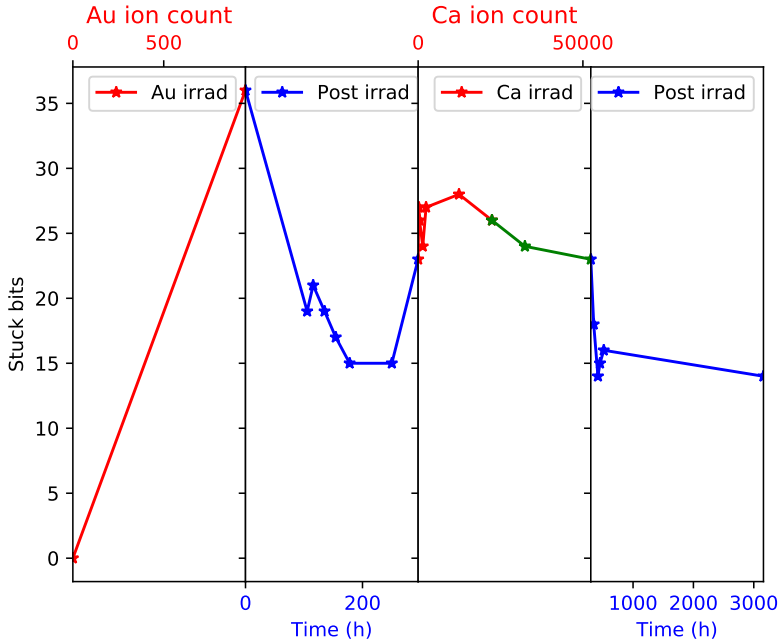


Fig. 7. The number of stuck bits in DRA7 during irradiation as a function of ion count and after irradiation as a function of time, for irradiation with both Au and Ca. The Au irradiation was done under one dynamic modified March C- test. All points are taken with $F_{op} = 100$ MHz and $F_r = 128$ kHz, except the green points during the Ca irradiation where $F_{op} = 50$ MHz.

figure shows all of the stuck bits in the memory and not the new ones compared to previous runs as was the case in Fig. 4. What can also be seen is that the bits that anneal do so in a rather short time scale, after which the number of stuck bits stays relatively constant (on the time scale of the data). This behaviour is consistent between all three tested memories.

Errors from weak bits have also in this work been seen to have a dependence on the wait time between write and read operations. For a given refresh frequency, the number of bits which return a faulty value when they are read, increases with the waiting time. This could be ascribed to that the cell capacitor leakage current is larger for the

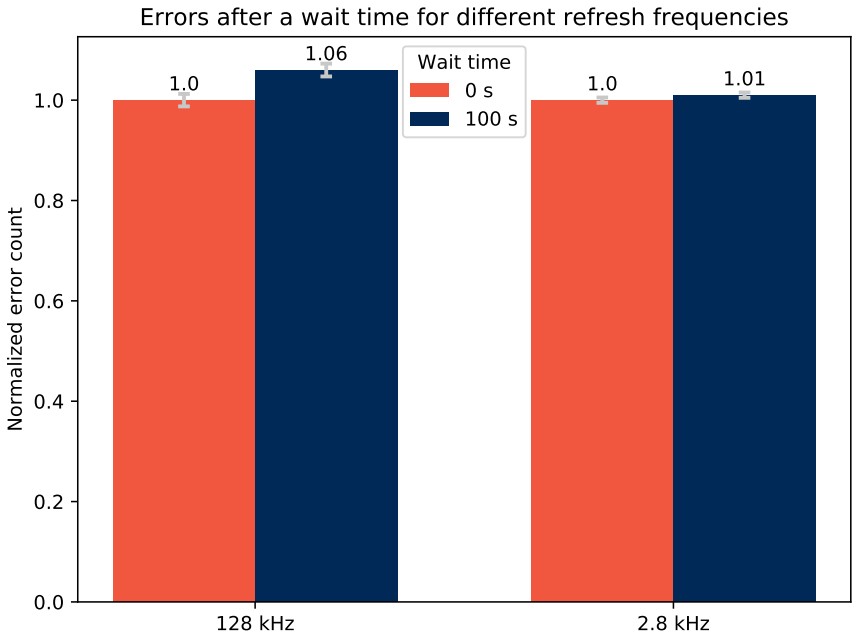


Fig. 8. A comparison between the number of errors in the memory when reading the memory immediately after writing was complete, versus waiting 100 s before reading it. The figure shows the number of errors normalized to the error count after 0 s wait time for a given value of F_r after 100 test iterations. Memory operated at $F_{op} = 100$ MHz, data from DRA6.

weak cells, making the charge stored on the capacitor smaller for the damaged cells at the time of refreshing for a given refresh frequency. For some weakened cells, the charge upon refresh will then be close to the limit of being evaluated as in the charged or discharged state. As the evaluation is subject to a certain amount of statistical noise, and as the read noise margin diminishes for discharged cells, evaluation errors of the weak cells will then happen with some probability in each refresh cycle and over time these weak cells will, one after the other, eventually be evaluated as being in the discharged state. From then on, the refresh controller will maintain them in the discharged state.

This effect is shown in Fig. 8. Here is seen that there are fewer detected errors if the memory is read immediately after writing is completed (0 s wait time in the figure), compared to if a wait time is inserted before reading the memory (100 s wait time in the figure). In Fig 8 the relative difference is larger for the higher refresh frequency 128 kHz than for the lower $F_r = 2.8$ kHz. This is due to the fact that a larger total number of errors were observed at the lower refresh frequency, but the difference in the number of errors between the two cases was similar.

The test was done so that the memory was written with a pattern, then read immediately. Subsequently the memory was rewritten, then read after a 100 s wait time period while the memory was only refreshing. This was repeated 100 times. A handful (on average 3 for both F_r) more bits were upset after the 100 s wait time than after 0 s wait time in both cases per test iteration, but a larger number of total errors at $F_r = 2.8$ Hz (about 350 per read compared to about 60 per read for 128 kHz) made the relative difference smaller for this refresh frequency. The error bar magnitude is the square root of the measured error number.

The data in the figures presented here have for this reason been measured with a consistent time between the write and read operations of the data sets presented within each figure. An exception is the first two data points in Fig. 3, where the time was not registered, but probably shorter than the other data points in the same figure. These points also exhibit a lower number of stuck bits than the rest, following the linear trend in the figure.

VI. Summary

Stuck and weak bits in the ISSI 512 Mb SDRAM were studied at the microbeam facility in GSI with irradiation experiments using Au and Ca ions. The manner in which the weak bits can cause errors in the memory when changing parameters such as the refresh frequency were investigated. Using the memory (reading and writing) also affects the number of stuck bits, so that more bits manifests themselves as stuck when the memory is operated. Also the wait time between write and read operations have an impact on the number of errors that are observed in the memory.

No upsets or errors were observed when irradiating regions of the memory outside the bit arrays.

ACKNOWLEDGEMENT

The results presented here are part of a project (RADSAGA) that has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Sklodowska-Curie grant agreement No 721624. This work was also in part supported by the European Space Agency under Contract 4000124504/18/NL/KML/zk. The results are based on an experiment which was performed at the UNILAC microprobe beam line at the GSI Helmholtzzentrum für Schwerionenforschung, Darmstadt (Germany) in the frame of FAIR Phase-0.

Thanks to Veronique Ferlet-Cavrois for her contribution to the beam time proposal to GSI.

REFERENCES

[1] G. M. Swift, D. J. Padgett, and A. H. Johnston, "A new class of single event hard errors," *IEEE Trans. Nucl. Sci.*, vol. 41, no. 6, pp. 2043–2048, Dec. 1994.

[2] L. D. Edmonds, S. M. Guertin, L. Z. Scheick, D. Nguyen, and G. M. Swift, "Ion-induced stuck bits in 1T/1C SDRAM cells," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pp. 1925–1930, Dec. 2001.

[3] H. Shindou, S. Kuboyama, N. Ikeda, T. Hirao, and S. Matsuda, "Bulk damage caused by single protons in SDRAMs," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 1839–1845, Dec. 2003.

[4] L. D. Edmonds and L. Z. Scheick, "Physical mechanisms of ion-induced stuck bits in the hyundai 16M x 4 SDRAM," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3265–3271, Dec. 2008.

[5] A. M. Chugg, J. McIntosh, J. Burnell, P. H. Duncan, and J. J. Ward, "Probing the nature of intermittently stuck bits in dynamic RAM cells," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3190–3198, Dec. 2010.

[6] A. Rodriguez, F. Wrobel, A. Samaras, F. Bezerra, B. Vandevelde, R. Ecoffet, A. Touboul, N. Chatry, L. Dilillo, and F. Saigné, "Proton-induced single-event degradation in SDRAMs," *IEEE Trans. Nucl. Sci.*, vol. 63, no. 4, pp. 2115–2121, Aug. 2016.

[7] A. M. Chugg, A. J. Burnell, P. H. Duncan, S. Parker, and J. J. Ward, "The random telegraph signal behavior of intermittently stuck bits in SDRAMs," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3057–3064, Dec. 2009.

[8] L. Dilillo, G. Tsiligiannis, V. Gupta, A. Bosser, F. Saigne, and F. Wrobel, "Soft errors in commercial off-the-shelf static random access memories," *Semiconductor Science and Technology*, vol. 32, no. 1, p. 013006, dec 2016.

[9] F. Irom and M. Amrbar, "Heavy ion single event effects measurements of 512Mb ISSI SDRAM," *2015 IEEE Radiation Effects Data Workshop REDW*, pp. 1–6, 2015.

[10] J. P. David, F. Bezerra, E. Lorfèvre, T. Nuns, and C. Inguimbert, "Light particle-induced single event degradation in SDRAMs," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3544–3549, Dec. 2006.