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Improving TID Radiation Robustness of a CMOS OxRAM-based Neuron Circuit by Using Enclosed Layout Transistors

Pablo Ilha Vaz, Patrick Girard, Arnaud Virazel, and Hassen Aziza.

***Abstract*—Aerospace applications are attractive candidates to embed Artificial Neural Networks despite their excellent parallel processing capability and reduced energy consumption. Nonetheless, the long-term exposure to incidence levels of ionizing radiation may degrade their physical components reducing, therefore, their reliability and expected lifetime. Thus, it is mandatory to face the challenge of enhancing the radiation hardening characteristics of a neural circuit before operating in harsh environments. A possible solution to substantially reduce long-term spurious effects caused by ionizing radiation (referred to as Total Ionizing Dose - TID) is to change the conventional rectangular MOS gate geometry to a non-standard topology referred to as Enclosed Layout Transistor (ELT). In the context of hardening a complete neuron circuit against TID effects, together with the well-established ELT paradigm, it is possible to exploit the inclusion of other hardened devices, for instance, the memory element. In this sense, the Oxide-based Resistive Random Access Memory (OxRAM) can be used as the memory element, which is inherently tolerant against ionizing radiation, and, hence, better suited for a fully hardened circuit. In this work, we propose to harden the design of an existing OxRAM-based neuron circuit [1] through the inclusion of ELTs, i.e., to improve the radiation hardening characteristics of a preexistent convenient neuron circuit topology by using the enclosed gate geometry for the n,pMOS devices. Electrical simulations, considering a standard commercial bulk CMOS fabrication process, in a $180\,nm$ technology, have been carried out to validate our proposed design. Additionally, we exploit two simulation setups. First, the OxRAM's behavior in a simple circuit configuration, to provide a better understanding of the OxRAM device. Second, the OxRAM-based neuron circuit, to evaluate the behavior of the proposed neuron circuit hardened with ELTs. The simulation results, supported by the analysis of former works regarding the incidence of ionizing radiation in OxRAM and ELTs, indicate that the proposed hardened neuron circuit is a feasible solution to embed neuromorphic computing in aerospace applications.**

***Index Terms*—Artificial Neural Networks, bulk CMOS, Enclosed Layout Transistor, OxRAM, Neuron circuit, Radiation Hardening, Fault-tolerance.**

I. Introduction

THE emergence of Artificial Neural Networks (ANNs) has brought a paradigm shift in computing architectures with brain-inspired systems. In contrast with the conventional von Neumann's computation, ANNs have the ability to learn and adapt through complex nonlinear relationships [2]. Moreover, this biological-inspired approach has an excellent parallel computing capability with a significantly lower power consumption when compared to Central Processing Units (CPUs) and Graphic Processing Units (GPUs) [3]. In this context, critical applications, such as Space & Satellite (S&S), which impose severe constraints in terms of power consumption and computing efficiency, are excellent candidates to embed ANNs.

Nonetheless, applications exposed to incidence levels of ionizing radiation, as in the case of S&S, may have their physical components degraded. Depending on the energy of the incident particle, and time exposure to such ions, this ionizing radiation gives rise to transient upsets or even permanent damage to the device's materials [4]–[6]. Thus, this vulnerability becomes a significant issue when designing a circuit operating properly between acceptable error margins, i.e., failure tolerance, for a baseline application.

In this context, to embed a state-of-the-art neuromorphic circuit operating in harsh environments, it is necessary to face the challenge of enhancing its radiation hardening characteristics, thus satisfying its reliability constraints.

As introduced in Fig. 1, there are several techniques capable of hardening a device to mitigate the effects associated with the incidence of ionizing radiation. The methods referred in Fig. 1 range from the higher abstraction level (i.e., the system-level) to the lower abstraction level (i.e., the layout-level).

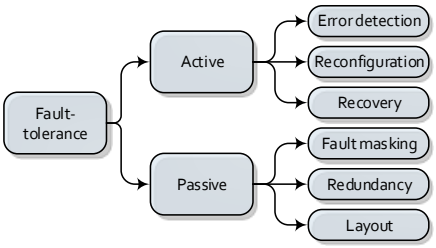

Fig. 1. Summary of different approaches to exploit fault-tolerance.

At the system-level, the widespread reasoning to deal with transient faults and errors (i.e., the manifestation of faults in a system [6], [7]) has its basis on mechanisms relying on redundancies together with voting-based schemes [8], [9]. Nevertheless, the drawback of such an approach is a direct area overhead (i.e., higher cost) and lower computing performance, mainly due to the additional data processing.

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Therefore, such drawbacks become intractable to conceive redundancies, without a proper strategy on a large scale [7].

On the other hand, regarding long-term and cumulative exposure to ionizing radiation, it is possible to harden a CMOS device by applying specific changes at the layout-level. Hardening the basic building block of ICs, i.e., a single transistor, allows the system to achieve the highest level of tolerance against long-term exposure, maintaining the possibility to embed other higher-level mitigation techniques [5], [10].

Favorably, at the system-level, neuromorphic computing systems have some levels of intrinsic fault-tolerance, inherited from their natural properties, e.g., self-distributed connections [3]. Thus, by adopting a proper neural circuit topology, it is effortless to absorb some vulnerabilities.

In contrast, at the layout-level, standard commercial bulk CMOS devices have physical regions intrinsically susceptible to collect and store unwanted radiation-induced spurious charges. In this case, it is possible to eliminate (or substantially reduce) such locations by laying out a different non-standard device topology. In this sense, a potential solution is to adopt the annular gate geometry referred to as Enclosed Layout Transistor (ELT) [5], [10]–[12], a well-established topology capable to efficiently reducing these sensitive regions.

In fact, by combining complementary approaches, applicable at various abstraction levels, as shown in Figure 2, it is possible to achieve the highest level of fault-tolerance [7], [13]. Indeed, this composition can complement one to each other, to exploit the ultimate benefit brought by the emerging brain-inspired computing paradigm, enhanced through well-established fault-tolerance techniques, necessary to properly operate in harsh environments.

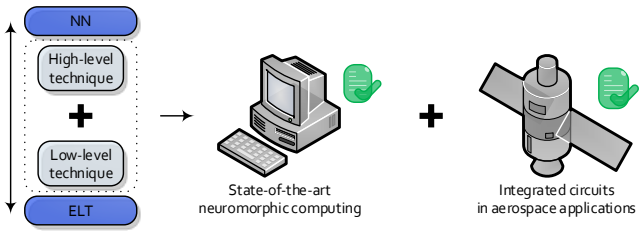

Fig. 2. A combination of different fault-tolerance approaches allows an ANN to extends its lifetime in aerospace applications.

Thus, in this work, taking into account the reliability challenges associated with the possibility to consolidate a state-of-the-art ANN in aerospace applications, we present the design of the basic building block of brain-inspired networks, i.e., a neuron cell, hardened through the inclusion of ELTs. To this purpose, we use the neuron circuit topology introduced in [1] that includes Oxide-based Resistive Random Access Memory (OxRAM) device as the memory element, which is inherently tolerant against ionizing radiation [14], and, hence, better suited for a fully hardened circuit.

Previous related works [5], [15]–[17], which are supported based on measurement results, have demonstrated the intrinsic hardening characteristics of ELTs when compared to standard gate geometry. These studies confirm that the proposed neuron circuit may have even higher radiation tolerance than the original topology based only on OxRAM devices and standard gate geometry. In other words, it is expected an increase in radiation tolerance because the OxRAM devices are intrinsically tolerant. Furthermore, all CMOS devices (standard topology) are changed for their hardened version (enclosed topology).

To the best of our knowledge, this is the first work proposing to harden the design of an existing neuron circuit topology integrating these two hardened solutions (i.e., ELT and OxRAM). Therefore, such design has relevant value to explore further artificial neural units, e.g., synapses, and to solve complex tasks in aerospace applications using neuromorphic computing.

The remaining of this work is organized as follows. Section II introduces the basic concepts related to Ionizing Radiation, its effects on circuits and systems, and the ELT paradigm. Section III introduces the fundamentals of brain-inspired computing and OxRAM technology. Section IV presents the neuron circuit topology adopted in this work. Sections V and VI describe the simulation setup, and simulation results, respectively. Finally, Section VII provides the conclusion of the work.

II. Ionizing radiation and Enclosed Layout Transistor theory background

Circuit reliability constitutes an imperative role for applications operating in environments exposed to ionizing radiation, for instance, those in aerospace, aeronautics, and, even at the ground level, as high-energy physics. Therefore, to maintain an integrated circuit proper operation inside acceptable error margins throughout an extended lifetime, it is mandatory to enhance its radiation hardening characteristics [12].

When radiation particles travel through solid materials, they may transfer kinetic energy to atomic electrons [4]. Depending on the energy of the incident particle, this interaction produces a path composed of electron-hole pairs ($\bar{e}/h$) [18], [19]. However, these $\bar{e}/h$ produced during the ion incidence may migrate when exposed to an external electric field, for instance, as generated when biasing a MOS device. The change resulted from this charge migration, i.e., the flow rate of electric charge, results in unwanted behavior in MOS devices, giving rise to transient upsets or permanent damage both for analog and digital circuit operations [18], [19]. In other words, while the interaction of the radiation particles occurs in a reverse-biased PN junction, the distortion of the depletion layer may cause a transient spurious current pulse, whose behavior may lead to functional failures. In these cases, a proper architecture-level circuit design, based on redundancies and voting schemes, can be adopted to mitigate unwanted characteristics, e.g., such as bit-flips [6].

On the other hand, while the ionizing radiation hits the oxide regions, such as the gate-oxide (SiO_2), the electric field, inherently existent due to device bias, may disrupt electronic bounds transporting the generated carriers. Through this process, as shown in Figure 3, the electrons, which have higher mobility, are removed from the dielectric, leaving the less mobile holes in the oxide [10], [20]–[24].

The holes within SiO_2 experience a stochastic hopping transport through localized states toward the cathode direction,

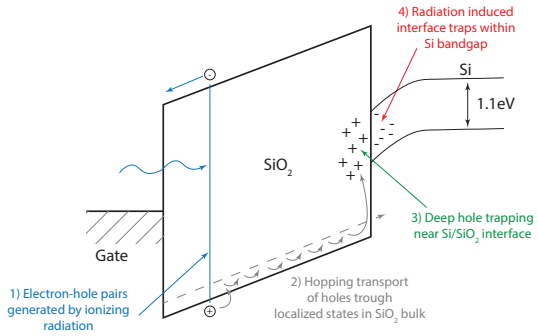

Fig. 3. Energy band diagram for charge generation and charge transport in SiO_2 [10].

until they become trapped near the SiO_2/Si interface. This positive (and accumulated) charge near the interface between the dielectric and silicon bulk may consequently induce the formation of an inversion layer in the channel region [23]. The presence of this parasitic inversion layer has observable effects such as threshold voltage shift for the device, and the increase in the leakage current, which especially for reduced oxide thickness (i.e., for gate lengths of about $0.24\,\mu m$), is considered the most prominent spurious degradation [6], [10], [25].

To achieve high levels of tolerance to permanent damage caused by ionizing radiation, a robust design should be embedded at the layout-level to prevent the susceptible regions from storing parasitic charge [5], [11]. One well-established solution to minimize the accumulation of long-term radiation-induced parasitic charge is to change the standard commercial gate disposal (i.e., straight polysilicon stripe) to the annular geometry referred to as Enclosed Layout Transistors (ELTs) [5], [10]–[13], [16], [17], [24]. Instead of standard two-edged devices, related in Figure 4 (I) and (III), the use of ELTs, Fig. 4 (II), eliminates the transition region where the polysilicon layer extends over the well-to-substrate boundary, hence, significantly reducing the radiation-induced leakage current which may exist between source and drain (S/D) contacts [5], [11].

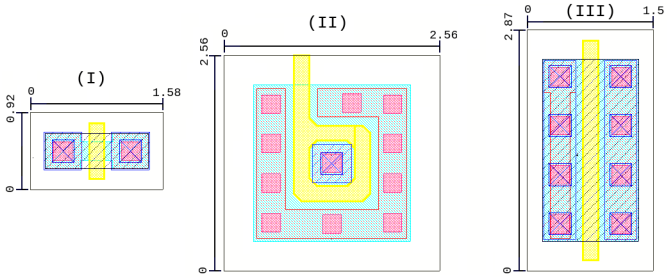

Fig. 4. a) Minimum-sized standard two-edged device, b) Minimum-sized ELT, and c) Standard two-edged device equivalent to the minimum-sized ELT.

In the field of radiation tolerance, researchers have made a substantial contribution to the High Energy Physics domain, which has investigated and characterized commercial devices under ionizing radiation [5]. Moreover, in our recent work [10], based on experimental results, we have performed an extensive analysis of ELTs and deeply investigated the effects of the incidence of cumulative radiation, thus corroborating the findings presented in former works.

In this previous work [10], we characterized and evaluated the output characteristic $(I_D\ vs.\ V_{DS})$ and transfer function $(I_D\ vs.\ V_{GS})$ of the nELTs, pre- and post-radiation following both the same design methodology and W/L equations as analyzed during the current work.

From this study [10], we have extracted Fig. 5, which provides a sample of the transfer function behavior, respectively for minimum-sized (a) standard (STD), and (b) ELT when exposed to different irradiation doses. An oxide thickness of $12.5\,nm$ was used in both cases.

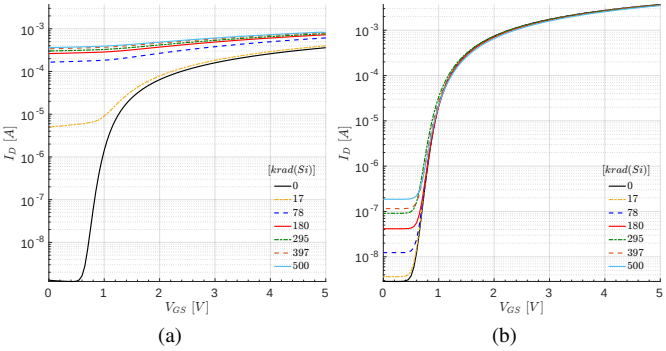

Fig. 5. $(I_D\ vs.\ V_{GS})$ nMOS characteristics, respectively for: STD devices (a) and ELT (b).

Based on referred experimental irradiation measurements (i.e., from Fig. 5), we observed increments of approximately 3 orders of magnitude in the leakage current (I_{leak}) of nSTD devices when irradiated up to $500\,krad(Si)$. On the other hand, in the same irradiation experiments, for ELTs, we verified deviations of less than 1% in the I_{leak}. These previous experimental irradiation results clearly demonstrate that the proposal of hardening an OxRAM-based neuron circuit through the addition of ELTs will improve its radiation hardening characteristics.

Additionally, recently, related work [14] has deeply investigated the effects of the incidence of the transient heavy-ion strikes and cumulative radiation dose in a 1-Transistor-1-Resistor (1T1R) structure, similarly as presented during this current work. In this study, the presented results have shown that the resistive RAM neuromorphic computing systems are highly resistant against transient SEEs due to their lower cross-section. Moreover, they are also tolerant to multi-Mrad levels of total ionizing and displacement damage doses, i.e., even harder than ELT paradigm.

Finally, the electrical simulation results presented in this work, together with the support of previous practical irradiation measurements, presented in Fig. 5, clearly demonstrate that the proposal of hardening an OxRAM-based neuron circuit through the addition of ELT paradigm improves its radiation hardening characteristics.

Nonetheless, the determination of the aspect ratio (W/L) in ELTs is not a straightforward task. In ELTs, conversely to standard-devices, the electric field under the gate corners is not uniform and, thus, a methodology is needed to estimate

the equivalent aspect ratio of such devices. In our previous work [10], we have deeply investigated a wide range of ELT's $(W/L)_{eff}$ predictions. In this work, we adopted the equations first presented in [11].

III. OxRAM-BASED NEUROMORPHIC SYSTEMS THEORY BACKGROUND

The basic building block of ANNs are neurons (or nodes), and the transmission of their information occurs through electrical signals, in the form of spikes (conveyed by synapses).

In an ideal ANN, each neuron should be able to receive an input signal, i.e., stimuli from a previous synapse, and change its internal structure accordingly to better process it.

Through this brain-inspired paradigm, it is viable to accomplish matrix vector-based tasks, such as image pattern recognition, with remarkable energy efficiency and matching performance when compared to CPUs and GPUs [3], [26].

Together with ANNs, recent advances in non-volatile memories (NVMs) have emphasized the opportunity to perform in-memory computing, a pivotal character to emulate an *in situ* learning mechanism. In this direction, during the last few years, the scientific community has proposed the first neuron circuits and synapses integrating NVMs [27].

In this context, one of the promising device to act as the memory element is the OxRAM cell. The OxRAM cells are excellent candidates to be designed within ANNs, especially regarding their compatibility with CMOS back-end-of-line (high integration density), exceptional switching speed (fast programming), and low energy operation [28], [29], [40], [41].

An OxRAM device is a Metal-Insulator-Metal (MIM) based element. Its metal oxide can be composed of a range of different materials, such as HfO_2, NiO, TiO_2, and TaO_2, all of them compatible with the CMOS processes. In this work, as depicted in Fig. 6, we considered a HfO_2-based cell.

From the designer's perspective, i.e., behavioral view, the stack of $TiN/Ti/HfO_2/TiN$, Fig. 6, can be seen as a resistive switching device or, in other words, as a two-terminal device adjustable resistor.

The OxRAM operation relies on the formation/dissolution of an internal Conductive Filament (CF), as shown in Fig. 6. While the CF does not exist (or is weakly formed), the device can be considered in the OFF state (with very High Resistance State - HRS). Then, it is possible to gradually switch their conductance by increasing the magnitude of the voltage potential between its top (V_T) and bottom terminals (V_B). With the occurrence of this voltage potential increment, the OxRAM passes throughout a plethora of intermediate states, until the total formation of the CF, where it reaches the ON state (with very Low Resistance State - LRS).

The evolution of the CF occurs based on the generation and migration of oxygen ions (O^{2-}) and vacancies (V_o) inside the OxRAM cell. Thus, to accurately simulate such devices, it is necessary to have a proper physical model prediction. In this sense, we invite the reader to consult the related work [31], which presents an extensive comparison among a series of distinct OxRAM models.

Figure 7, introduced in [30], illustrates the above OxRAM device operation with a sample of the measurements of the I-V characteristics made on real OxRAM device in the logarithm scale. In the referred figure, it is possible to verify the abrupt change between the HRS and the LRS when the difference voltage potential between V_T and V_B reaches specific values (i.e., V_{SET} and V_{RESET} required to switch from HRS to LRS and from LRS to HRS, respectively) [30].

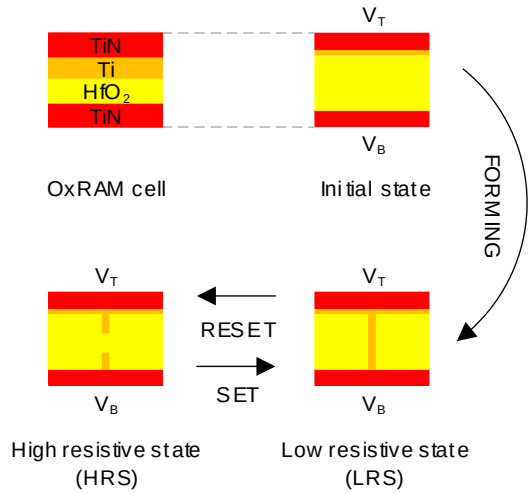

Fig. 6. Basic conceptual OxRAM operations.

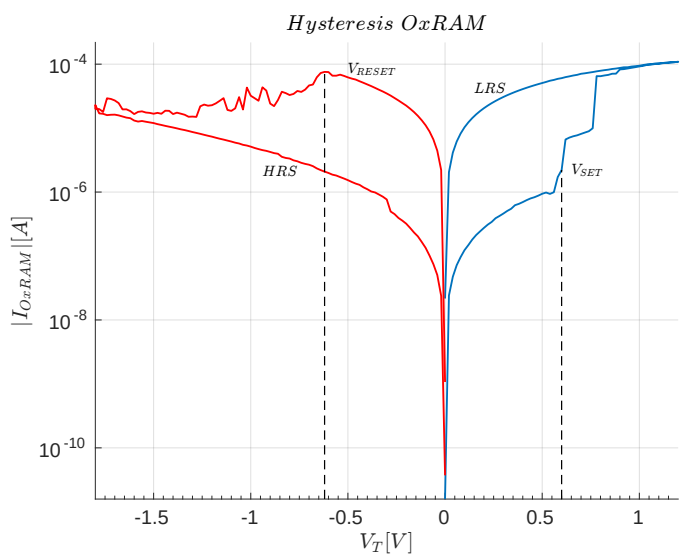

Fig. 7. I-V characteristics of an OxRAM device in the logarithm scale.

In this work, we adopted the model introduced by Stanford [32]. This referred model captures both DC and AC electrical characteristics of OxRAM devices with physics-based compact model descriptions.

IV. BULK CMOS NEURON ARCHITECTURE

One of the first conceptual and purest implementations of a neuron model is known as the Leaky Integrate and Fire (LIF) model [33]. The global mixed-signal concept of a LIF neuron suggests two main procedures: the integration of input signals, and an additional trigger mechanism, which is activated when the integration process reaches a certain threshold value.

The primary operation of a LIF neuron circuit is present in Fig. 8 [1]. The procedure of integration of the excitatory input signal is modeled by the capacitor C_{mem} (i.e., C_{mem} models the cell membrane). The continued process of integration increases cell membrane potential (V_{mem}). Thus, when V_{mem} reaches the threshold voltage (V_{th}), the neuron circuit fires, generating an output spike. Finally, the capacitor is discharged. Regarding the fact that the cell membrane is not ideal, the charge slowly *leaks* through the capacitor - hence, explaining the conceptual *leaky* behavior. The resistor R models its behavior in parallel with the capacitor C_{mem}.

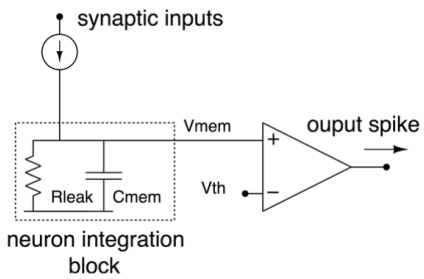

Fig. 8. Basic conceptual working operation of a Leaky Integrate and Fire neuron circuit [1].

The first procedure, i.e., the integration of input synaptic stimuli, plays the role of the brain's ability to store synapsis history. The electronic equivalent to emulate such brain-inspired memory behavior can be designed, for instance, through OxRAM devices – regarding their advantages when compared to CMOS based-components, as introduced in Sec. III.

The second procedure, i.e., trigger activation, receives the signal of integration threshold and, when reaches the limit value, generates a digital output spike to be sent to post-neurons and to reset the current one.

Taking into account the previous conceptual implementation of a LIF neuron circuit, the block diagram presented in Fig. 9 introduces the complete neuron topology analyzed in this work. The original circuit architecture has been introduced in [1]. In this work, we propose reducing the long term degradation caused by the incidence of ionizing radiation of the neuron circuit by changing the gate geometry of the standard two-edged devices (which are identified by M_{ref}, M_1 to M_7, and the switches S_1 to S_4) using the ELT paradigm. In this work, the remaining neuron circuit blocks, i.e., *RS Latch* and *Pulse Gen.*, are simulated with functional VerilogA codes..

The neuron circuit can be understood as the composition of three distinct blocks: the *Current comparator*, the trigger (the combination of the *RS Latch* and *Pulse generator*), and the *Feedback path*.

The *Current comparator* block is responsible for integrating the input signal coming from the *VPreSpike* pin (i.e., V_T in the current block). The core of this current integration block is the OxRAM element, in which each excitatory input signal slightly changes its internal conductance. The maximum current which flows through the OxRAM (I_{OxRAM}) is regulated by the constant current input source pin (I_{thr}) – due to $M_{1,2}$ current mirror. Hence, the current difference between I_{thr} and I_{OxRAM} is "calculated" and amplified due to the current

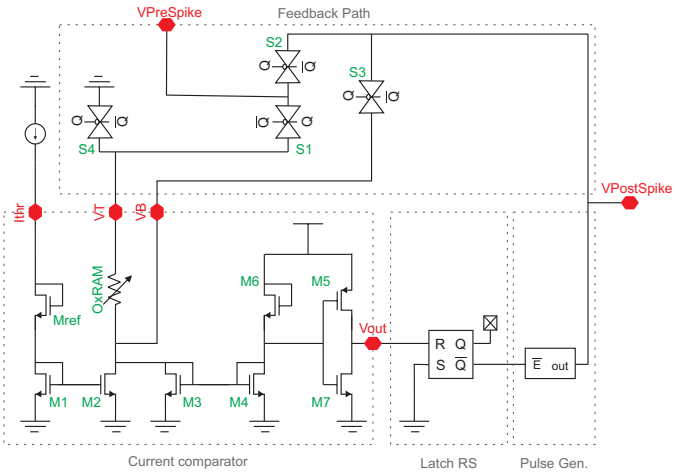

Fig. 9. Schematic view of the analyzed neuron circuit.

mirror $M_{3,4}$. Finally, when the I_{OxRAM} exceeds I_{thr}, the analog output V_{out} reaches the digital equivalent *high level*, i.e., the voltage necessary to activate the next block.

The trigger mechanism, represented in Fig. 9 by the combination of the *RS Latch* and *Pulse generator* sub-blocks, receives (and monitors) the analog output of the preceding block (V_{out}). When V_{out} reaches the threshold voltage necessary to active (or reset) the *RS Latch*, the intermediate signal $\bar{Q}$ falls to the digital equivalent *low level*. Thus, the *Pulse generator* produces the *VPostSpike* signal – a single output pulse with both voltage and period predetermined.

The last block, the *Feedback path*, is formed by a set of switches (S_1 to S_4). The role of this block is to allow a proper input/output signal decoupling between *VPreSpike* (neuron input) and *VPostSpike* (neuron output and internal reset signal V_B).

V. Simulation Setup

With the aim to provide a better understanding of the OxRAM device, and subsequently to evaluate the behavior of the proposed neuron circuit hardened with ELTs, we exploit two different simulation setups:

A) The OxRAM's behavior in a simple circuit configuration.
B) The OxRAM-based neuron circuit.

Moreover, for each simulation setup (i.e., *A* and *B*) we propose to acquire a sub-set of simulations based on three different n,pMOS device variations:

- STD_{min}: Minimum-sized standard two-edged devices.
- ELT_{min}: Minimum-sized ELT rules.
- STD_{equ}: Standard two-edged devices with the $(W/L)_{eff}$ equivalent to the ELT_{min}.

For simulating the OxRAM switching behavior, we adopted the SPICE-compatible *Stanford model V2* [32]. Besides, the electrical level simulations are performed at the SPICE level, using a commercial CAD tool in a $180\,nm$ bulk CMOS technology.

The decision to use a $180\,nm$ CMOS technology to perform our simulations was motivated by the possibility to integrate the same ELT data (i.e., layout constraints and its effective

equivalent W/L aspect ratio) acquired in our last work [10] for comparison purpose. In our perspective, the ELT's design and its modeling equations are the most sensitive parameters to support a functional layout proposal and a correct prediction of the effective W/L aspect ratio of such layouts.

A. OxRAM device

The OxRAM's behavior is analyzed in a single 1T1R circuit configuration, as depicted in Fig. 10. This configuration, introduced in [34], is a standard circuit arrangement for OxRAM's applications and, thus, to analyze its switching behavior [27], [35]–[37].

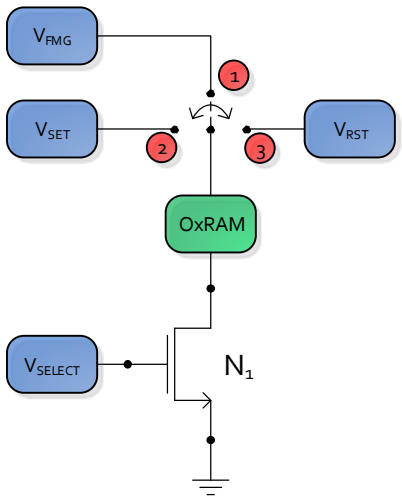

Fig. 10. OxRAM in a single 1T1R circuit configuration.

To emulate a complete cycle operation of the OxRAM or, in other words, its complete hysteresis characterization – related to the formation and dissolution of the CF – after an initial forming stage (V_{FMG}), its top electrode voltage should vary by ranging from V_{SET} to $-V_{RST}$. Moreover, the gate voltage (V_{SELECT}) should be configured to limit the maximum current which flows through their terminals.

Regarding device's sizes, the OxRAM is considered with an area of $1\,pm^2$ (in a square geometry of $1\,\mu m \times 1\,\mu m$), and the nMOS device (N_1) in both STD_{min} and ELT_{min} configurations considers the minimum DRC features. Furthermore, the width of the nMOS in the STD_{equ} configuration is designed to be equivalent to the $(W/L)_{eff}$ of the ELT_{min}.

Despite the minimum DRC features, the ELT's minimum geometry (ELT_{min}) has a $(W/L)_{eff}$ of approximately 9.8 times greater than the minimum standard two-edged (STD_{min}). Therefore, to allow a fair comparison with the same limiting OxRAM's writing current, the nMOS gate voltages for both ELT_{min} and STD_{equ} configurations were set to compare all arrangements with the same current (around $100\mu A$ – the same value used during the neuron circuit simulations).

Finally, transient simulations are performed within a supply voltage (i.e., top electrode voltage V_T) specified in steps of $100\,\mu s$ considering the following intermediate voltages: $0; 1.2; 0; -1; 0\ [V]$.

It is noteworthy that the afore-described circuit configuration and methodology to extract the OxRAM's Figures of Merit (FoMs) follows the general procedures described in related works [32], [35], [38].

B. Neuron circuit

The neuron cell circuit behavior is analyzed in the topology presented in Fig. 9. As in the previous OxRAM configuration setup, the simulation Test Bench (TB) is proposed to compare the figures of merit of ELTs against those of standard two-edged devices. Thus, the same n,pMOS arrangements are considered for STD_{min}, ELT_{min}, and STD_{equ}.

In each configuration, the input/output signals *VPreSpike*, *VPostSpike*, V_{out}, and, V_Q are monitored during simulations. Initially, the input value for the threshold current takes into account the detection precision of the difference between I_{OxRAM} and I_{thr}. In this case, related studies about OxRAM programming current have reported an error of less than 0.1% for $100\,\mu A$ embedded in the same built-in current comparator and similar oxide thickness [1]. Thus, such nominal value is chosen.

Regarding devices sizing, Table I presents both width and length of n,pMOS devices. The value 1 designates the minimum device size; higher values correspond to multiples of their minimum dimensions.

TABLE I
NEURON CIRCUIT TB DEVICES' SIZES.

$Device$	M_{ref}	$M_{1,7}$	M_5	$nMOS\ S_{1,4}$	$pMOS\ S_{1,4}$
$Width$	1	1	2	9	9
$Lenght$	1	1	1	1	1

Finally, Table II summarizes the entire group of simulation parameters.

TABLE II
NEURON CIRCUIT TB SIMULATION PARAMETERS.

$Variable$	I_{thr}	t_{period}	$t_{fall,rise}$	V_{DD}
$Value$	100μ	$100n$	$100p$	1.8
$Unit$	A	s	s	V

VI. SIMULATION RESULTS

Following the simulation setup descriptions introduced in Section V, this Section presents the simulation results for the OxRAM device and the OxRAM-based neuron circuit.

A. OxRAM device

Figure 11 presents the switching behavior of the OxRAM cell. The first graph ($V_T\ vs.\ time$) describes the evolution of the supply voltage applied at the top electrode. The intermediate graph ($I_{OxRAM}\ vs.\ time$) shows the current which flows through the OxRAM for each nMOS device (i.e., STD_{min}, ELT_{min}, and STD_{equ}). The last graph ($Filament\ Creation\ vs.\ time$) presents the evolution of the filament creation during the switching process. The values, given in percentage, were normalized to ease the representation from the virgin stage (i.e., 0%) to the strongly formed (i.e., 100%).

Although the percentage of the filament creation is the same (during several periods), the current flowing through the ELT and STD devices' terminals are different. This difference occurs because of the difference in the devices' geometry and the gate voltage values. Besides, the difference appears less prominent when comparing ELT_{min} vs. STD_{equ} than when comparing ELT_{min} vs. STD_{min} because in the first case the device is *calculated* to behave as if it were an ELT.

Figure 12 presents the hysteresis of the I-V switching characteristics of the OxRAM device. The results are shown for the three nMOS devices (i.e., STD_{min}, ELT_{min}, and STD_{equ}) in the log-normal plot. Note that the Stanford model parameters are calibrated on an actual technology (the $130nm$ node), and, as a consequence, Fig. 12 is expected to reflect silicon data.

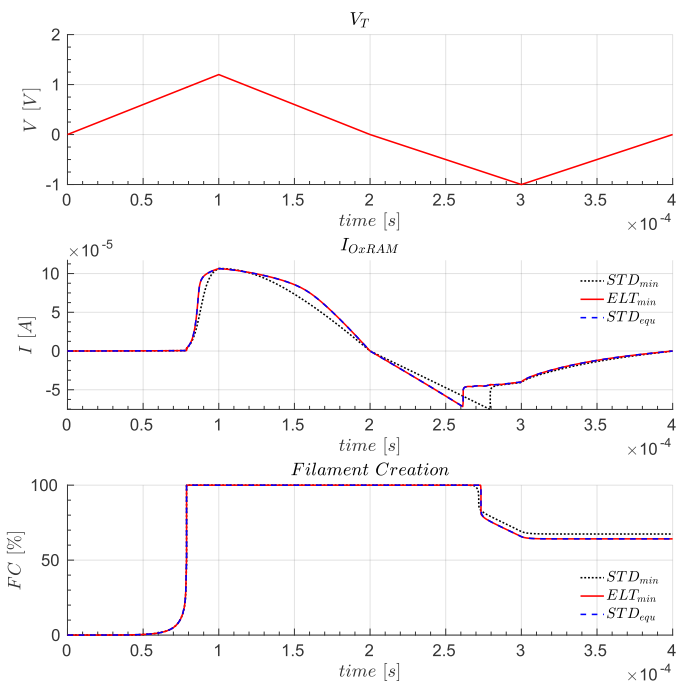

Fig. 11. Transient simulation results for OxRAM device: I) V_T $vs.$ $time$, II) I_{OxRAM} $vs.$ $time$, and III) $Filament\ Creation$ $vs.$ $time$.

In a quantitative analysis of the OxRAM I-V switching characteristics, presented in Figures 11 and 12, it is possible to verify that the typical fingerprints correspond to what is expected based on the sample results, presented in the original Stanford model reference [32]. The Stanford model is a proven model, calibrated on the proposed OxRAM technology. It accurately reproduces the OxRAM cell behavior during SET and RESET operations. The functional correspondence behavior is crucial to support the coherent OxRAM simulation for the three simulated gate arrangements (i.e., STD_{min}, ELT_{min}, and STD_{equ}).

Regarding calculation of OxRAM cell parameters (Fig. 12), Table III shows the achieved FoMs in which, referred variables, respectively represent: $I_{LRS,HRS}$, the low resistance (maximum) and high resistance (minimum) currents during switching; $V_{HRS,LRS}$, the voltages related to high and low resistive states; and, $R_{HRS,LRS}$ the resistances related to high and low resistive states.

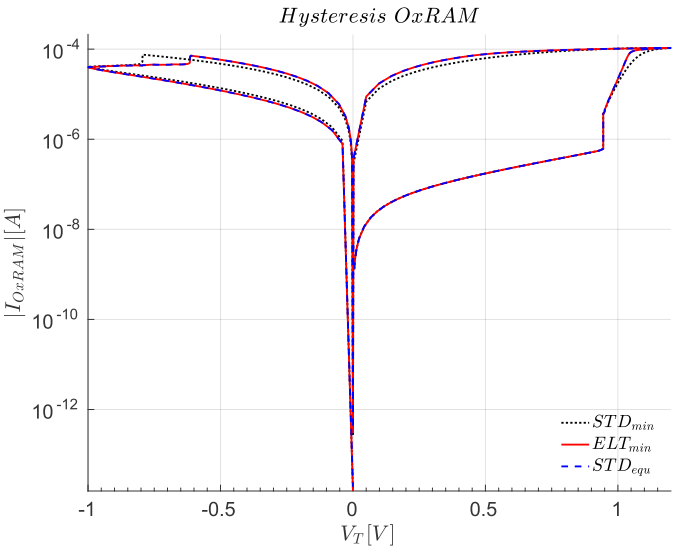

Fig. 12. Simulated I-V characteristics for bipolar OxRAM device in the Log-normal scale.

TABLE III
CALCULATED PARAMETERS OF OXRAM'S HYSTERESIS.

$Parameter$	STD_{min}	ELT_{min}	STD_{equ}
I_{LRS} $[\mu A]$	106.5	106.4	106.3
I_{HRS} $[\mu A]$	-67.2	-86.2	-86
V_{HRS} $[mV]$	-709	-730	-730
V_{LRS} $[V]$	1.18	1.19	1.19
R_{HRS} $[M\Omega]$	3	3.15	3.15
R_{LRS} $[k\Omega]$	11.1	11.2	11.2

Considering the qualitative insight related to the hysteresis simulation results, which are presented in Table III, we also confirm coherence with the Stanford model [32]. In this case, the original Stanford's work reports the high resistive state R_{HRS} values about 3 orders of magnitude higher than for lower state (i.e., R_{LRS}), an I_{LRS} about two times higher than the absolute value of I_{HRS}, and a higher V_{LRS} than V_{HRS}. This similar trend is also reported in other related works [31], [39].

B. Neuron circuit

Figure 13 shows the simulation results for the OxRAM-based neuron circuit. In the referred figure, (a) illustrates the behavior of the main input/output signals monitored during one cycle of ELT_{min} topology functioning (i.e., *VPreSpike*, V_{out}, V_Q, and, *VPostSpike*). Additionally, for the three neuron simulated configurations, Fig. 13 (b) presents the current which flows both through the OxRAM and the M_3 device (specified in Fig. 9). For each analyzed configuration, the quantitative values for the calculation of the average current through OxRAM ($Icell_{Avg}$) and the energy per cycle (or spike) ($E/Cycle$) are presented in Table IV.

Regarding the neuron circuit, this work adopted the same simulation methodology and calculations procedure, as reported in the reference work [1]. This conformity allows a direct behavior and performance comparison against the original one. In this context, the reference work, evaluated in $130\,nm$

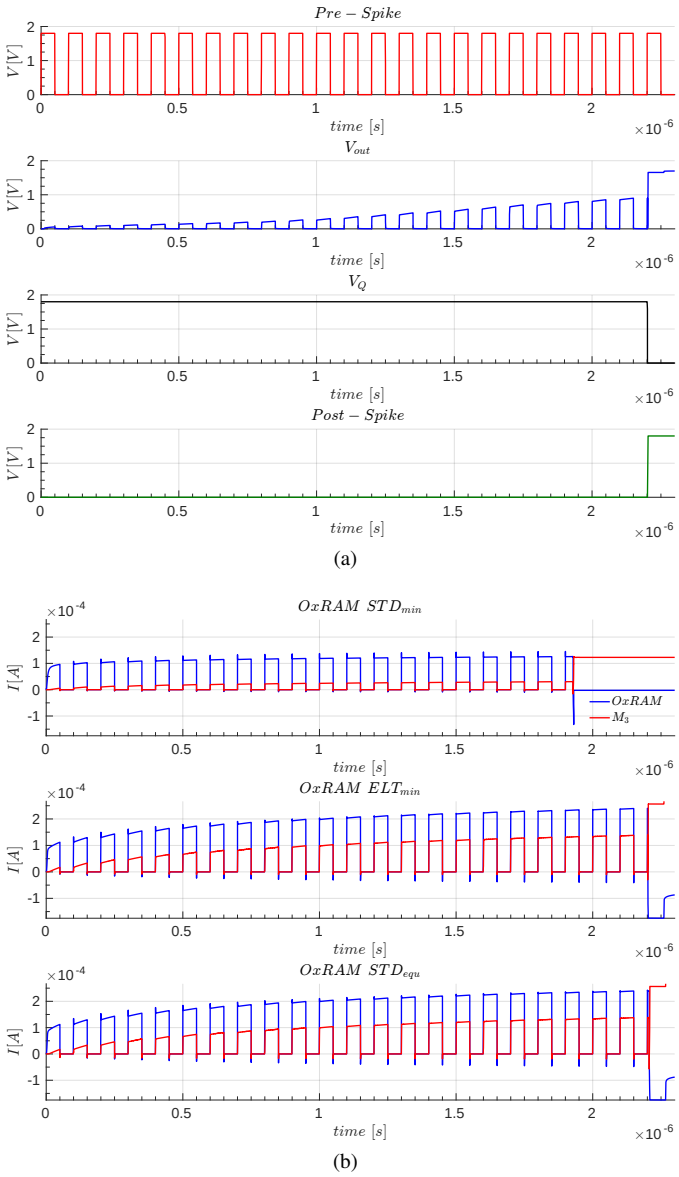

Fig. 13. Transient simulation results for the OxRAM-based neuron circuit: a) main input/output signals, and b) current through the OxRAM device.

TABLE IV
NEURON CIRCUIT FIGURES OF MERIT COMPARISON.

FoM \ Dev. type	STD_{min}	ELT_{min}	STD_{equ}
$Icell_{(Avg)}$ $[\mu A]$	5.35	7.68	7.69
$E/Cycle$ $[pJ]$	9.63	13.82	13.85

and biased with a $V_{DD} = 3.3\,V$, reports an energy per cycle $(E/Cycle)$ equal to $33\,pJ$, and an average current $\left(Icell_{(Avg)}\right)$ of $10\,\mu A$.

By comparing the above referenced values against those from Table IV, at first, we observe a reduction in the $Icell_{(Avg)}$ of the STD_{min} configuration of about $\approx 1.8\times$. This value is in absolute accordance with what was expected, since the V_{DD} in the reference work is $3.3\,V$, and, in this work $1.8\,V$ (i.e., a voltage difference ratio about $\approx 1.8\times$). It is noteworthy that the I_{thr} current is an adjustable parameter, besides, the correspondence between ELT_{min} and STD_{equ}, in terms of current conduction, corroborates their equivalent behavior.

Moreover, the increment in the $E/Cycle$ of the ELT_{min} when compared against STD_{min} represents $\approx 1.4\times$. This increase is due to the area increment, which in practice, establishes the increment in the effective (W/L) aspect ratio, i.e., the effective (W/L) of a minimum-sized ELT is about 9.8 times higher than the (W/L) of the STD_{min}.

It is noteworthy that the inclusion of ELTs does not affect the functional behavior of the neuron circuit. In this case, the functional correspondence can be confirmed not only by $Icell_{(Avg)}$ and $E/Cycle$, presented in Table IV, but also substantiated with Fig. 13 (b) in which the neuron circuit *fires* in the same cycle (i.e., when comparing ELT_{min} vs. STD_{equ}). The asymmetry between the source/drain areas of the ELT_{min} when compared to STD_{equ} configuration diminishes the $E/Cycle$ about $\approx 0.2\%$ and the $Icell_{(Avg)}$ about $\approx 0.13\%$. This almost negligible difference is in absolute accordance with what was expected since the STD_{equ} has sized according to the same effective (W/L) of the ELT_{min}, and, thus, the only remaining difference is related to the source and drain different areas.

Regarding the physical neuron circuit area estimation, we calculated the relation among the three MOS different configurations. The quantitative values for the area analysis are given in Table V. In this table, the *Device relation* $(STD_{min}\ vs.\ \#)$ represents the area difference calculated between MOS type and the reference value STD_{min}. Moreover, the $Width\ vs.\ Length$ represents the relation between the cell's width and length, and, finally, $Area$ refers to the total neuron cell area for each MOS type. It is noteworthy that all area estimations only take into account the layout of the MOS devices, as depicted in Fig. 4.

From Table V, it is possible to calculate the inherent area penalty necessary to implement ELTs, as shown in Fig. 4. When comparing the area overhead between a minimum-sized single two-edged device to a minimum-sized ELT, the area increases by 4.51 times.

Moreover, when estimating the total neuron circuit area, i.e., taking into account the OxRAM device alongside ELTs, we presume that the silicon overhead should be negligible. It occurs because the OxRAM devices are placed on top of the CMOS subsystem during the back-end phase, contrary to conventional capacitors, which demand an extensive area. In this work, we considered the OxRAM device with the dimensions of $1\mu m \times 1\mu m$. This area (i.e., $1pm^2$) represents only about 15% of a single ELT device designed with minimum DRC rules, as presented in Fig. 4 (b). These values for the area estimation are in accordance with our previous work [24], in the same technology node, based on practical results.

TABLE V
NEURON CIRCUIT AREA COMPARISON.

Device relation	STD_{min}	ELT_{min}	STD_{equ}
$STD_{min}\ vs.\ \#$	1.00	4.51	2.96
$Width\ vs.\ Length$	0.58	1.00	1.91
$Area$	8.30	37.42	24.58

Finally, regarding the interchangeable (i.e., different) source and drain areas of an ELT, the preceding slight reduction in

the FoMs can be related to the fact that an ELT has a reduced output capacitance. In an ELT, the choice for an enclosed drain reduces the associated output capacitance. Therefore, shorter switching times are required to charge/discharge such capacitances [10], [24].

VII. Conclusion

In this work, to face the reliability challenges related to the incidence of ionizing radiation in ICs and to consolidate a state-of-the-art ANN in aerospace applications, we presented the design of an OxRAM-based neuron circuit, hardened through the inclusion of ELTs.

To the best of our knowledge, this is the first work that addressed the design of a preexistent convenient OxRAM-based neuron circuit integrating ELT paradigm.

To provide the reader a better understanding of both the OxRAM and ELTs and, thus, to ease the evaluation of the OxRAM-based neuron circuit, we performed two different simulation setups: the OxRAM behavior in a simple 1T1R configuration, and the OxRAM-based neuron circuit. For each simulation setup, we presented the simulation results in a sub-set of three different n,pMOS arrangements: the standard two-edged device, the minimum-sized ELT, and the standard two-edged equivalent to the minimum sized ELT.

The electrical level simulation results presented in this work for both OxRAM and the neuron circuit are in accordance with practical measurements reported on former works. Therefore, this coherence supports a proper OxRAM model usage and a correct neuron circuit functional behavior.

Demonstrating (or identifying) in which irradiated dose the circuit will cause an error, fail, or stop correctly working was not among the main purposes of this work. Thus, simulating the whole circuit, including the TID effects for specific absorbed doses, is outside the scope of this work.

After all, when introducing ELTs, the simulation proposals and analysis presented in this work have proven that, at the cost of the area, it is possible to harden a preexistent neuron circuit topology. Moreover, when taking into account the OxRAM devices, laid-out into back-end-of-line (BEOL), we expect a negligible area overhead, thus, reiterating the relevance of this work in the field of reliability of neural networks embedded in aerospace applications.

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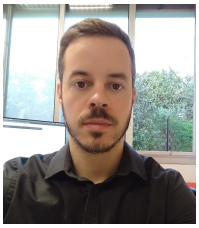

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