Design of Radiation Hardened Latch and Flip-Flop with Cost-Effectiveness for Low-Orbit Aerospace Applications

Aibin Yan, Aoran Cao, Zhelong Xu, Jie Cui, Tianming Ni, Patrick Girard, Xiaoqing Wen

Design of Radiation Hardened Latch and Flip-Flop with Cost-Effectiveness for Low-Orbit Aerospace Applications

Aibin Yan, Aoran Cao, Zhelong Xu, Jie Cui, Tianming Ni, Patrick Girard, *Fellow*, *IEEE*, and Xiaoqing Wen, *Fellow*, *IEEE*

***Abstract*—To meet the requirements of both cost-effectiveness and high reliability for low-orbit aerospace applications, this paper first presents a radiation hardened latch design, namely HLCRT. The latch mainly consists of a single-node-upset self-recoverable cell, a 3-input C-element, and an inverter. If any two inputs of the C-element suffer from a double-node-upset (DNU), or if one node inside the cell together with another node outside the cell suffer from a DNU, the latch still has a correct value on its output node, i.e., the latch is effectively DNU hardened. Based on the latch, this paper also presents a flip-flop, namely HLCRT-FF that can tolerate SNUs and DNUs. Simulation results demonstrate the SNU/DNU tolerance capability of the proposed HLCRT latch and HLCRT-FF. Moreover, due to the use of a few transistors, clock gating technologies, and high-speed paths, the proposed HLCRT latch and HLCRT-FF approximately save 61% and 92% of delay, 45% and 55% of power, 28% and 28% of area, and 84% and 97% of delay-power-area product on average, compared to state-of-the-art DNU hardened latch/flip-flop designs, respectively.**

***Index Terms*—Radiation hardening, latch design, flip-flop design, soft error, double-node-upset**

I. Introduction

With the advancement of manufacturing technologies of *integrated circuits* (*ICs*) into the deep nano-scale era, the integration and performance of circuits have been significantly improved. Meanwhile, the operational voltage of a circuit is correspondingly lowered so as to reduce power dissipation. However, as the critical charge of circuit nodes decreases with technology scaling, the radiation induced reliability issues of safety-critical applications (even terrestrial) are becoming more and more serious. That is, even low-energy particles in the terrestrial environment can also cause soft errors [1]. Soft errors are transient errors mainly caused by radiative particles. Statistical evidences are abundant that soft errors caused by particles of various types have become a severe problem for advanced ICs [2-3], especially for aerospace applications.

Single-node-upsets (*SNUs*), *double-node-upsets* (*DNUs*), *single-event-transients* (*SETs*), and *single-event-latchups* (*SELs*) are typical soft errors. Among them, SNUs and DNUs are dominating causes for soft errors [4]. When a particle strikes a sensitive node in a storage element, such as a latch or a flip-flop, the generated carriers can be collected by the source drain diffusion area, causing a voltage perturbation on the affected node. If the amount of injected charge exceeds that of the critical charge of the affected node, the stored value on the node may be flipped to an invalid value. This phenomenon is called an SNU. Moreover, in nano-scale CMOS technologies, a single-particle striking may affect two adjacent nodes due to the charge-sharing mechanism, causing voltage perturbations on the two nodes. This phenomenon is called a DNU. Since SNUs and/or DNUs can lead to system-level soft errors in the worst case, many effective schemes to improve circuit reliability against SNUs and DNUs have been proposed using the popular *radiation hardening by design* (*RHBD*) approach.

The design targets of radiation hardening mainly include memory cells [2, 5], *flip-flops* (*FFs*) [6, 7], and latch designs [8-18]. In recent years, many hardened latch designs have been proposed to mitigate SNUs, including the *High-Performance SNU Tolerant* (*HPST*) [8], *High-performance Low-cost Robust* (*HLR*) [9], and *Feedback Redundant Soft error Tolerant* (*FERST*) [10] latch designs. Moreover, corresponding hardened FF designs can be constructed from such latches to mitigate SNUs, including the HPST-FF, HLR-FF and FERST-FF. These designs either employ the RHBD approach, such as *dual-modular redundancy* (*DMR*), *feedback loops interlocking* (*FLI*), and guard gates, or introduce delays in feedback mechanisms to robustly retain values in presence of SNUs. However, most of these designs cannot tolerate DNUs, making them unsuitable to low-orbit aerospace applications that require high reliability.

Manuscript received ????,????; A preliminary version of this paper was presented at the IEEE Asian Test Symposium (ATS 2019) [1].

Aibin Yan, Aoran Cao, Zhelong Xu and Jie Cui are with the School of Computer Science and Technology, Anhui University, Hefei 230601, China. (E-mail: {abyan, cuijie}@mail.ustc.edu.cn, arcao_ahu@163.com, restraintxu@qq.com).

Tianming Ni is with the College of Electrical Engineering, Anhui Polytechnic University, Wuhu 241000, China. (E-mail: timmyni126@126.com). He is the corresponding author.

Patrick Girard is with the Laboratory of Informatics, Robotics and Microelectronics of Montpellier, UMR 5506, University of Montpellier / CNRS, Montpellier 34095, France (E-mail: girard@lirmm.fr).

Xiaoqing Wen is with the Graduate School of Computer Science and Systems Engineering, Kyushu Institute of Technology, Fukuoka 820-8502, Japan (E-mail: wen@cse.kyutech.ac.jp).

To effectively mitigate DNUs, many novel latch designs have been proposed [3, 19-30, 38], including the *DNU self-Recoverable* (*DNURL*) [3], *Circuit and Layout Combination Technique* (*CLCT*) [23], *Double Node Charge Sharing SNU Tolerant* (*DNCSST*) [24], *Delta Dual-Interlocked-Cell* (*DeltaDICE*) [25] and *Single Event Double-Upset-Fully-Tolerate (SEDUFT)* [38] latch designs. Moreover, corresponding hardened FF designs can be constructed from such latches to mitigate DNUs, including the DNURL-FF, CLCT-FF, DNCSST-FF, DeltaDICE-FF, and SEDUFT-FF. These designs mainly employ techniques, such as increasing transistor feature sizes for weak nodes, *triple-modular redundancy* (*TMR*), and layout modification solutions to get wider node spacing, well isolation, and guard rings. However, the DNURL, CLCT, DNCSST, DeltaDICE, and SEDUFT latch/FF designs have large overhead in terms of transmission delay, power dissipation, silicon area, and *delay-power-area product* (*DPAP*), making them unsuitable for low-orbit aerospace applications that also require cost-effectiveness. Moreover, some advanced designs that can tolerate both DNUs and *triple-node-upsets* (*TNUs*) have been proposed recently [31-33]. However, these latch/FF designs are mainly used for aerospace applications in harsh radiation environments that require very high reliability and have to use redundancy-induced large area/delay/power overhead.

In our previous work, a novel DNU-hardened latch, namely HLCRT latch, with cost-effectiveness, has been proposed [1]. In this paper, the HLCRT latch is extended to an FF, namely HLCRT-FF, for low-cost and low-orbit aerospace applications. The HLCRT latch is mainly constructed from a *Dual-Interlocked-Cell* (*DICE*) [34], a 3-input *C-element* (*CE*), and an inverter. When one node inside the DICE cell together with another node outside the DICE cell are affected by a DNU, or any two inputs of the CE are affected by a DNU, the latch still has a correct value on its output node. The HLCRT-FF is mainly constructed from a master latch and a slave latch that are both HLCRT. Thus, the HLCRT-FF still has the similar reliability and cost-effectiveness as the HLCRT latch. Simulation results demonstrate the SNU/DNU tolerance capability and cost-effectiveness of the proposed HLCRT latch/FF design compared to state-of-the-art DNU hardened latch/FF designs, indicating that the proposed latch/FF can be applied to low-orbit aerospace applications that require not only high reliability but also cost-effectiveness.

The rest of the paper is organized as follows. Section II discusses the existing hardened latch/FF designs. Section III details the implementation, working principles, and robustness assessment of the proposed latch design. Section IV details the implementation, working principles, and robustness assessment of the proposed FF design. Section V presents comparison and evaluation results for latches and FFs. Section VI concludes the paper and introduces further work.

II. Previous Hardened Latch and Flip-Flop Designs

Among existing hardened latch designs, such as the HPST [8], HLR [9], FERST [10], CLCT [23], DNCSST [24], DeltaDICE [25], DNURL [3], and SEDUFT [38], CEs and DICE cells are widely used as important components. Their circuit schematics and symbols are shown in Fig. 1. A CE behaves as an inverter if its inputs have the same value but goes into *high-impedance state* (*HIS*) if its inputs change and become different. This means that a CE can temperately retain the previous value when entering into HIS. A DICE cell can return to the correct value when any of its nodes suffers from an SNU [34].

Fig. 2 shows the schematics of representative SNU and DNU hardened latch designs. The HPST latch [8] in Fig. 2-(a) mainly employs two interlocked feedback loops connecting to a clock-gating based 2-input CE to tolerate SNUs. However, the HPST latch cannot provide complete DNU tolerance capability since the inputs of the output-level CE of the latch can be flipped by a DNU.

The HLR latch [9] in Fig. 2-(b) mainly employs two traditional D-latches connected to a clock-gating based 2-input CE to tolerate SNUs. However, the HLR latch cannot effectively tolerate DNUs since it is not DNU-

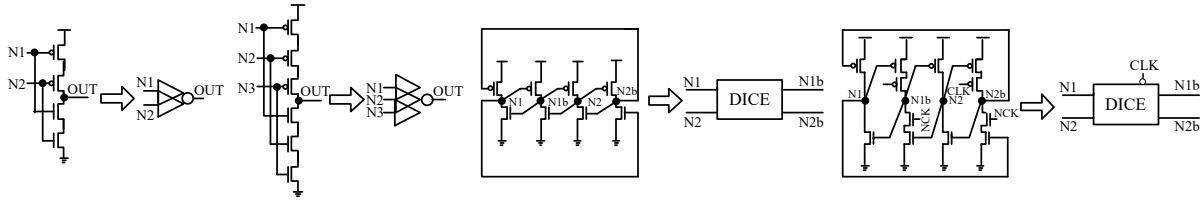


Fig. 1. Schematics and symbols of the widely used components (C-elements and DICE cells) in hardened latch and flip-flop designs. (a) 2-input C-element, (b) 3-input C-element, (c) DICE cell, (d) Clock-gating based DICE cell.

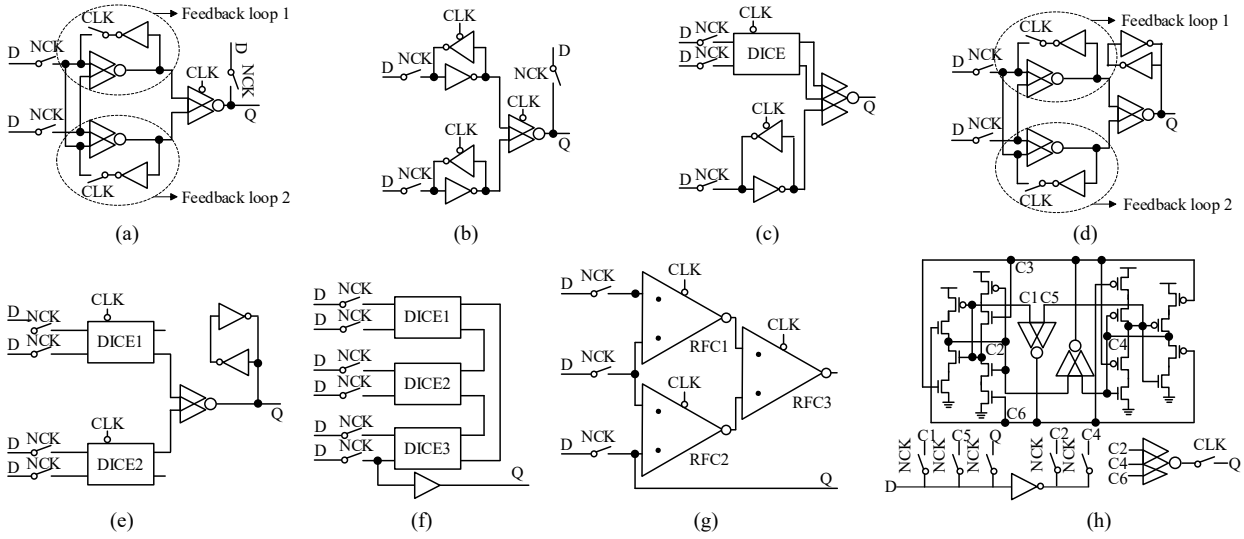


Fig. 2. Schematics of SNU and DNU hardened latch designs. (a) HPST [8], (b) HLR [9], (c) CLCT [23], (d) FERST [10], (e) DNCSST [24], (f) DeltaDICE [25], (g) DNURL [3] and (h) SEDUFT [38].

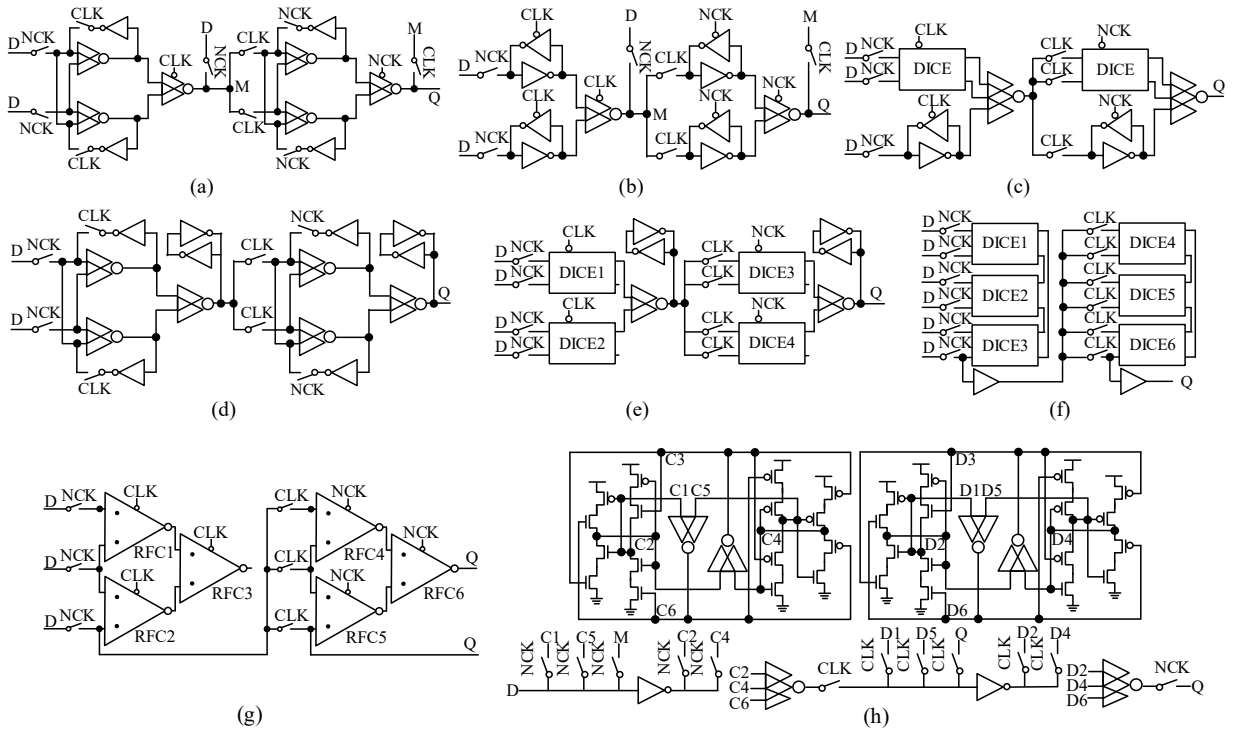


Fig. 3. Schematics of representative SNU and DNU hardened latch designs. (a) HPST-FF, (b) HLR-FF, (c) CLCT-FF, (d) FERST-FF, (e) DNCSST-FF, (f) DeltaDICE-FF, (g) DNURL-FF and (h) SEDUFT-FF.

hardened as the HPST latch.

The CLCT latch [23] in Fig. 2-(c) mainly employs a clock-gating based DICE cell and a clock-gating based keeper connected to a 3-input CE to tolerate SNUs and DNUs. However, the CLCT latch has a counter-example that it cannot tolerate a DNU if the DNU affects the output and the bottom input of the 3-input CE.

The FERST latch [10] in Fig. 2-(d) mainly employs two interlocked feedback loops and a keeper connected to a 2-input CE to tolerate SNUs. However, the FERST

latch cannot effectively tolerate DNUs since it is not DNU-hardened as the HPST latch.

The DNCSST latch [24] in Fig. 2-(e) mainly employs two clock-gating based DICE cells connected to a 2-input CE and a keeper connected to the output of the latch to tolerate SNUs and DNUs. However, the power dissipation of the DNCSST latch is large due to the large current competition especially in the keeper. Moreover, the delay of the DNCSST latch is large since there are many devices in its transmission path from D to Q.

The DeltaDICE latch [25] in Fig. 2-(f) mainly employs three interlocked DICE cells and a buffer to tolerate SNUs and DNUs. However, the power dissipation of the DeltaDICE latch is large due to the large current competition inside and between DICE cells.

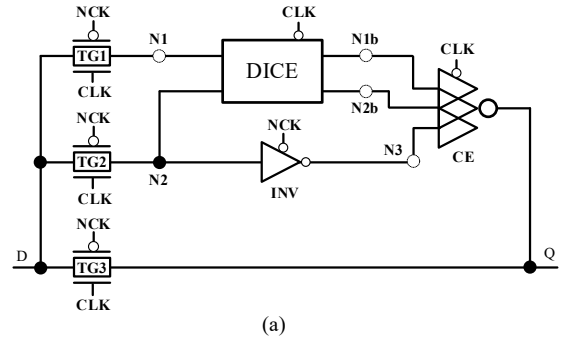
The DNURL latch [3] in Fig. 2-(g) employs three RFC cells [17] to tolerate SNUs and DNUs. However, the power dissipation of the DNURL latch is large due to its large area.

The SEDUFT latch [38] in Fig. 2-(h) mainly employs a four interlocked branch circuits based storage element, two 2-input CEs, and a 3-input CE connected to the output of the latch to tolerate SNUs and DNUs. However, the power dissipation of the SEDUFT latch is also large.

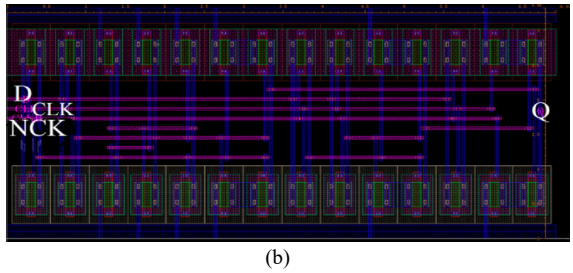
Fig. 3 shows the schematics of representative SNU and DNU hardened FF designs. They are constructed from the latches shown in Fig. 2.

III. Proposed HLCRT Latch Design

A. Circuit Schematic and Behavior



(a)



(b)

Fig. 4. Proposed HLCRT latch design. (a) Schematic, (b) Layout.

The schematic and layout of the proposed HLCRT latch design are presented in Fig. 4. The HLCRT latch is constructed from a DICE cell that can self-recover from any possible SNU, a 3-input CE with clock-gating (CG) that can intercept errors, an inverter with CG, i.e., INV in Fig. 4, and four transmission gates (TGs), i.e., TG1, TG2, TG3, and TG4 as shown in Fig. 4. Note that the differences between the proposed HLCRT latch and the CLCT latch shown in Fig. 2-(c) are discussed: (1) We create a high-speed path from D to Q to reduce transmission delay. (2) We use a clock-gating based inverter feeding the bottom input of the 3-input CE. Meanwhile, the 3-input CE is still based on clock-gating so as to reduce power dissipation. (3) We connect the DICE with the clock-gating based inverter to feed the CE in transparent mode.

In the latch structure, D is the input, Q is the output, and CLK and NCK are the system clock and negative system clock signals, respectively. The HLCRT latch has two operation modes, i.e., transparent mode and hold mode. In transparent mode, CLK is high and NCK is low. As a result, TG1, TG2, and TG3 are ON. In the case of D = 0, since N1 and N2 are directly driven by D through TG1 and TG2, respectively, it is clear that N1 = N2 = 0. This means that the inputs of the DICE cell can be determined. However, the DICE cell will not output values on N1b and N2b, due to the OFF states of the transistors with CG in the DICE cell. This means that the feedback loops are not constructed in the DICE cell in transparent mode, resulting in reduced current competition on nodes to save power dissipation. At the same time, all transistors with CG in INV are ON, and thus N3 = 1. Therefore, not all inputs of the CE can be determined and then the CE outputs no value in initialization. Note that, in other transparent mode, the output of the CE depends on previous values of N1b and N2b that are in HIS. Furthermore, TG3 is ON, and thus the output node Q is directly driven by D through TG3 (Q = D = 0), instead of being driven by the inputs of the CE since only some of the inputs of the CE are determined. This can avoid current competition on Q to reduce both power dissipation and transmission delay for the latch. It can be seen that all the critical transistors of the latch are correctly pre-charged in transparent mode. In the case of D = 1, a similar scenario can be observed.

When CLK is low and NCK is high, the latch operates in hold mode. In this case, TG1, TG2, TG3, and the transistors with CG in INV are OFF, and the transistors with CG in the DICE cell are ON. This means that the pre-charged N1 and N2 can drive N1b and N2b, and then all inputs of the CE have values since the DICE cell outputs values on N1b and N2b, and N3 still has its previous value, making the latch output the stored val-

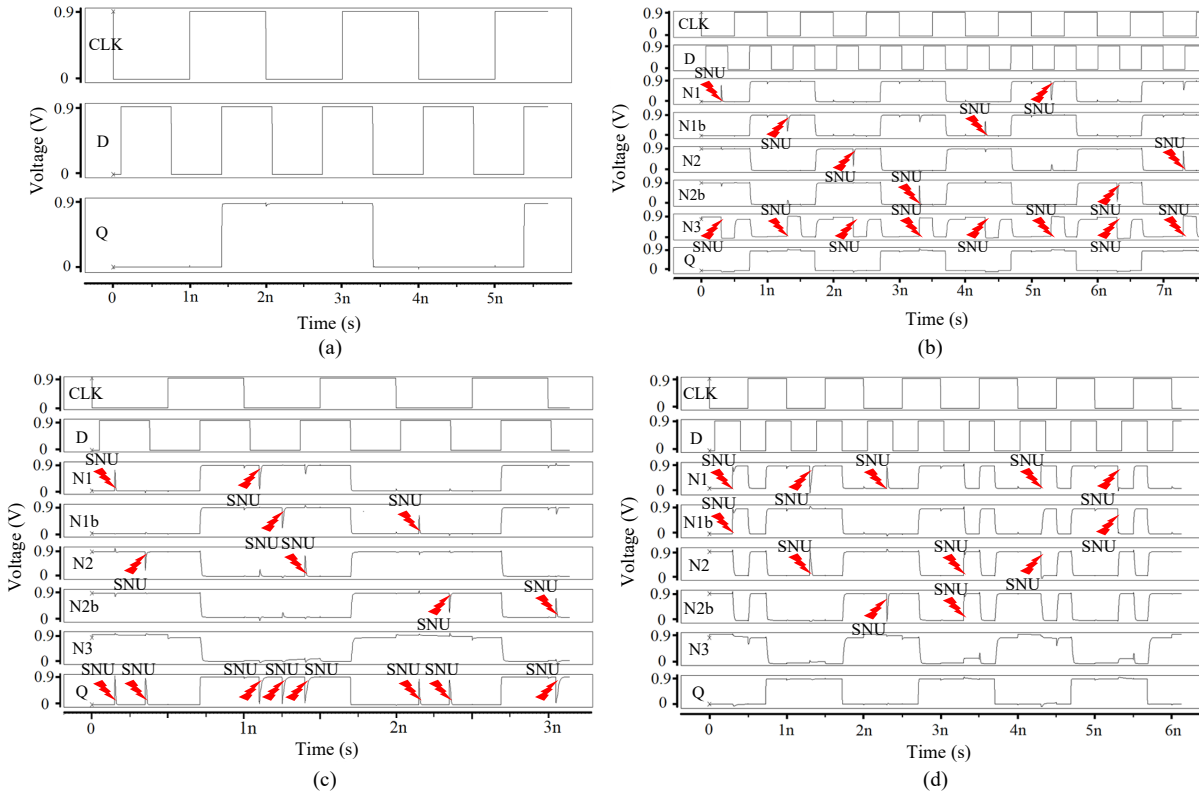


Fig. 5. Simulation waveforms for the proposed HLCRT latch design. (a) Error-free case (without fault injections), (b) DNU case with injections to N3 and an internal node of the DICE cell, (c) DNU case with injections to Q and an internal node of the DICE cell, (d) DNU case with injections to node-pairs in the DICE cell.

ue. In other words, the latch can correctly hold the stored value.

Let us now describe the fault-tolerance mechanism of the proposed latch in hold mode. Here we still consider the example of holding 0 by the latch (i.e., Q = N1 = N2 = 0). Let us first discuss the SNU tolerance of the latch. Since it is well known that the DICE cell is self-recoverable from any possible SNU, the SNU tolerance of the nodes in the DICE cell is omitted (related details can be found in [34]). Note that, when N2 is affected by an SNU, the error cannot propagate to N3 due to the node isolation using INV with CG. Therefore, only N3 and Q need to be discussed for SNU tolerance. In the case where N3 is affected by an SNU, N3 is flipped from 1 to 0. In this case, since the inputs of the CE become different, the CE will still have its previous value on Q (i.e., Q = 0) although N3 cannot self-recover from the SNU. In the case where Q is affected by an SNU, Q is temporally flipped from 0 to 1. In this case, since the inputs of the CE still have the original correct value (i.e., N1b = N2b = N3 = 1), the CE will still output the correct value (i.e., Q = 0, and Q can self-recover from the SNU). Therefore, the proposed HLCRT latch can tolerate any possible SNU. Note that for Q = N1 = N2 = 1, a similar scenario can be observed.

Let us now discuss the DNU tolerance of the latch. It is well known that the DICE cell cannot provide any-possible-DNU self-recoverability. This means that we have to consider the worst case where all nodes in the DICE cell are flipped when a node-pair in the DICE cell suffers from a DNU. It is obvious that the DICE cell has 6 node-pairs, i.e., <N1, N2>, <N1, N1b>, <N1, N2b>, <N2, N1b>, <N2, N2b>, and <N1b, N2b>. In the case where any of these node-pairs suffers from a DNU, N3 is not affected. In other words, all inputs of the CE are not simultaneously affected. Therefore, the CE can still have its previous value on Q although many of these node-pairs cannot self-recover from DNUs. Therefore, the latch is DNU tolerant for all above mentioned node-pairs.

Finally, we consider the case where one node inside the DICE cell together with another node outside the DICE cell is affected by a DNU. It is obvious that, outside the DICE cell, we only need to consider two nodes, i.e., N3 and Q. In the case where N3 together with any single node inside the DICE cell are affected by a DNU, the single node inside the DICE cell can self-recover to the correct state. However, N3 will still retain its flipped value. This means that the inputs of the CE become different. In this case, however, the CE still has its previous value on Q. Furthermore, in the case

where Q together with any single node inside the DICE cell are affected by a DNU, the single node inside the DICE cell can self-recover to the correct state. This means that the inputs of the CE will still have their previous values, making the CE still output its previous value on Q. In other words, any above mentioned node-pair can tolerate DNUs. Note that, if node-pair <N3, Q> is affected by a DNU, the latch cannot tolerate the DNU. In summary, the latch can tolerate SNUs and DNUs (except a DNU on node-pair <N3, Q>).

B. Robustness Assessment Results

The HLCRT latch was implemented in a commercial 32nm CMOS technology, the operational voltage was set to 0.9V, and pertinent simulations using Synopsys HSPICE were performed. The transistor sizes employed in the latch design are listed in the following. (a) For TG1 and TG2 that drive both the DICE cell and the inverter when the latch operates in transparent mode, as well as the normal input-split inverters inside the DICE cell and the CG-based inverter, the pMOS transistor had W/L = 128/32nm while the nMOS transistor had W/L = 45/32nm, (b) for the CG-based input-split inverters inside the DICE cell, and the 3-input CE, the pMOS transistors had W/L = 180/32nm while the nMOS transistors had W/L = 100/32nm, and (c) for TG3 that drives Q when the latch operates in transparent mode, the pMOS transistors had W/L =128/32nm while the nMOS transistors had W/L = 65/32nm.

Fig. 5 shows the simulation waveforms for the proposed HLCRT latch. In Fig. 5-(a), the error-free case (without fault injections) capturing input D and feeding output Q at the operational supply-voltage of 0.9V is shown. It can be seen from the simulation result that, the latch can correctly operate in transparent mode (D = Q) when CLK is high; the latch can correctly operate in hold mode (the previous D was kept on Q) when CLK is low. In other words, the operation of the HLCRT latch in normal modes is similar to that of a conventional unhardened latch.

In the following simulations, a controllable double exponential current source model was employed to simulate fault injections [24]. The worst case injected charge was chosen to be up to 45fC for a single node, which is large enough since we aimed at validating the circuit operation under extreme DNU conditions that disturb the nodes of the latch. The time constant values of the rise and fall of the current pulse were set to 0.1 and 3.0 ps, respectively. Fig. 5-(b) to (d) show the DNU injection simulation results for the HLCRT latch.

Fig. 5-(b) shows the simulation waveform of the proposed HLCRT latch with DNU injections when the latch operates in hold mode. In the DNU node-pairs, one node is N3 and another is an internal node of the DICE cell. At 0.3ns, 1.3ns, 2.3ns, and 3.3ns, a DNU was injected on the node-pairs <N1, N3>, <N1b, N3>, <N2, N3>, and <N2b, N3>, respectively. To ensure that any node was injected with an error no matter its original correct value is high or low, at 4.3ns, 5.3ns, 6.3ns, and 7.3ns, the supplemental injections on the node-pairs <N1b, N3>, <N1, N3>, <N2b, N3>, and <N2, N3> were performed, respectively. It can be seen from Fig. 5-(b) that only N3 inside these node-pairs cannot self-recover from the injected DNUs; however, the error is blocked by the 3-input CE, resulting in nearly no effect on Q, i.e., the latch still has its previous value on Q.

Fig. 5-(c) shows the simulation waveform of the proposed HLCRT latch with new DNU injections when the latch operates in hold mode. In the DNU node-pairs, one node is Q and another is an internal node of the DICE cell. All of the four single nodes inside the DICE cell were selected for fault injections. As shown in Fig. 5-(c), at 0.15ns, 1.25ns, 1.40ns, and 2.35ns, a DNU was injected on the node-pairs <N1, Q>, <N1b, Q>, <N2, Q>, and <N2b, Q>, respectively. To ensure that any node was injected with an error no matter its original correct value is high or low, at 0.35ns, 1.10ns, 2.15ns, and 3.10ns, the supplemental injections on the node-pairs <N2, Q>, <N1, Q>, <N1b, Q>, and <N2b, Q> were performed, respectively. It can be seen from Fig. 5-(c) that all of these nodes can self-recover from the injected DNUs, i.e., the latch still has its previous values on all nodes.

Fig. 5-(d) shows the simulation waveform of the proposed HLCRT latch with the last type of DNU injections when the latch operates in hold mode and each DNU node-pair is inside the DICE cell. As previously described, there are 6 node-pairs inside the DICE cell, i.e., <N1, N1b>, <N1, N2>, <N1, N2b>, <N1b, N2>, <N1b, N2b>, and <N2, N2b>. The four key/indicative node-pairs <N1, N1b>, <N1, N2>, <N1, N2b>, and <N2, N2b> were selected for fault injections. At 0.3ns, 1.3ns, 2.3ns, and 3.3ns, a DNU was injected on the node-pairs <N1, N1b>, <N1, N2>, <N1, N2b>, and <N2, N2b>, respectively. To ensure that any node was injected with an error no matter its original correct value is high or low, at 4.3ns and 5.3ns, the supplemental injections on the node-pairs <N1, N2> and <N1, N1b> were performed, respectively. It can be seen from Fig. 5-(d) that most of these nodes cannot self-recover from the injected DNUs. However, the retained errors can be blocked by the 3-input CE, resulting in nearly no effect on Q. Therefore, the above mentioned simulation results have validated the ability of the proposed HLCRT latch to provide fault tolerance against DNUs.

IV. Proposed HLCRT-FF Design

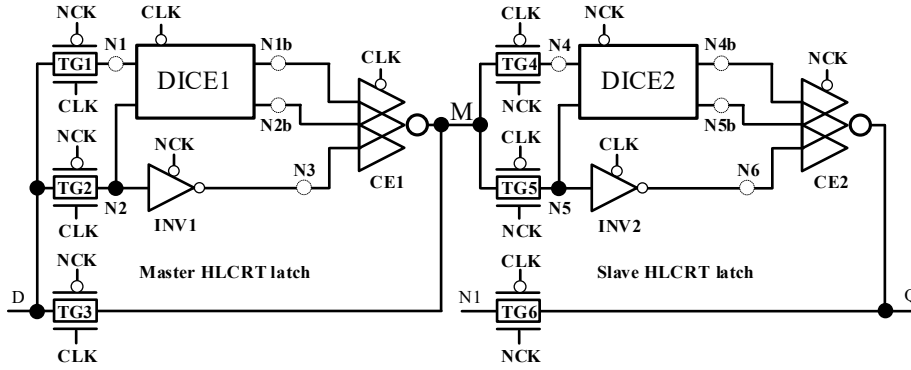


Fig. 6. Schematic of the proposed HLCRT-FF design.

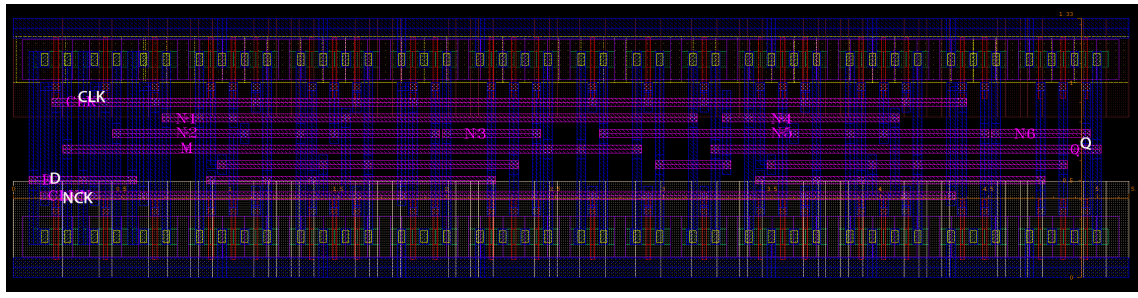


Fig. 7. Layout of the proposed HLCRT-FF design.

A. Circuit Schematic and Behavior

The schematic and layout of the proposed HLCRT-FF design are presented in Fig. 6 and Fig. 7, respectively. The HLCRT-FF is constructed from a master and a slave HLCRT latch that can tolerate SNUs and DNUs. In the FF structure, D is the input, Q is the output, and CLK and NCK are the system clock and negative system clock signals, respectively. Moreover, the output M of the master latch is connected to TG4 and TG5 of the slave latch and the node N1 of the master latch is connected to TG6 of the slave latch. The HLCRT-FF has four normal operational modes, which are discussed below.

During initialization, CLK = 1 and NCK = 0, the master latch works in transparent mode. Thus, N1, N2 and M can be initialized through three TGs (TG1, TG2 and TG3), and subsequently, the values of most nodes except N1b and N2b in the master latch can be determined. At this time, the slave latch does not receive any value from the master latch since the data-paths between the master and the salve latches are blocked through three TGs (TG4, TG5 and TG6) in the slave latch. Thus, the output Q of the FF does not receive any value.

When CLK switches to 0 and NCK switches to 1, three TGs (TG1, TG2, and TG3) in the master latch become OFF and the master latch switches into hold mode. Indeed, the master latch retains the initialized D-value since the feedback loops in DICE1 can be constructed. At this time, the value of M is determined by CE1 instead of TG3. The three TGs (TG4, TG5 and TG6) in the slave latch become ON and the slave latch switches into transparent mode. Thus, the value to be stored in the master latch propagates to the slave latch. The output Q directly receives the D-value to be stored in the master latch through a high-speed path (i.e., N1 → TG6 → Q).

When CLK = 0 and NCK = 1, the master latch works in hold mode and the slave latch works in transparent mode. At this time, the master latch cannot receive any new D-value, and node values of the slave latch (including the output Q) are determined by the stored value of the master latch. Thus, the output Q has the value of the stored value in the master latch.

When CLK switches to 1 and NCK switches to 0, the master latch switches into transparent mode and receives a new D-value. The slave latch switches into hold mode, and stores and outputs the previous D-value. Therefore, the output Q of the FF has the previous D-value.

Let us now describe the fault-tolerance mechanism of the proposed FF. It is clear that the operational modes of the master and the slave latches are equivalent when any of them works in hold mode. Thus, we mainly

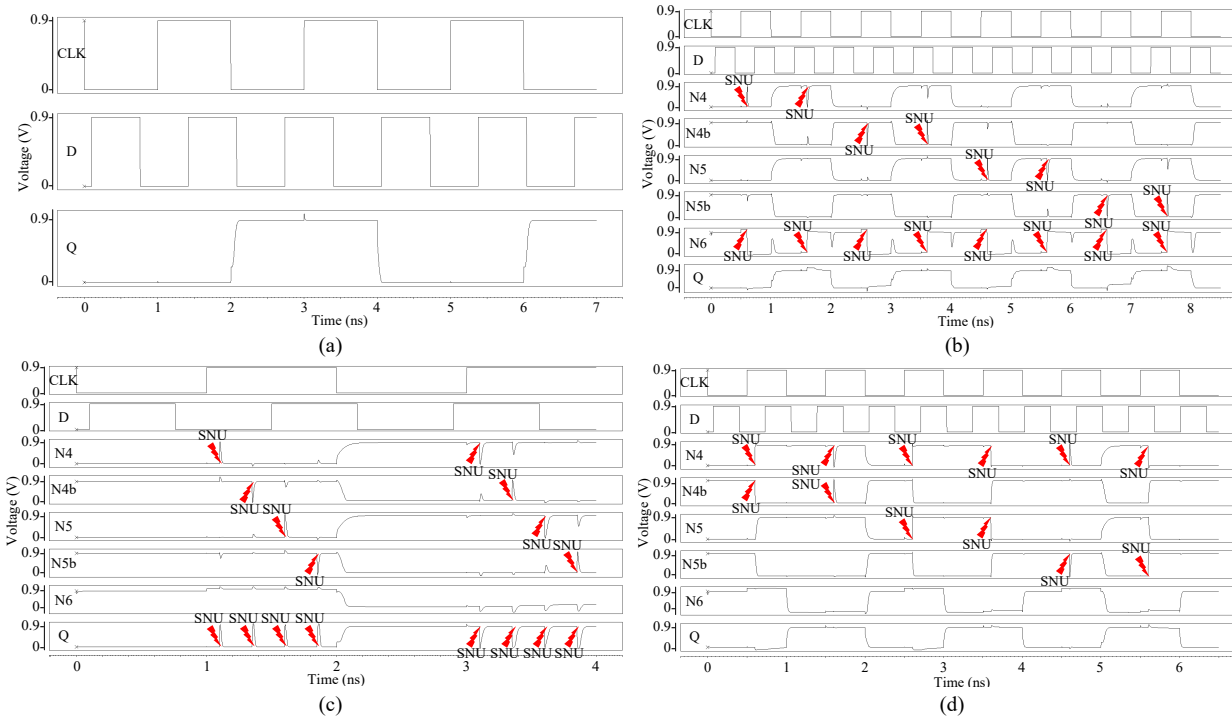


Fig. 8. Simulation waveforms for the proposed HLCRT-FF design. (a) Error-free case (without fault injections), (b) DNU case with injections to N6 and an internal node of the DICE cell, (c) DNU case with injections to Q and an internal node of the DICE cell, (d) DNU case with injections to node-pairs in the DICE cell.

select the slave latch to discuss the SNU and the DNU tolerance principles in its hold mode. First, the SNU tolerance of the FF is discussed. When the master latch works in transparent mode and the slave latch works in hold mode, the master latch can self-recover from any SNU since the master latch works in transparent mode and can receive a new D-value to be refreshed. It is clear that the slave latch can tolerate SNUs. Therefore, the HLCRT-FF can tolerate any SNU.

Next, the DNU tolerance of the FF is discussed. When the master latch works in transparent mode and the slave latch works in hold mode, the master latch can self-recover from any DNU since the master latch works in transparent mode and can receive a new D-value to refresh. It is clear that the slave latch can tolerate DNUs (except a DNU on node-pair <N6, Q>). Therefore, the HLCRT-FF can tolerate most DNUs (this is sufficient for low-orbit aerospace applications).

B. Robustness Assessment Results

The HLCRT-FF was implemented with the same parameters as those listed in Section III.B. Fig. 8 shows the simulation waveforms for the proposed HLCRT-FF. In Fig. 8-(a), the error-free case (without fault injections) capturing input D and feeding output Q at the operational supply-voltage of 0.9V is shown. Initially, as shown in Fig. 8-(a), when CLK = 1 and NCK = 0, the master latch works in transparent mode, the output Q and the input D were initialized to 0. When CLK switches to 0 and NCK switches to 1, the master latch switches into hold mode (it stores the D-value) and the slave latch switches into transparent mode. The value of the output Q is determined by the stored D-value in the master latch. When CLK = 0 and NCK = 1, the master latch works in hold mode and the slave latch works in transparent mode. The value of the output Q keeps the stored D-value in the master latch. When CLK switches to 1 and NCK switches to 0, the master latch switches into transparent mode (it receives a new D-value) and the slave latch switches into hold mode. The value of the output Q keeps the previous stored D-value in the slave latch. It can be seen from the simulation result in Fig. 8 that the FF can correctly operate in the four normal operational modes. Therefore, the normal operations of the HLCRT-FF are similar to those of the traditional unhardened FF.

In the following simulations, the same method and parameters as those described in Section 3.2 were used. There are totally only three cases such as the following that need to be verified for DNU tolerance.

Case 1: A DNU affects node N6 and an internal node of the DICE cell. The indicative node-pairs are <N4, N6>, <N4b, N6>, <N5, N6> and <N5b, N6>

Case 2: A DNU affects node Q and an internal node of the DICE cell. The indicative node-pairs are <N4, Q>, <N4b, Q>, <N5, Q> and <N5b, Q>.

Case 3: A DNU affects two nodes of the DICE cell. The indicative node-pairs are <N4, N4b>, <N4, N5>, and <N4, N5b>.

Fig. 8-(b) to (d) show the DNU injection simulation results for the proposed HLCRT-FF. Fig. 8-(b) shows the simulation waveform for the proposed HLCRT-FF with Case-1 DNU injections when the slave latch operates in hold mode. At 0.6ns, 2.6ns, 4.6ns, and 6.6ns, a DNU was injected on node-pairs <N4, N6>, <N4b, N6>, <N5, N6>, and <N5b, N6>, respectively. To ensure that any node was injected with an error no matter its original correct value is high or low, at 1.6ns, 3.6ns, 5.6ns, and 7.6ns, the supplemental injections on the node-pairs <N4, N5>, <N4b, N6>, <N5, N6>, and <N5b, N6> were performed, respectively. It can be seen from Fig. 8-(b) that, only N6 inside these node-pairs cannot self-recover from DNUs; however, the error is blocked by the 3-input CE, resulting in nearly no effect on Q, i.e., the FF still keeps its previous value on Q.

Fig. 8-(c) shows the simulation waveform for the proposed HLCRT-FF with Case-2 DNU injections when the slave latch operates in hold mode. As shown in Fig. 8-(c), at 1.10ns, 1.35ns, 1.60ns, and 1.85ns, a DNU was injected on node-pairs <N4, Q>, <N4b, Q>, <N5, Q>, and <N5b, Q>, respectively. To ensure that any node was injected with an error no matter its original correct value is high or low, at 3.10ns, 3.35ns, 3.60ns, and 3.85ns, the supplemental injections on node-pairs <N4, Q>, <N4b, Q>, <N5, Q>, and <N5b, Q> were performed, respectively. It can be seen from Fig. 8-(c) that all nodes can self-recover from the injected DNUs, i.e., the FF still keeps its previous values on all nodes.

Fig. 8-(d) shows the simulation waveform for the proposed HLCRT-FF with Case-3 DNU injections when the slave latch operates in hold mode. At 0.6ns, 2.6ns, and 4.6ns, a DNU was injected on node-pairs <N4, N4b>, <N4, N5>, and <N4, N5b>, respectively. To ensure that any node was injected with an error no matter its original correct value is high or low, at 1.6ns, 3.6ns and 5.6ns, the supplemental injections on node-pairs <N4, N4b>, <N4, N5>, and <N4, N5b> were performed, respectively. It can be seen from Fig. 8-(d) that most of these nodes cannot self-recover from the injected DNUs. However, the retained errors can be blocked by the 3-input CE, resulting in nearly no effect on Q, i.e., the FF still keeps its previous value on Q. Therefore, the above mentioned simulation results and discussions validate the ability of the proposed HLCRT-FF to provide fault tolerance against DNUs.

V. Comparison and Evaluation Results

To make a fair comparison, the latch designs HPST [8], HLR [9], FERST [10], CLCT [23], DNCSST [24], DeltaDICE [25], DNURL [3], and SEDUFT [38] were designed under the same conditions as those of the proposed HLCRT latch. Table I shows the detailed comparison results for the above-mentioned SNU and/or DNU hardened latch designs, including the proposed HLCRT latch, in terms of D to Q transmission delay, average power dissipation (dynamic and static), silicon area, and *delay-power-area product* (*DPAP*) calculated by multiplying delay, power, and area. The silicon area of these latch designs was also measured as in [32] for a fair comparison. It is obvious that, a smaller DPAP is better as for the same type of latch designs (e.g., the DNU hardened type), since the overall overhead of this type of latch designs is small.

Table I
Comparison results for the SNU and/or DNU hardened latch designs

Latch	SNU Tolerant?	DNU Tolerant?	Delay (ps)	Power (μW)	10^{-4}×Area (nm^2)	10^{-2}× DPAP
HPST [8]	Yes	No	2.14	0.51	10.90	0.12
HLR [9]	Yes	No	2.12	0.38	9.04	0.07
FERST [10]	Yes	No	85.65	1.41	11.09	13.39
CLCT [23]	Yes	Yes	31.98	0.70	12.41	2.78
DNCSST [24]	Yes	Yes	69.71	1.65	16.16	18.59
DeltaDICE [25]	Yes	Yes	10.08	0.85	17.95	1.54
DNURL [3]	Yes	Yes	5.47	1.81	26.55	2.63
SEDUFT [38]	Yes	Yes	1.69	1.23	11.25	0.23
HLCRT (Proposed)	Yes	Yes	2.14	0.60	11.10	0.14

Table II
Comparison results for the SNU and/or DNU hardened latch designs

Latch	ΔDelay (%)	ΔPower (%)	ΔArea (%)	ΔDPAP (%)
CLCT [23]	93.31	14.29	10.56	94.96
DNCSST [24]	96.93	63.64	31.31	99.25
DeltaDICE [25]	78.77	29.41	38.16	90.91
DNURL [3]	60.88	66.85	58.19	94.68
SEDUFT [38]	-26.63	51.22	1.33	39.13
Average	60.65	45.08	27.91	83.79

It can be seen from Table I that, compared to the SNU hardened latch designs, i.e., the first three designs (HPST, HLR, and FERST), the transmission delay of the proposed HLCRT latch is not as small as that of the HPST and HLR, the power dissipation and silicon area of the proposed HLCRT latch are not as small as those

of the HLR. However, the HPST, HLR, including the FERST latches, are not DNU hardened at all. Furthermore, compared with the 4th to 8th DNU tolerant latches, i.e., the CLCT, DNCSST, DeltaDICE, DNURL, and SEDUFT, the overhead of the proposed HLCRT latch is the smallest for the power dissipation, silicon area, and DPAP product, which can effectively validate the cost-effectiveness of the proposed HLCRT latch.

To make a further detailed quantitative comparison, the relative overhead in terms of delay (ΔDelay), power (ΔPower), area (ΔArea), and DPAP (ΔDPAP) among the DNU hardened latches compared with the proposed HLCRT latch was calculated with Eq. (1). Table II shows the relative overhead of the DNU hardened latches compared with the proposed HLCRT latch.

$$\Delta = [(\text{Compared} - \text{Proposed}) / \text{Compared}] \times 100\% \quad (1)$$

It can be seen from Eq. (1) that a positive percentage in Table II means that the overhead of the proposed HLCRT latch is smaller than that of the compared latches. Conversely, a negative percentage means that the overhead of the proposed HLCRT latch is larger than that of the compared latches.

It can be seen from Table II that all percentages are positive, which means that the overhead of the proposed HLCRT latch is small for all aspects of overhead. Furthermore, it can also be seen that the proposed HLCRT latch can save about 60.65% of transmission delay, 45.08% of power dissipation, 27.91% of silicon area, and 83.79% of DPAP on average. Therefore, the proposed HLCRT latch is cost-effective compared with the same type of latches.

Moreover, the FF designs, such as HPST-FF, HLR-FF, FERST-FF, CLCT-FF, DNCSST-FF, DeltaDICE-FF, DNURL-FF, and SEDUFT-FF were also implemented/designed under the same conditions as those of the proposed HLCRT-FF. Table III shows the detailed comparison results for these above mentioned SNU and/or DNU hardened FF designs, including the proposed HLCRT-FF, in terms of CLK to Q transmission delay, average power dissipation (dynamic and static), silicon area, and DPAP.

It can be seen from Table III that, compared to the SNU hardened FF designs, i.e., the first three designs (HPST, and HLR and FERST), the power dissipation of the proposed HLCRT-FF is not as small as that of the HPST-FF and the HLR-FF, the silicon area of the proposed HLCRT-FF are not as small as that of the above three. However, the first three latches are not DNU hardened at all. Furthermore, compared with the 4th to 8th DNU tolerant FFs, i.e., the CLCT-FF, DNCSST-FF, DeltaDICE-FF, DNURL-FF and SEDUFT-FF, the overhead of the proposed HLCRT-FF is the smallest for the transmission delay, power dissipation, silicon area, and DPAP product, which can effectively validate the cost-effectiveness of the proposed HLCRT-FF.

TABLE III
RELATIVE OVERHEAD OF THE DNU HARDENED FF DESIGNS COMPARED WITH THE PROPOSED FF DESIGN

FF	SNU Tolerant?	DNU Tolerant?	Delay (ps)	Power (μW)	10^{-4}×Area (nm^2)	10^{-2}× DPAP
HPST-FF	Yes	No	26.98	1.56	21.79	8.96
HLR-FF	Yes	No	28.53	1.26	18.08	6.39
FERST-FF	Yes	No	85.29	3.31	22.18	58.63
CLCT-FF	Yes	Yes	71.52	2.44	24.83	38.81
DNCSST-FF	Yes	Yes	70.77	4.48	32.32	90.66
DeltaDICE-FF	Yes	Yes	89.82	3.50	35.90	110.21
DNURL-FF	Yes	Yes	47.09	5.35	53.10	130.64
SEDUFT-FF	Yes	Yes	45.17	3.78	22.51	38.43
HLCRT-FF (Proposed)	Yes	Yes	4.80	1.65	22.20	1.76

TABLE IV
RELATIVE OVERHEAD OF THE DNU HARDENED FF DESIGNS COMPARED WITH THE PROPOSED FF DESIGN

FF	ΔDelay (%)	ΔPower (%)	ΔArea (%)	ΔDPAP (%)
CLCT-FF	93.29	32.38	10.59	95.51
DNCSST-FF	93.22	63.17	31.31	98.06
DeltaDICE-FF	94.66	52.86	38.16	98.40
DNURL-FF	89.81	69.16	58.10	98.56
SEDUFT-FF	89.37	56.35	1.38	95.42
Average	92.07	54.78	27.91	97.21

Table IV shows the relative overhead of the DNU hardened FFs compared to the proposed HLCRT-FF. It can be seen from Table IV that all percentages are positive, which means that the overhead of the proposed HLCRT-FF is small for all aspects of overhead. Furthermore, it can also be seen that the proposed HLCRT-FF can save about 92.07% of transmission delay, 54.78% of power dissipation, 27.91% of silicon area, and 97.21% of DPAP on average. Therefore, the proposed HLCRT-FF is cost-effective compared with the same type of FFs. In summary, the proposed HLCRT latch and HLCRT-FF are not only reliable but also cost-effective, and thus they are suitable for low-orbit aerospace applications that require both high reliability and cost-effectiveness.

Readers of this paper may be aware that the nodes such as N3 and Q can enter into high impedance state when the proposed structure works in hold mode. We take N3 for an example. When N3 switches into high impedance state, because N1b and N2b can always feed the other inputs of the CE, the CE can temporarily have

the original correct value at its output. Especially, if the latch works in a high frequency, the clock period is short so that N3 has no time to float to an undetermined value. Meanwhile, the proposed structure has a small delay. Therefore, the proposed structure is suitable for high performance applications as well.

Moreover, impacts of *process, voltage, and temperature* (PVT) variations on FFs are also considered, because FFs are more sensitive to PVT variations especially in nano-scale CMOS technologies. Note that, latches are mainly used to construct FFs, so that the PVT variations on FFs instead of latches are performed in this paper. Figures 9 to 12 show the estimation results of the temperature and supply voltage variation impacts on delay (i.e., CLK-to-Q delay) and power for FFs. Note that, the temperature ranges from -25℃ to 125℃, and the supply voltage ranges from 0.75V to 1.05V.

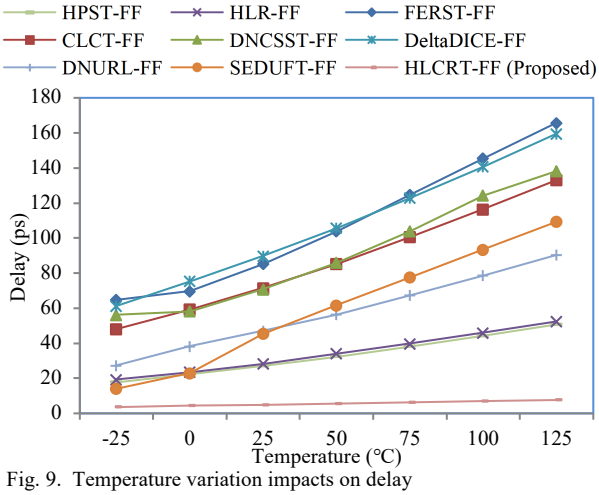


Fig. 9. Temperature variation impacts on delay

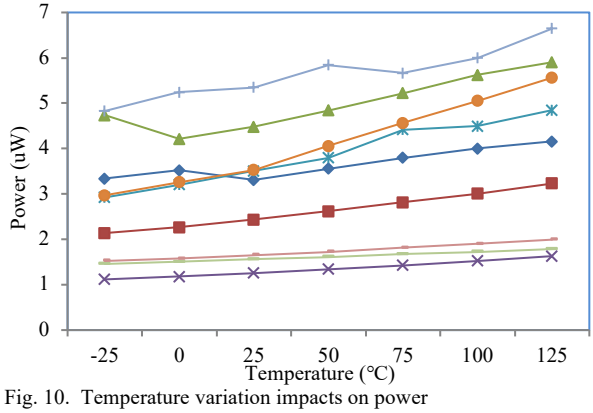


Fig. 10. Temperature variation impacts on power

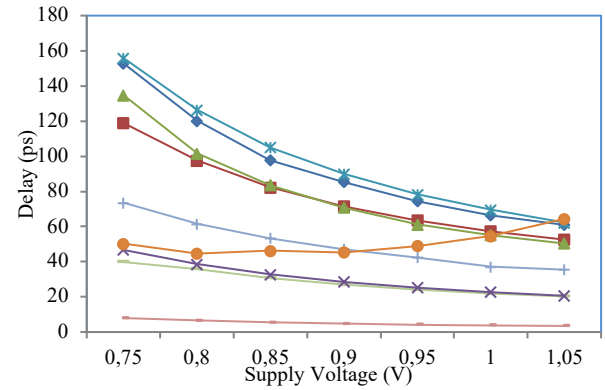


Fig. 11. Supply voltage variation impacts on delay

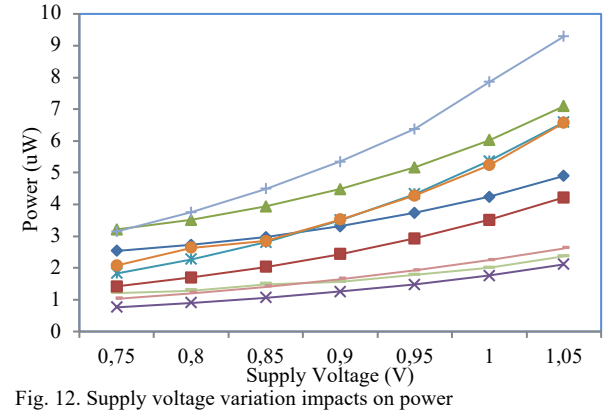


Fig. 12. Supply voltage variation impacts on power

It can be seen from Fig. 9 that most state-of-the-art FFs are sensitive to temperature variations on delay. However, the proposed HLCRT-FF is less insensitive to temperature variations on delay. It can be seen from Fig. 10 that some FFs (such as the bottom three) are less sensitive to temperature variations on power. Figures 9 and 10 generally indicate that delay and power increase with the increasing temperature. The main reason is the decrease of carrier mobility when the temperature is increasing [39].

It can be seen from Fig. 11 that the DeltaDICE-FF is the most sensitive to supply voltage variations on delay since there are much current competition on the path from D to Q. However, the proposed HLCRT-FF is less sensitive to supply voltage variations on delay mainly because there is a high-speed path from D to Q. Figure 11 generally indicates that delay decreases with the increasing supply voltage. Obviously, high supply voltage can generally drive devices fast. It can be seen from Fig. 12 that the power of all FFs increases when the supply voltage increases, since the power dissipation quadratically depends on the supply voltage [39].

To investigate the process variation effect on FFs, Monte Carlo simulations were performed using the PVT estimation methodologies [32]. The threshold

voltage and oxide thickness of transistors are generated randomly using the normal distribution with ±5% maximum deviations from the original [32]. Note that, the negative varied values (less than the original ones) on the normal distribution curves for the effective channel length of transistors are mapped to positive ones by coordinate transformation in the HSPICE netlist file, since these variations are almost impossible [32]. To get parameters of average deviation (dev) and standard deviation (σ) for FFs, 500 times' Monte Carlo simulations were performed, and the calculation formulas for these parameters are given in the following.

$$dev = \frac{\sum|X_i - \varphi|}{N} \quad (1)$$

$$\sigma = \sqrt{\frac{\sum(X_i - \varphi)^2}{N}} \quad (2)$$

In Eq. (1)-(2), N, Xi and φ denote, respectively, the number of sample values (equal to 500), the sample values and the standard value (equal to 1 due to the normalization). Accordingly, the normalized average deviation (dev) and standard deviation (σ) for power and delay of FFs are calculated and shown in Table V.

TABLE V
NORMALIZED AVERAGE DEVIATION (DEV) AND STANDARD DEVIATION (Σ) FOR POWER AND DELAY OF FFS

FF	dev		σ	
	power	delay	power	Delay
HLCRT-FF (Ours)	1.00	1.00	1.00	1.00
HPST-FF [8]	0.93	1.03	0.97	1.06
HLR-FF [9]	0.97	1.09	1.00	1.14
FERST-FF [10]	1.43	3.08	1.45	3.12
CLCT-FF [23]	1.54	2.01	1.57	2.00
DNCSST-FF [24]	2.94	1.98	2.97	2.03
DeltaDICE-FF [25]	2.37	3.01	2.43	3.03
DNURL-FF [3]	3.06	1.36	3.11	1.40
SEDUFT-FF [38]	2.91	1.53	2.95	1.57

From Table V, in terms of power, three conclusions can be drawn. First, compared with the proposed HLCRT-FF, all the compared FFs have a larger sensitivity to the process variation effect on power (except for the HPST-FF and HLR-FF), which is mainly due to the increased area for hardening. Second, the DNURL-FF has the largest sensitivity to the process variation effect on power mainly since its area is the largest. Third, the HPST-FF and HLR-FF have a similar-and-lower sensitivity to the process variation effect for power, compared with most of the other hardened FFs. From Table V, in terms of delay, three conclusions can be drawn. First, compared with the proposed HLCRT-FF, the HPST-FF and HLR-FF have a lower sensitivity to the process variation effect on delay, which is mainly due to the employment of the high-speed transmission path. Second, the FERST-FF has the largest sensitivity to the process variation effect on delay, which is mainly because there are many devices from D to Q. Third, the HPST-FF and HLR-FF have a lower sensitivity to the process variation effect on delay, compared with most of the other hardened FFs. In summary, the proposed HLCRT-FF has a moderate sensitivity on the PVT variation effects, compared with most of the state-of-the-art hardened FFs.

VI. CONCLUSION AND FURTHER WORK

In this paper, a cost-effective and radiation hardened latch and a corresponding FF have been proposed. Using the error masking mechanism of the C-element, the proposed latch and FF are effectively DNU hardened. Moreover, employing fewer transistors, clock-gating, and a high-speed path from the input to the output, the proposed latch has low overhead. The proposed FF also has low overhead since it is mainly constructed from the proposed latch. Simulation results have clearly demonstrated the DNU tolerance and cost-effectiveness of the proposed latch and FF, making the latch and FF widely applicable to low-orbit aerospace applications that require both high reliability and cost-effectiveness.

Readers of this paper may be aware that the schematic simulations are not sufficient for this kind of design, since the charge sharing between nodes can be complicated. Therefore, in our further work, the design will be tested with ion experiments, or at least some TCAD simulations.

ACKNOWLEDGMENT

The corresponding author is Tianming Ni. This work was supported in part by the National Natural Science Foundation of China under Grants 61974001, 61874156, and 61904001, and Anhui University Doctor Startup Fund (Y040435009). This research was also supported in part by the NSFC-JSPS Exchange Program under Grant 6201101398.

REFERENCES

[1] A. Yan, Z. Wu, L. Lu, Z. Chen, J. Song, Z. Ying, P. Girard, and X. Wen, "Novel Radiation Hardened Latch Design with Cost-Effectiveness for Safety-Critical Terrestrial Applications," Proc. IEEE Asian Test Symposium, pp. 43-48, Kolkata, India.

[2] A. Yan, Z. Wu, L. Lu, Z. Chen, J. Song, Z. Ying, P. Girard, and X. Wen, "Radiation-Hardened 14T SRAM Bitcell with Speed and Power Optimized for Space Application," IEEE Transac-

tions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 2, pp. 407-415, 2019.
[3] A. Yan, Z. Huang, M. Yi, X. Xu, Y. Ouyang, and H. Liang, "Double-Node-Upset-Resilient Latch Design for Nanoscale CMOS Technology," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 6, pp. 1978-1982, 2017.
[4] D. Mavis and P. Eaton, "SEU and SET Modeling and Mitigation in Deep Submicron Technologies," Proc. IEEE International Reliability Physics Symposium, Phoenix, USA, pp. 293-305, 2007.
[5] C. Peng, S. Xiao, W. Lu, J. Zhang, X. Wu, J. Chen, and Z. Lin, "Average 7T1R Nonvolatile SRAM With R/W Margin Enhanced for Low-Power Application," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 26, no. 3, pp. 584-588, 2018.
[6] Y. Li, H. Wang, R. Liu, Chen, I. Nofal, S. Shi, A. He, G. Guo, S. Baeg, S. Wen, R. Wong, M. Chen, and Q. Wu, "A Quatro-Based 65 nm Flip-Flop Circuit for Soft-Error Resilience," IEEE Transactions on Nuclear Science, vol. 64, no. 6, pp. 1554-1561, 2017.
[7] Y. Li, H. Wang, R. Liu, L. Chen, I. Nofal, Q. Chen, A. He, G. Guo, S. Baeg, S. Wen, R. Wong, Q. Wu, and M. Chen, "A 65 nm Temporally Hardened Flip-Flop Circuit," IEEE Transactions on Nuclear Science, vol. 63, no. 6, pp. 2934-2940, 2016.
[8] Z. Huang, "A High Performance SEU Tolerant Latch for Nanoscale CMOS Technology," Proc. IEEE Design Automation Test in Europe, Dresden, Germany, pp. 1-5, 2014.
[9] H. Nan, and K. Choi, "High Performance, Low Cost, and Robust Soft Error Tolerant Latch Designs for Nanoscale CMOS Technology," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, 1no. 7, pp. 445-1457, 2012.
[10] M. Fazeli, S. Miremadi, A. Ejlali, and A. Patooghy, "Low Energy Single Event Upset/Single Event Transient-Tolerant Latch for Deep Submicron Technologies," IET Computers & Digital Techniques, vol. 3, no. 3, pp. 289-303, 2009.
[11] S. Mitra, M. Zhang, N. Seifert, T. Mak, and K. Kim, "Built-in Soft Error Resilience for Robust System Design," Proc. IEEE International Conference on IC Design and Technology, Austin, USA, pp. 1-6, 2007.
[12] M. Omana, D. Rossi, and C. Metra, "High-Performance Robust Latches," IEEE Transactions on Computers, vol. 59, no. 11, pp. 1455-1465, 2010.
[13] S. Lin, Y. Kim, F. Lombardi, "Design and Performance Evaluation of Radiation Hardened Latches for Nanoscale CMOS," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 7, pp. 1315-1319, 2011.
[14] X. She, N. Li, J. Tong, "SEU Tolerant Latch Based on Error Detection," IEEE Transactions on Nuclear Science, vol. 59, no. 1, pp. 211-214, 2012.
[15] H. Nan and K. Choi, "Low Cost and Highly Reliable Hardened Latch Design for Nanoscale CMOS Technology," Microelectronics Reliability, vol. 52, pp. 1209-1214, 2012.
[16] Z. Huang, H. Liang, and S. Hellebrand, "A High Performance SEU Tolerant Latch," Journal of Electronics Testing, vol. 31, pp. 349-359, 2015.
[17] A. Yan, H. Liang, Z. Huang, C. Jiang, and M. Yi, "A Self-Recoverable, Frequency-Aware and Cost-Effective Robust Latch Design for Nanoscale CMOS Technology," IEICE Transactions on Electronics, vol. E98-C, no. 12, 1171-1178, 2015.
[18] C. Qi, L. Xiao, and J. Guo, "Low Cost and Highly Reliable Radiation Hardened Latch Design in 65 nm CMOS Technology," Microelectronics Reliability, vol. 55, pp. 863-872, 2015.
[19] K. Katsarou and Y. Tsiatouhas, "Soft Error Interception Latch: Double Node Charge Sharing SNU Tolerant Design," Electronics Letters, vol. 51, no. 4, 330-332, 2015.
[20] Y. Li, H. Wang, S. Yao, X. Yan, Z. Gao, and J. Xu, "Double Node Upsets Hardened Latch Circuits," Journal of Electronics Testing, vol. 31, pp. 537-548, 2015.
[21] N. Eftaxiopoulos, N. Axelos, and K. Pekmestzi, "DONUT: A Double Node Upset Tolerant Latch," Proc. IEEE Annual Symposium on VLSI, Montpellier, France, pp. 509-514, 2015.
[22] K. Namba, M. Sakata, and H. Ito, "Single Event Induced Double Node Upset Tolerant Latch," Proc. IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, Kyoto, Japan, pp. 280-288, 2010.
[23] X. Hui and Z. Yun, "Circuit and Layout Combination Technique to Enhance Multiple Nodes Upset Tolerance in Latches," IEICE Electronics Express, vol. 12, no. 9, pp. 1-7, 2015.
[24] K. Katsarou and Y. Tsiatouhas, "Double Node Charge Sharing SEU Tolerant Latch Design," Proc. IEEE International Symposium on On-Line Testing and Robust System Design, Platja d'Aro, Spain, pp. 122-127, 2014.
[25] N. Eftaxiopoulos, N. Axelos, G. Zervakis, K. Tsoumanis, and K. Pekmestzi, "Delta DICE: A Double Node Upset Resilient Latch," Proc. IEEE International Midwest Symposium on Circuits and Systems, Fort Collins, USA, pp. 1-4, 2015.
[26] A. Yan, K. Yang, Z. Huang, J. Zhang, J. Cui, X. Fang, M. Yi, and X. Wen, "A Double-Node-Upset Self-Recoverable Latch Design for High Performance and Low Power Application," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 2, pp. 287-291, 2019.
[27] A. Watkins and S. Tragouodas, "A Highly Robust Double Node Upset Tolerant Latch," Proc. IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, Storrs, USA, pp. 15-20, 2016.
[28] J. Jiang, Y. Xu, J. Ren, W. Zhu, D. Lin, J. Xiao, W. Kong, and S. Zou, "Low-Cost Single Event Double-Upset Tolerant Latch Design," Electronics Letters, vol. 54, no. 9, pp. 554-556, 2018.
[29] H. Li, L. Xiao, and C. Qi, "High Robust and Cost Effective Double Node Upset Tolerant Latch Design for Nanoscale CMOS Technology," Microelectronics Reliability, vol. 93, pp. 89-97, 2019.
[30] R. Ramin, "Single Event Double Node Upset Tolerance in MOS/Spintronic Sequential and Combinational Logic Circuits," Microelectronics Reliability, vol. 69, pp. 109-114, 2017.
[31] A. Watkins and S. Tragouodas, "Radiation Hardened Latch Designs for Double and Triple Node Upsets," IEEE Transactions on Emerging Topics in Computing, vol. 99, pp. 1-10, 2017.
[32] A. Yan, L. Lai, Y. Zhang, J. Cui, Z. Huang, J. Song, J. Guo, and X. Wen, "Novel Low Cost, Double-and-Triple-Node-Upset-Tolerant Latch Designs for Nano-scale CMOS," IEEE Transactions on Emerging Topics in Computing, vol. 99, pp. 1-14, 2018.
[33] D. Lin, Y. Xu, X. Li, X. Xie, J. Jiang, J. Ren, H. Zhu, Z. Zhang, and S. Zou, "A Novel Self-Recoverable and Triple Nodes Upset Resilience DICE Latch," IEICE Electronics Express, vol. 15, no. 19, pp. 1-10, 2018.
[34] T. Calin, M. Nicolaidis, and R. Velazco, "Upset Hardened Memory Design for Submicron CMOS Technology," IEEE Transactions on Nuclear Science, vol. 43, no. 6, pp. 2874-2878, 1996.
[35] R. Yamamoto, C. Hamanaka, J. Furuta, K. Kobayashi, and H. Onodera, "An Area-Efficient 65 nm Radiation-Hard Dual-Modular Flip-Flop to Avoid Multiple Cell Upsets," IEEE Transactions on Nuclear Science, vol. 58, no. 6, pp. 3053-3059, 2011.
[36] G. Jaya, S. Chen, and S. Liter, "A Dual Redundancy Radiation-Hardened Flip-Flop Based on C-element in 65nm Process," Proc. IEEE International Symposium on Integrated Circuits, Singapore, pp. 1-4, 2016.

[37] F. Alghareb and R. DeMara, "Design and Evaluation of DNU-Tolerant Registers for Resilient Architectural State Storage," Proc. ACM Great Lakes Symposium on VLSI, Washington, USA, pp. 1-4, 2019.
[38] H. Zhang, Z. Liu, J. Jiang, J. Xiao, Z. Zhang, and S. Zou, "High-Performance and Single Event Double-Upset-Immune Latch Design," Electronics Letters, vol. 56, no. 23, pp. 1243-1245, 2020.
[39] Z. Huang, H. Liang, and S. Hellebrand, "A High Performance SNU Tolerant Latch," Journal of Electronic Testing, vol. 31, no. 4, pp. 349-359, 2015.

Aibin Yan received the Ph. D degree in Computer Application Technology from Hefei University of Technology, and received the M.S. degree in Software Engineering from the University of Science and Technology of China (USTC), Hefei, in 2015 and 2009, respectively. In 2016, he joined Anhui University, and currently he is an associate professor. His research interests mainly include radiation hardening for CMOS ICs such as latches, flip-flops, and memory cells.

Aoran Cao is with the School of Computer Science and Technology, Anhui University, Hefei, Anhui, China. Currently, he is pursuing his M.S. degree for computer technology major in Anhui University. He received his B.E degree from Hebei North College in 2019. His research interests include radiation hardening by design for nano-scale CMOS ICs such as latches, flip-flops, and SRAMs.

Zhelong Xu is with the School of Computer Science and Technology, Anhui University, Hefei, Anhui, China. Currently, he is pursuing his M.S. degree for computer technology major in Anhui University. He received his B.E degree from Anhui University in 2019. His research interests include radiation hardening by design for nano-scale CMOS ICs such as latches, flip-flops, and SRAMs.

Tianming Ni received a Ph.D. degree from Hefei University of Technology, Hefei, China, in 2018. He joined the College of Electrical Engineering, Anhui Polytechnic University in 2018. His research interest includes built-in-self-test, design automation of digital systems, design for IC reliability, 3D IC test and fault tolerance.

Patrick Girard (Fellow, IEEE) received a M.Sc. degree in Electrical Engineering and a Ph.D. degree in Microelectronics from the University of Montpellier, France, in 1988 and 1992 respectively. He is currently Research Director at CNRS (French National Center for Scientific Research) and works in the Microelectronics Department of the Laboratory of Informatics, Robotics and Microelectronics of Montpellier (LIRMM) - France. From 2010 to 2014, he was head of this Microelectronics Department. He is co-Director of the International Associated Laboratory « LAFISI » (French-Italian Research Laboratory on Hardware-Software Integrated Systems) created in 2013 by the CNRS and the University of Montpellier with the Politecnico di Torino, Italy. His research interests include all aspects of digital testing and memory testing, with emphasis on critical constraints such as timing and power. Reliability and fault tolerance are also part of his research activities. He is an Associate Editor of the IEEE Transactions on Aerospace & Electronic Systems, IEEE Transactions on Emerging Topics in Computing, and the Journal of Electronic Testing (JETTA - Springer). He has supervised 40 PhD dissertations and has published 7 books or book chapters, 80 journal papers, and more than 250 conference and symposium papers on these fields. Patrick Girard is a Fellow of the IEEE.

Xiaoqing Wen (Fellow, IEEE) received the B.E. degree from Tsinghua University, China, in 1986, the M.E. degree from Hiroshima University, Japan, in 1990, and the Ph.D. degree from Osaka University, Japan, in 1993. From 1993 to 1997, he was an Assistant Professor at Akita University, Japan. He was a Visiting Researcher at University of Wisconsin, Madison, USA, from Oct. 1995 to Mar. 1996. He joined SynTest Technologies, Inc., USA, in 1998, and served as its Chief Technology Officer until 2003. In 2004, he joined Kyushu Institute of Technology, Japan, where he is currently a Professor of the Department of Creative Informatics. He founded Dependable Integrated Systems Research Center in 2015 and served as its Director until 2017. His research interests include VLSI test, diagnosis, and testable design. He co-authored and co-edited two books: VLSI Test Principles and Architectures: Design for Testability (Morgan Kaufmann, 2006) and Power-Aware Testing and Test Strategies for Low Power Devices (Springer, 2009). He holds 43 U.S. Patents and 14 Japan Patents on VLSI testing. He received the 2008 IEICE-ISS Best Paper Award for his pioneering work on X-filling-based low-capture-power test generation. He is a Fellow of the IEEE, a Senior Member of the IEICE, and a Senior Member of the IPSJ. He is serving as associate editors for IEEE Trans. VLSI and the Journal of Electronic Testing: Theory and Applications.