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Syed Farah Naz[1], Ambika Prasad Shah[1], Suhaib Ahmed[2], Patrick Girard[3] and Michael Waltl[4]

[1]Discipline of Electrical Engineering, Indian Institute of Technology Jammu, J&K 181221, India

[2]Department of ECE, BGSB University Rajouri, J&K 185234, India [3]LIRMM, University of Montpellier / CNRS, Montpellier, France

[4]Institute for Microelectronics, TU Wien, Austria

***Abstract*—In this paper, a new XOR gate is discussed in quantum-dot cellular automata (QCA). The proposed gate is a single layer structure with no crossovers, and has been designed with redundant cells to increase the amplitude of the output signal and to improve the fault tolerance and reliability of the circuit. Based on the performance comparison, the investigated XOR gate has very high fault tolerance to single-cell addition and single-cell omission defects, thereby making them suitable candidates for designing reliable QCA based digital circuits.**

***Index Terms*—Quantum dot cellular automata, fault tolerant design, XOR gate, nanoelectronics.**

I. Introduction

QUANTUM dot cellular automata (QCA) provide high logic device density, small size, and ultra-low power dissipation in the nano regime while operating at high frequencies (in the range of few THz), which makes it an emerging technology for the design of digital circuits. They are especially advantegous in the sub nano regime where the established CMOS technology faces its limitations. Over the last decade, QCA has been exhaustively used to design various logic circuits with improved performance [1][2].

Instead of the traditional operation of MOS transistors, QCA operates on the principle of the cell to cell interaction [3]. A cell consists of four quantum dots wherein two electrons reside in diagonal positions with minimum electrostatic repulsion. This leads to two possible polarization states which are considered as binary 0 and binary 1, as shown in Fig. 1(a). These cells, when connected together in series, form a binary wire, as shown in Fig. 1(b), which is used for transmission of information. The polarity of a cell is decided by its neighboring cells. For proper routing of information, QCA has four clock zones, i.e. zone 0 through 3, where each zone has a phase difference of 90° compared to the previous clock zone, as shown in Fig. 1(b).

Amongst other logic operations the XOR gate is vital for designing of various digital circuits. The XOR gate has a logic high output only when the two inputs are different. The input-output relation of XOR logic is not linearly separable. Thus, it becomes pertinent to have an efficient XOR gate design to not impede the logic of circuits designed afterward using the same XOR design in addition to other logic gates [4].

II. Proposed XOR Gate

The proposed two-input XOR gate based on QCA, shown in Fig. 1(c), is a single layer structure designed using 135 cells occupying a cell area of 0.0437 μm^2 and total area of 0.1182 μm^2 with a latency of 2 clock cycles and no crossovers.

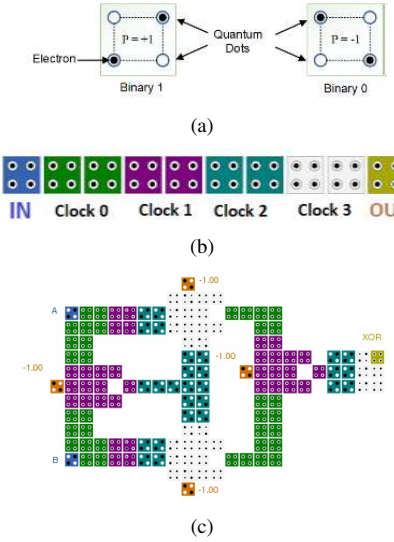


Fig. 1. Illustration of (a) QCA cells with two possible polarization states (b) binary wire depicting various clock zones of QCA. (c) Schematic of QCA based proposed two input XOR gate.

It uses 4 constant inputs with fixed polarization of '-1.00' (depicting binary 0). Here the output is obtained by one cell influencing the other, i.e. by cell level methodology. The XOR gate operates on the phenomenon of a cell to cell interaction, and the output cell polarity is achieved as either 1 or 0. The proposed gate is designed with redundant cells to increase the amplitude of the output signal, and to improve the fault tolerance and reliability of the circuit. In addition to this, all the input and output cells are placed at the border of the circuit. The applicability and scalability of the proposed XOR gate in complex circuits is very efficient and does not require any crossovers, which will reduce the cost and complexity of the circuits.

A. Simulation Results

The proposed design is analyzed and simulated using the QCADesigner v 2.0.3 tool [5]. We considered the default cell size of $18 \times 18 nm^2$ for all the considered XOR gates.

The simulation waveform of the proposed XOR gate is shown in Fig. 2. The results reveal that the circuit performs well as an XOR gate for all possible input combinations with a delay of two clock cycles. It is also observed that the maximum polarization at the 2-input XOR output ($P_{\max} = 0.985$) is significantly strong. To further verify the robustness of the proposed XOR gate, we simulate the design for various values

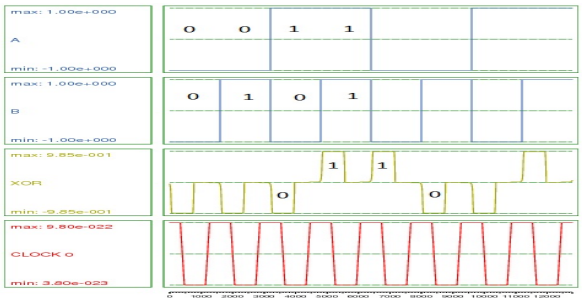


Fig. 2. Simulation waveform of proposed XOR gate.

TABLE I
ENERGY DISSIPATION OF PROPOSED XOR GATE WITH DIFFERENT ENERGY LEVELS

Parameters	Tunneling Energy Level (Ek)	Energy Dissipation (meV)
Average Leakage	0.5	28.03
	1.0	93.84
	1.5	180.45
Average Switching	0.5	226.48
	1.0	210.23
	1.5	191.49

of radius of effect ranging from 40 to 80 nm. The proposed XOR behavior is found to remain unaltered, and maximum polarization at the output remains almost the same. In addition to this, the proposed XOR gate's QCA circuit is stable within the temperature range of 1–15 K, as the output amplitude remains approximately the same. The thermal stability of the circuit is obtained by simulating the QCA circuit at different temperatures.

B. Power Analysis

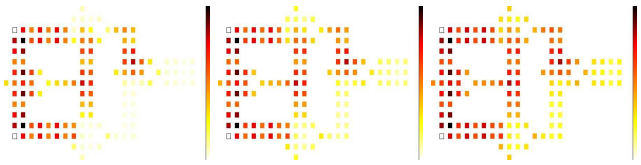
The power dissipation of the proposed XOR gate is analyzed using the QCAPro tool [6]. It is a probabilistic modeling tool that uses the Hartree-Fork approximation to identify erratic energy cells. The power dissipation analysis is performed at three different tunneling energy levels: 0.5Ek, 1.0Ek, and 1.5Ek. Fig. 3 shows the power dissipation map of the proposed XOR gate at all considered energy levels at an operating temperature of 1K. The total energy dissipated of proposed XOR at different energy levels is given in Table I.

C. Fault Tolerance Analysis

To evaluate the circuit's reliability, in regard to a single cell omission defect, the cells in the design are omitted one by one, and simulations are performed for each case. Results indicate that the total fault coverage for single-cell omission defect for the proposed XOR structure is 88.28%.

Similarly, fault tolerance for the multiple missing cell defects is calculated and it is found that the proposed XOR gate has 81.82%, 84.14%, and 68.48% fault tolerance against the missing double cell, missing triple cell, and missing quadruple cell defects, respectively.

Similarly, for single-cell addition defect a new cell is added in the design and simulation results are analyzed. It can be observed that the fault tolerance to single additional cell defect for the proposed XOR structure is 95.33%.



(a) (b) (c)

Fig. 3. Power dissipation map of proposed XOR gate at (a) 0.5Ek level, (b) 1.0Ek level, and (c) 1.5Ek level.

TABLE II
FAULT TOLERANCE PERFORMANCE COMPARISON

XOR Design	Fault tolerance to Single Cell	
	Omission Defect	Addition Defect
[1]	43.75%	70.83%
[7]	50%	63.89%
[4]	53.125%	82.14%
[2]	12.5%	73.64%
Proposed	88.28%	95.33%

The fault tolerance performance comparison of various XOR design architectures is given in Table II. Based on the above results and discussions, it is observed that the proposed XOR gate has the highest fault tolerance to both single-cell omission defect and single-cell addition defect as compared to the other considered XOR designs, thereby making it more reliable in designing QCA based digital circuits.

III. CONCLUSION

A novel and efficient two-input XOR gate in QCA has been proposed. It is a single layer design with no crossover and works on cell-to-cell interaction phenomenon. The proposed XOR gate's operation has been verified with extensive simulations, and it can be observed that the proposed design has a very high fault tolerance of 95.33% against single-cell addition defect along with 88.28%, 81.82%, 84.14%, and 68.48% fault tolerance against the single missing cell, missing double cell, missing triple cell, and missing quadruple cell defects, respectively. The proposed XOR gate also has higher thermal stability compared to existing designs.Thus, it can be efficiently used in the design of various reliable and fault-tolerant circuit designs.

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