Voltage Bootstrapped Schmitt Trigger based Radiation Hardened Latch design for Reliable Circuits

Neha Gupta, Nikhil Agrawal, Narendra Singh Dhakad, Ambika Prasad Shah, Santosh Kumar Vishvakarma, Patrick Girard

Voltage Bootstrapped Schmitt Trigger based Radiation Hardened Latch design for Reliable Circuits

ABSTRACT

Soft error is one of the major reliability issue with technology scaling. In this work, we propose a radiation hardened voltage bootstrapped schmitt trigger (VB-ST) latch. To evaluate the circuit radiation resilience, we calculated the critical charge under the PVT variations at the most sensitive node and observed that the proposed latch has the highest critical charge and the lowest soft error rate ratio when compared to existing latches. We analyzed the impact of process variations on our design and observed that the VB-ST latch has 0.42× less critical voltage variability as compared to ST latch. Further, dynamic power and propagation delay are examined for various supply voltages, and we observed that the VB-ST latch has the lowest power consumption and delay propagation when compared to the other considered latches. For the validation of the proposed latch, a charge to power-delay-area product ratio (QPAR) is calculated and we clearly observed that the proposed VB-ST based latch significantly outperforms the performance of existing designs.

KEYWORDS

Reliability, robustness, transient fault, single event effect, radiation hardened latch, voltage bootstrapped circuit

ACM Reference Format:

. 2021. Voltage Bootstrapped Schmitt Trigger based Radiation Hardened Latch design for Reliable Circuits. In *Virtual Conference and Exhibition, June 22-25, 2021, Woodstock, NY*. ACM, New York, NY, USA, 6 pages. https://doi.org/10.1145/nnnnnnn.nnnnnnn

1 INTRODUCTION

As the technology is scaled down, the supply voltage and node capacitance are also aggressively scaled. As a result the amount of charges that can be stored on a node is also reduced [1, 7]. Therefore, logic designs are more endangered to soft errors and more susceptible to external noise, like alpha particles. When alpha particles strike at a sensitive node of a digital design, a secondary carrier may be generated and collected by the source/drain diffusion regions, which leads to a glitches or transient fault (TF) [9, 11]. When the amount of collected charge is high, the TF will appear as an electrical pulse which is referred to as a single event transient (SET) [11]. The SET would propagate through combinational logic and may be harmful in the sequential circuits e.g. latches, flip-flop. When the particle strikes at the most sensitive node of the sequential circuit, there is a chance to flip the stored value if the deposited charge exceeds the critical charge at that sensitive node. This phenomenon is referred to as a single event upset (SEU) [11].

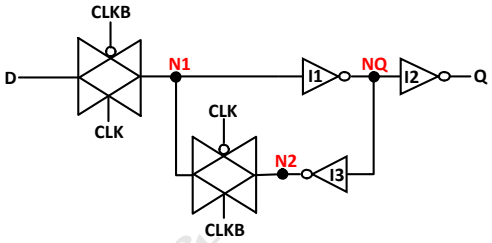

Figure 1: Schematic of a conventional unhardened latch or reference latch.

Traditionally, SEU are considered for the hardening in a latch and researchers have addressed this issue at various design levels. The latches are hardened against SEU and it can be verified that a single event only affects a single node in the latch [4]. Therefore, the main focus of this paper is to propose a reliable and hardened latch, which is robust against soft error.

The rest of the paper is organised as follows. Section 2 describes existing hardened latches. Subsequently, section 3 presents the proposed latch design and its features. Section 4 is dedicated to the evaluation and comparison of the proposed radiation hardened latch with the various other reference latch circuits. Section 5 concludes the paper.

2 EXISTING HARDENED LATCHES

Some specific hardened latches presented so far in the literature are discussed in this section with regard to their SEU tolerance capability.

2.1 Reference Latch

The schematic design of an unhardened latch is shown in Figure 1, which is referred to as reference latch in the sequel [6]. Here D and Q denote the input and output nodes, respectively, CLK and CLKB are the system clock. N1, N2 and NQ are the internal nodes of the latch.

2.2 ST based Latch

The Schmitt Trigger (ST) based latch is shown in Figure 2. In the ST based latch [6, 9], a 6 transistors based ST circuit is used in place of the I1 inverter in the reference latch with the feedback loop consisting of inverter I3 and a transmission gate. When internal node N1 is low and node NQ is high, node x is charged. If TF occurs on an internal node, NQ state changes and node x needs to be discharged first. Hence, the ST inverter circuit protects the internal

GLSVLSI 2021, June 22-25, 2021, Woodstock, NY

ACM ISBN 978-x-xxxx-xxxx-x/YY/MM…$15.00
https://doi.org/10.1145/nnnnnnn.nnnnnnn

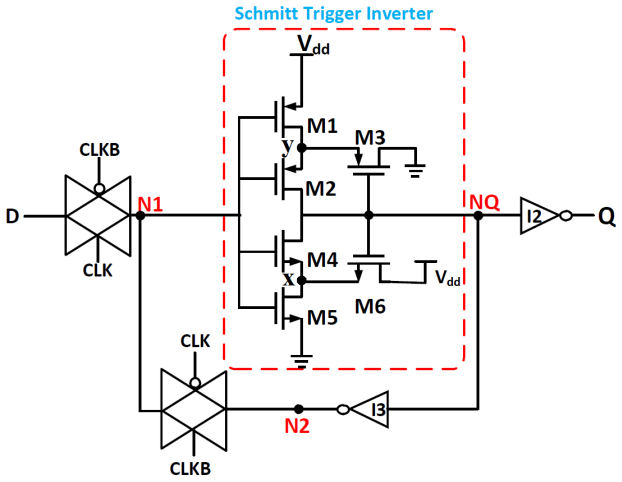

Figure 2: Schematic of a Schmitt trigger based radiation hardened latch.

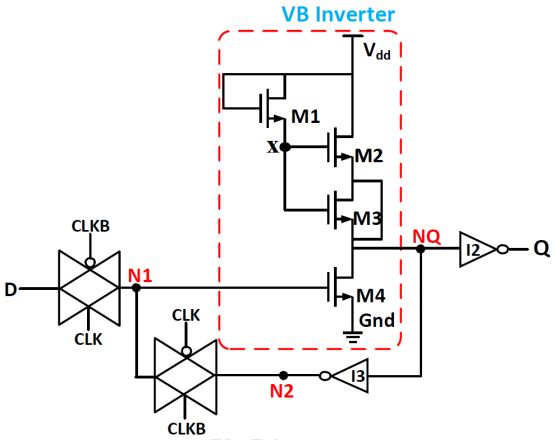

Figure 3: Schematic of a Voltage bootstrapped based radiation hardened latch.

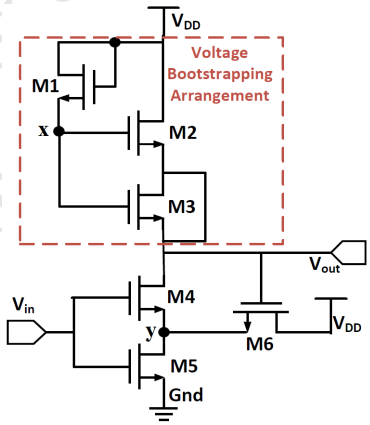

Figure 4: Schematic of the proposed Voltage bootstrapped Schmitt trigger (VB-ST) circuit [3].

nodes against transient faults due to its hysteresis loop. The Schmitt trigger provides better robustness to soft errors. However, the ST latch is slower due to the hysteresis effect.

2.3 VB based Latch

In the similar concept of ST based latch, we have implemented a VB based latch and compared it with the proposed latch which will be discussed in the next section. The schematic of the VB based latch is shown in Figure 3. In [5], the Voltage bootstrapped inverter circuit is discussed using only NMOS transistors, which conquer the problem of aging, especially NBTI. When an internal node N1 is low and node NQ becomes high because of the transistors M2 and M3, which are directly connected to the supply voltage. If the transient fault occurs at the node x, the gate voltage of the transistor M2 decreases which results in M2 is in OFF state and disturbs the output voltage value. However, VB circuit has not achieved the full supply voltage at the output node when the fault occurs and also reduced the noise margin of the circuit.

3 PROPOSED VB-ST BASED DESIGN

To address the drawback of the ST and VB based latch, a voltage bootstrapped Schmitt trigger (VB-ST) circuit is proposed and replace the inverter I1 in order to enhance the radiation hardening property.

3.1 Proposed VB-ST Circuit

The schematic of the proposed VB-ST circuit is shown in Figure 4 [3]. The bootstrap circuit is mainly helpful to improve the input impedance of the circuit, which provides better resilience to process variations. Also, bootstrapping is commonly useful to pull up the operating point of the transistor, which may be fruitful to achieve full voltage swing in the circuit. The main attribute of this circuit is the only use of NMOS transistors [3]. The key features of the proposed circuit are as follows:

- Transistor ($M2$) is used in the pull-up network to increase the threshold voltage and overcome the output voltage drop in the inverter circuit.
- Transistor $M3$ acts as MOS capacitor to bootstrap the voltage collected from V_Y and passed to the output node. Hence, the $M3$ transistor is named as a bootstrapped capacitor with a dummy MOS device or bootstrapped transistor.
- The feedback arrangement of the transistor $M4$ with transistor $M6$ is used to increase the noise immunity of the inverter circuit.
- This feedback connection also protects the output logic state from a radiation particle that could strike the sensitive nodes of the circuit.

3.2 Proposed VB-ST Latch

The radiation hardened and soft error tolerant latch is designed by utilizing the benefits of the proposed VB-ST inverter circuit. Figure 5 shows the proposed VB-ST based latch in which inverter

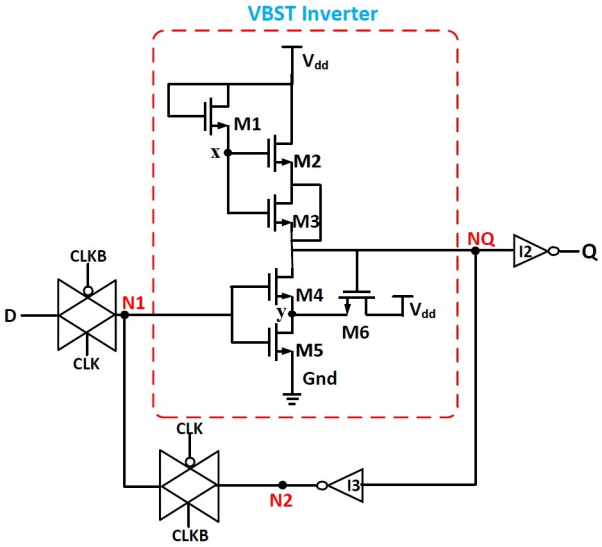

Figure 5: Schematic of the proposed VB-ST based radiation hardened latch.

I1 is replaced by the VB-ST circuit to enhance the soft error robustness. The radiation hardening would be further improved, when we replace all three inverter circuits by the VB-ST circuit but the latch design would be more complex. The latch is working in the transparent mode when CLK is logic 1 and in the latch mode when CLK is logic 0. As discussed in [6], the effect of radiation is higher when the circuit operates in the latch mode.

Let us assume that nodes N1 and NQ are logical low and high, respectively. The transistor M6 is in its ON state, which drives node y to VDD-V_{th6}. If a TF on a node goes from low to high, the output cannot change its state and be recovered by the M6 transistor because the M4 transistor is still in the OFF state. Similarly, when a negative pulse strikes at node x, this node needs to be discharged. But the temporary glitch on node x is readily recovered by the bootstrapped transistor M3, and the correct output is re-established. Therefore, the VB-ST circuit provides better robustness to the soft errors due to the charges stored at the internal nodes x and y.

4 EVALUATION AND COMPARISON OF RADIATION HARDENED LATCHES

The proposed VB-ST latch and other reference latches have been redesigned and simulated using industry-standard 65nm CMOS technology with device sizing. All the simulations are performed using HSPICE [10]. For the fair comparison of different latch designs, various performance parameters are analyzed in this section.

4.1 PVT Variation on Critical Charge Analysis

Critical charge is estimated as the minimum amount of charge collected by the sensitive node to flip the input and output voltage. The detailed description of the critical charge estimation equation is given in [3].

4.1.1 ***Effect of Process Variation on Critical Charge.*** The circuit performance can be seen through the process corner variations between the extreme points. The circuit functionality is decided by the process corner with the slow and fast device specifications during fabrication time. Normally TT process corner is used for the circuit analysis, but FF and SS process corners are examined for power and delay worst case analysis, respectively. Whereas, TT, SS and FF process corners affect PMOS and NMOS devices uniformly, FS and SF process corner effects in unequal ways. The critical charge is calculated for the different latch designs for the process corners [Fast-Fast (FF), Fast-Slow (FS), Slow-Fast (SF), Slow-Slow (SS), and Typical-Typical (TT)] at 0.4V supply voltage and 25°C temperature, as shown in Figure 6(a). The results show that the critical charge for the proposed VB-ST latch is higher than the other reference latch circuits for all process corners.

4.1.2 ***Effect of Voltage Variation on Critical Charge.*** The critical charge (Q_{crit}) is calculated with supply voltage variation for the considered latch circuits along with the proposed VB-ST latch circuit at the sensitive node N1, as shown in Figure 6(b). From the result, it is observed that the critical charge of the proposed VB-ST latch is 6.31×, 3.31× and 1.19× as compared to the reference, ST and VB latch circuits, respectively, at 0.4V supply voltage and 25°C temperature. The reasons for this enormous amount of increment in critical charge is the use of only NMOS transistors in the circuit and feedback loop. Hence, the proposed VB-ST latch circuit has better soft error hardening due to the higher critical charge for supply voltage variations.

4.1.3 ***Effect of Temperature Variation on Critical Charge.*** The critical charge is analyzed with the temperature ranging from T = 25°C to T = 100°C as shown in Figure 6(c). The result shows that the critical charge of the proposed VB-ST circuit is 7.22×, 3.56× and 1.11× as compared to the reference, ST and VB latch circuits, respectively at 0.4V supply voltage and 25°C temperature. From the result, it is also observed that there is a very small change in the critical charge with the temperature changing from 25°C to 100°C. The higher critical charge indicates that the proposed VB-ST latch has less impact of process, voltage and temperature variation and soft error resilient.

4.2 Soft Error Rate Ratio

At deep submicron technology, digital circuits are highly sensitive to soft errors and the critical charge of potential striking particles. The soft error rate (SER) exponentially depends on the Q_{crit} and it has been observed that the SER decreases when the value of Q_{crit} increases [3].

Soft error rate is calculated for different latches as compared to the reference unhardened latch (RL) at different supply voltage and temperature conditions. The soft error rate ratio (SERR) is calculated to analyze the soft error rate (SER) of the considered latches normalized to the reference latch (SER_{RL}) [2]. Therefore, the SERR is calculated using the given equation:

$$SERR_{\#} = \left.\frac{SER_{\#}}{SER_{RL}}\right|_{@VDD\ and\ T} \quad (1)$$

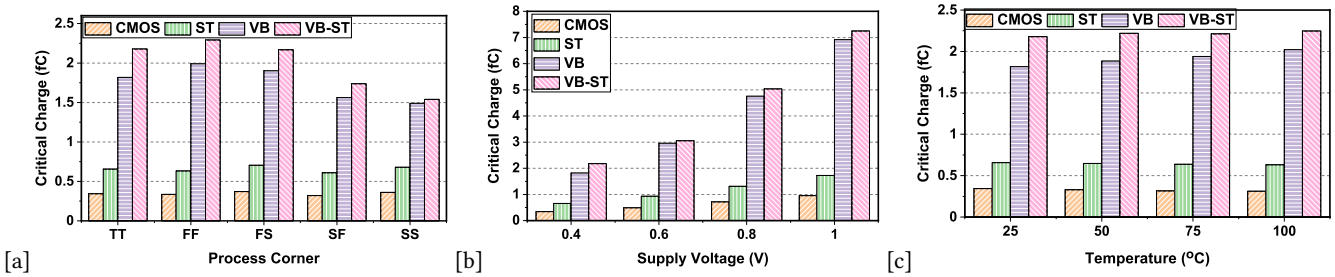

Figure 6: Critical charge analysis of latch circuits for (a) process corners variations at T=25° and VDD=0.4V, (b) supply voltage variations at T=25° and (c) temperature variations at VDD=0.4V.

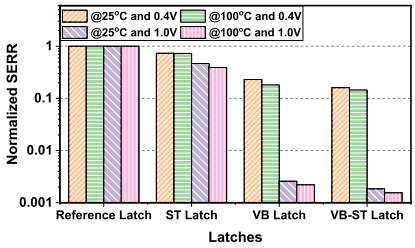

Figure 7: Soft error rate ratio for different latches at four extreme combinations of supply voltage and temperature variations.

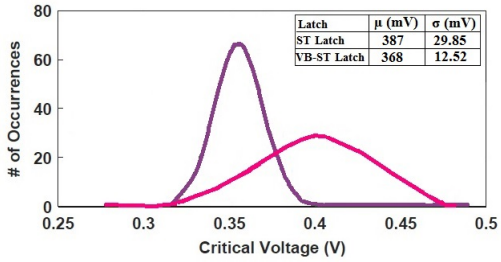

Figure 8: 5000 Monte-Carlo simulation of critical voltage for ST latch and VB-ST latch at 0.4V supply voltage.

$$SERR_{\#} \approx Antilog_e\left[Q_{crit}^{RL} - Q_{crit}^{\#}\right]\Big|_{@VDD\ and\ T} \quad (2)$$

Where, $SER_{\#}$ and SER_{RL} are the soft error rates, and $Q_{crit}^{\#}$ and Q_{crit}^{RL} are the critical charge for the considered latches and the reference latch, respectively.

Figure 7 shows the soft error rate ratio (SERR) for the different latches, which are normalized to the reference latch (RL) at four extreme combinations of supply voltages (VDD= 0.4V and 1.0V) and operating temperatures (T= 25°C and 100°C). The result shows that the SERR of the proposed VB-ST latch is minimum for all the combinations as compared to other considered latches. In our analysis, the maximum improvement in SERR is shown at 1V supply voltage. Higher supply voltage would increase the current flowing through the circuit and increase the critical charge at the sensitive node, which corresponds to the lower soft error rate. Hence, the proposed latch has better radiation hardening from the above discussions if we operate them in super-threshold conditions.

4.3 Process Variation Analysis

The critical voltage (V_{crit}) is examined using 5000 Monte-Carlo simulations including the process and mismatch variations with $\pm 3\sigma$ deviations at 0.4V supply voltage as illustrated in Figure 8. The Monte-Carlo simulation is performed using Cadence ADE-XL, which considers both the process and mismatch variations. It can be seen from the result that the proposed VB-ST latch has less sensitivity to process variation as compared to the ST latch. It can also be observed from the result that the mean (μ) and standard deviation (σ) of the proposed VB-ST latch is 0.95× and 0.42× lower as compared to the ST latch design. The reasons for the lower impact of the process variation are that the Schmitt trigger circuit is used in our proposed latch, which can increase the margin of threshold voltage due to its hysteresis property. While, the ST latch also presents the positive feedback loop but it activates both pull-up and pull-down network, which is highly sensitive to the process variations as compared to the proposed VB-ST latch design. Therefore, the above factors finally make our latch have a lower impact from process variation on its critical voltage.

4.4 Analysis of Power Dissipation

The dynamic power dissipation of different latches at different supply voltage and temperature conditions are shown in Figure 9. The results show that the dynamic power increases with the supply voltages and temperatures, where the proposed VB-ST latch consumed less power as compared to the other reference latches. The dynamic power of the proposed VB-ST latch is 65.08%, 61.92% and 48.71% lower at 1V supply voltage and 37.73%, 9.89% and 25.48% lower at 100°C temperature as compared to the reference latch, ST latch and VB latch, respectively. The above discussion indicates that the proposed latch is power efficient even at the highest supply voltage and temperature. The lower power dissipation of the VB-ST latch is due to the stacked transistors and feedback network used in the inverter circuit.

4.5 Timing and Delay Analysis

The propagation delay is an important parameter to analyze the circuit speed. Figure 10 shows the transient response of the proposed VB-ST based latch and Table 1 summarizes all the timing

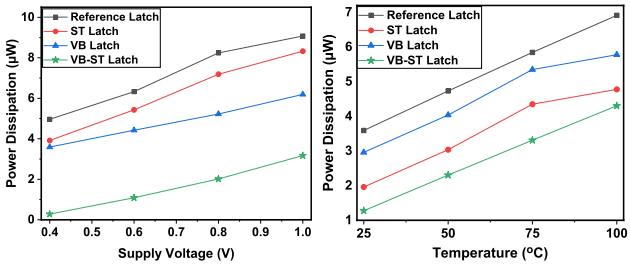

Figure 9: Power dissipation of different latches for (a) different supply voltages at T = 25°C and (b) different operating temperatures at VDD = 1.0V.

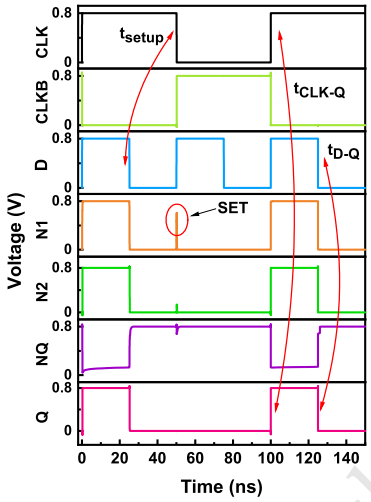

Figure 10: Transient response and timing diagram of the VB-ST latch

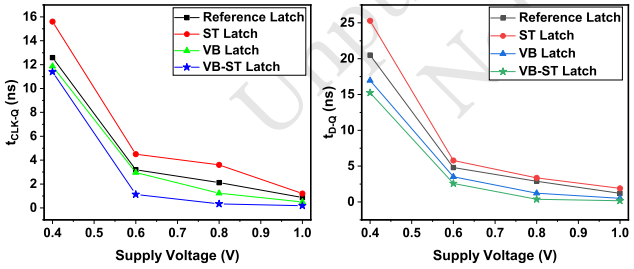

Figure 11: Propagation delay of the different latches at various supply voltages (a) from clock signal CLK to the output Q (b) from data signal D to the output Q

and delay performance metrics for all considered latches. In Figure 10, t_{setup} is the minimum time between a change in data D and trailing edge of the CLK in such a way that the new value of D can propagate to the output Q [6, 9]. Moreover, t_{CLK-Q} and t_{D-Q} are the propagation delay of the latch from CLK to output Q and D to Q, respectively. Hence, the total propagation delay is expressed as:

Table 1: Performance comparison of different latches at 1V supply voltage and 25°C temperature

Performance Parameters	Latch			
	Reference	ST	VB	VB-ST
Q_{crit} (fC)	0.96	1.72	6.92	7.25
Dynamic Power (μW)	9.08	8.32	6.2	3.17
t_{setup} (ns)	0.250	0.250	0.250	0.250
t_{CLK-Q} (ns)	0.87	1.2	0.5	0.18
t_{D-Q} (ns)	1.2	1.9	0.5	0.16
t_{delay} (ns)	1.12	1.45	0.75	0.43
Area (μm^2)	0.219	0.284	0.406	0.558
PDP (fJ)	10.17	12.06	4.65	1.36
QPAR	0.43	0.50	3.66	9.53

$$t_{delay} = t_{setup} + t_{CLK-Q} \quad (3)$$

From Table 1, it can be seen that the delay (t_{delay}) of the VB-ST latch has the lowest propagation delay as compared to the reference, ST and VB latches. Hence, it is concluded that the proposed VB-ST circuit has fast transition as compared to other latches. Further, the effect of supply voltages on the propagation delay is also analyzed for the various latches as shown in Figure 11. Results demonstrate that the propagation delay t_{CLK-Q} of the proposed VB-ST latch is 79.27%, 84.97% and 63.86% lower and delay t_{D-Q} is 85.96%, 91.12% and 66.71% lower as compared to the reference latch, ST latch and VB latch, respectively at 1V supply voltage. The propagation delay decreases with the supply voltage because higher supply voltage provides a higher current through the devices, leading to effectively faster switching and hence lower propagation delay. Additionally, the critical path formation for the delay analysis is more complicated in the proposed VB-ST circuit as the reference latch due to pull-down feedback loop. Whereas the critical path is more complex in the ST based latch due to feedback connection present in both the pull-up and pull-down network.

4.6 Circuit Area and Power Delay Product (PDP)

The physical layout structure of the reference latch and the VB-ST latch has been obtained using a 65nm standard CMOS technology, as shown in Figure 12. The reference latch and the proposed VB-ST latch area are 9.47μm^2 and 12.80μm^2, respectively, and the proposed latch consumed 1.35× more area than the reference latch. Moreover, the power delay product (PDP) is a useful metric for evaluation of the cost, which shows the trade-off between power and performance. Here we use the PDP as stated in [8]:

$$PDP = DP \times (t_{setup} + t_{CLK-Q}) \quad (4)$$

Where, DP denotes the dynamic consumed power. The power-delay product is illustrated in Figure 13 and is also given in Table 1. The result shows that the power-delay-product (PDP) is reduced by 0.13×, 0.11× and 0.29× as compared to the reference, ST and

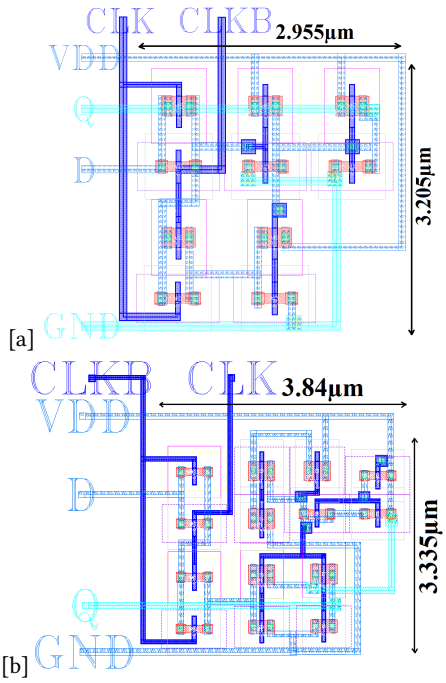

Figure 12: Layout of (a) Reference latch (b) VB-ST latch.

VB latches, respectively, at 1V supply voltage. The lower dynamic power of the VB-ST latch is the main factor for reducing the PDP.

4.7 Critical Charge to PDP-Area Ratio (QPAR)

The essential parameters are considered for the QPAR (Critical charge to PDP-area ratio), which include critical charge, PDP and area. From Table 1, it is demonstrated that the critical charge should be higher so we placed it at the numerator; PDP and area should be lowest so they are placed at the denominator in the equation [9]. Hence, the QPAR is expressed as:

$$QPAR = \frac{Critical\ Charge\ (Q)}{PDP\ (P) \times Area\ (A)} \tag{5}$$

From the equation (5), a larger value of QPAR leads to a higher critical charge with higher performance and lower soft error rate with lower power dissipation of the latch. Figure 13 shows that the QPAR of the proposed VB-ST based latch is 22.16×, 19.06× and 2.60× high as compared to the reference, ST and VB latch, respectively at 1V supply voltage. Hence, it is undoubtedly proven that the proposed VB-ST latch is advantageous and more robust when compared to the other considered latches.

5 CONCLUSION

In this paper, we proposed a new radiation hardened latch using the VB-ST inverter circuit, which significantly enhanced the reliability in terms of critical charge and soft error rate. We analyzed the critical charge and soft error rate ratio for the different latches and observed that the proposed VB-ST latch has higher critical charge and lower soft error rate ratio against the other latches. For the process variations analysis of the different latches, we performed

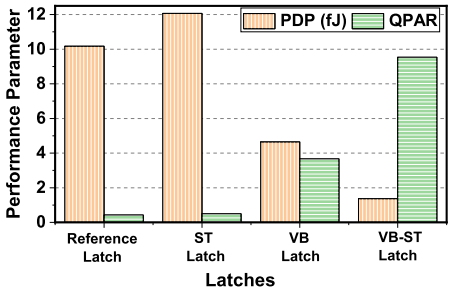

Figure 13: Power-delay product and QPAR of different latches at 1V supply voltage

5000 Monte Carlo simulations and observed that the failure probability of VB-ST latch is less as compared to the reference and ST latches. Further, the dynamic power and propagation delay are also important factors in the latch design and we observed that the proposed latch has the lowest power and delay when compared to the other considered latches. For the validation of the proposed latch, a figure of merit is proposed in terms of QPAR and clearly indicates that the QPAR of the proposed VB-ST latch is increased by 22.16× as compared to the reference latch. The radiation hardened latch is better for space applications where the effect of external radiations is crucial.

ACKNOWLEDGEMENT

This work was financially supported by Special Manpower Development Program for Chips to System Design (SMDPC2SD) research project of DeitY, Government of India.

REFERENCES

[1] Robert C Baumann. 2005. Radiation-induced soft errors in advanced semiconductor technologies. *IEEE Transactions on Device and materials reliability* 5, 3 (2005), 305–316.

[2] Neha Gupta, Ambika Prasad Shah, Rana Sagar Kumar, Tanisha Gupta, Sajid Khan, and Santosh Kumar Vishvakarma. 2020. On-Chip Adaptive VDD Scaled Architecture of Reliable SRAM Cell with Improved Soft Error Tolerance. *IEEE Transactions on Device and Materials Reliability* (2020).

[3] Neha Gupta, Ambika Prasad Shah, Rana Sagar Kumar, Gopal Raut, Narendra Singh Dhakad, and Santosh Kumar Vishvakarma. 2021. Soft error hardened voltage bootstrapped Schmitt trigger design for reliable circuits. *Microelectronics Reliability* 117 (2021), 114013.

[4] Zhengfeng Huang, Huaguo Liang, and Sybille Hellebrand. 2015. A high performance SEU tolerant latch. *Journal of Electronic Testing* 31, 4 (2015), 349–359.

[5] Sung-Mo Kang and Yusuf Leblebici. 2003. *CMOS digital integrated circuits*. Tata McGraw-Hill Education.

[6] Sheng Lin, Yong-Bin Kim, and Fabrizio Lombardi. 2010. Design and performance evaluation of radiation hardened latches for nanoscale CMOS. *IEEE transactions on very large scale integration (VLSI) systems* 19, 7 (2010), 1315–1319.

[7] Chunhua Qi, Liyi Xiao, Jing Guo, and Tianqi Wang. 2015. Low cost and highly reliable radiation hardened latch design in 65 nm CMOS technology. *Microelectronics Reliability* 55, 6 (2015), 863–872.

[8] Ramin Rajaei, Mahmoud Tabandeh, and Mahdi Fazeli. 2013. Low cost soft error hardened latch designs for nano-scale CMOS technology in presence of process variation. *Microelectronics Reliability* 53, 6 (2013), 912–924.

[9] Ambika Prasad Shah and Michael Waltl. 2019. Low Cost and High Performance Radiation Hardened Latch Design for Reliable Circuits. In *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. IEEE, 197–200.

[10] I Synopsys. 2010. HSPICE User's Manual: Simulation and Analysis. *Synopsys Inc, California* (2010).

[11] Aibin Yan, Huaguo Liang, Zhengfeng Huang, Cuiyun Jiang, Yiming Ouyang, and Xuejun Li. 2016. An SEU resilient, SET filterable and cost effective latch in presence of PVT variations. *Microelectronics Reliability* 63 (2016), 239–250.