A 4NU-Recoverable and HIS-Insensitive Latch Design for Highly Robust Computing in Harsh Radiation Environments

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QRHIL: A QNU-Recovery and HIS-Insensitive Latch Design for Space Applications in Harsh Radiation Environments

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Abstract

This paper proposes a 4-node-upset (4NU) recoverable and high-impedance-state (HIS) insensitive latch design, namely QRHIL, for highly robust computing in harsh radiation environments. The latch mainly comprises a 5×5 looped C-element matrix to store values and provide complete 4NU recovery. Owing to the multiple-level error-interception of the 5×5 C-element matrix, the latch can recover from all possible 4NUs; thus, the latch is insensitive to HIS. Simulation results demonstrate the 4NU-recovery of the proposed latch. The results also show that the latch can approximately save 46% D-Q delay and 46% CLK-Q delay owing to the use of a high-speed D-Q path and clock-gating, compared with the state-of-the-art 3NU-recoverable latch (TNURL) that is not 4NU-recoverable.

CCS CONCEPTS

• **Hardware → Circuit hardening; Latch design; Transient errors and upsets; Fault tolerance.**

Keywords

Harsh radiation; latch reliability; soft error; recovery

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1 Introduction

With the advancement of nano-scale CMOS technologies, the feature sizes of transistors continuously scale down, making electronic devices in circuits and systems more and more susceptive to soft errors [1]. When a particle, such as neutron, proton, alpha particle, electron and heavy ion [2-3] with large linear-energy-transfer strikes the diffusion region of an off-state transistor, a *single node upset* (*SNU*) can occur at the impacted transistor since the particle can cause faulty current to flow through the transistor temporarily. Moreover, in nano-scale CMOS technologies, the aggressively reduced transistor sizes and very large scale integration may cause the strike of a particle to induce single-event charge collection to impact 2 adjacent nodes, 3 adjacent nodes or even 4 adjacent nodes, resulting in a *2 node upset* (*2NU*), a *3 node upset* (*3NU*) or even a *4 node upset* (*4NU*), respectively [4]. SNUs, 2NUs, 3NUs and 4NUs are typical soft errors. Although the FinFET technology can reduce soft error rate [5], effective and scalable solutions for soft error tolerance are still needed.

It is reported in [4] that accurately calculating the possibility of 4NU occurrence is very difficult because at least six kinds of parameters should be known. Therefore, we qualitatively discuss the necessity of 4NU-recoverable design. Assumed that an SNU-recoverable latch is switched to standby mode for significantly reducing power consumption, its hold mode duration may be very long. During that long duration, the latch may be struck by a particle to cause a 2NU and subsequently another particle to cause another 2NU. Therefore, the two 2NUs may form a 4NU. Another possible case is that a 3NU and an SNU may also form a 4NU. Due to charge-sharing, a 4NU can occur through the strike of one high energy particle [4]. This is because, if a circuit is highly integrated and fabricated with a very small technology node such as 7nm, it is likely that more transistors/nodes will be much closer to each other, thus causing severe increase of the probability of an event like that.

As for radiation hardening for storage circuits, researchers have focused on the design of memory cells [6-8], flip-flops [9-11] and latches [4, 12-26]. This paper focuses on latch designs. In these latch designs, some are SNU-hardened only [12-13], some are SNU- and 2NU-hardened [14-17, 22-26], some are simultaneously hardened against SNUs, 2NUs and 3NUs [18-21]. To the best of our knowledge, there is only one latch that is simultanneously hardened against SNUs, 2NUs, 3NUs and 4NUs [4]. Moreover, although these latches can output a correct value, some nodes cannot self-recover after flipping; thus some hardened latches cannot provide complete node-upset-recovery. For example, among the SNU-hardened latches, only the latch in [13] can provide SNU-recovery. Among the 2NU-hardened latches, only

those in [17, 23, 25, 26] can provide 2NU-recovery. Among the 3NU-hardened latches, only the latch in [21] can provide 3NU-recovery. To the best of our knowledge, no latch can provide complete 4NU-recovery. This motivates us to design a 4NU-recoverable latch.

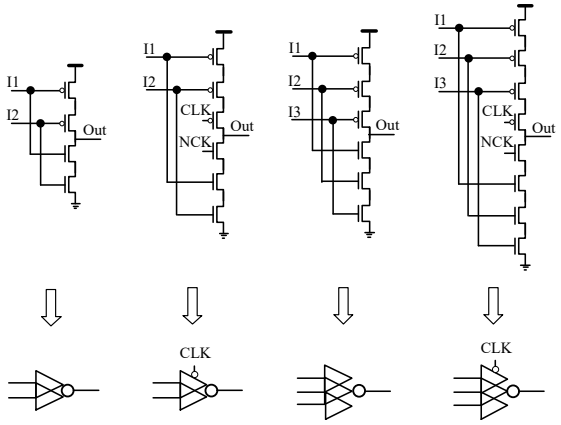

Figure 1: Different types of C-elements. (a) 2-input, (b) Clock-gating based 2-input, (c) 3-input, and (d) Clock-gating based 3-input.

The rest of the paper is organized as follows. Section 2 describes the schematic, normal working principles, and error-recovery verifications for the proposed latch design. Section 3 presents comparison results for latch designs, and Section 4 concludes the paper.

2 Proposed QRHIL Latch Design

2.1 Latch Schematic and Working Principles

In many radiation-hardened latch designs, CEs are widely used. Figure 1 shows different types of CEs, including 2-input and 3-input, and CG-based 2-input and 3-input ones. It is easy to create a 4-input one. A CE works as an inverter if its inputs have the same value but keeps its previous value at its output due to capacitances if the values of its inputs change to be different. A CG-based CE can also be controlled by system clock (CLK) and negative system clock (NCK) signals.

Figure 2 shows the schematic of the proposed QRHIL latch, comprising 5 TGs on the left side, a CE matrix with 25 interlocking 2-input CEs (i.e., CE1 to CE25), and 5 CG-based inverters on the right side. As shown in Figure 2, the CE matrix consists of 5 levels (columns) and each level consists of 5 CEs. It can be seen that the outputs of CEs in each level feed the inputs of CEs in the next level. For each CE, its output feeds the single inputs of the CEs in the next level, respectively. For the QRHIL latch, D is the input, Q (A5) is the output, CLK is the system clock, and NCK is the negative system clock, respectively.

When CLK = 1 and NCK = 0, the latch works in transparent mode. In this mode, the transistors in TGs connected to D are ON. Thus, A1 to A5 can be initialized by D. Then, B1 to B5 can be determined by A1 to A5 through CE1 to CE5. In this way, the outputs of all CEs can be determined/initialized. Note that, the outputs of CE21 to CE25 cannot feed A1 to A5 by CG transistors embedded in the inverters; thus, Q can only be driven by D through a TG to avoid current competition on Q to reduce power dissipation and transmission delay. Therefore, the latch operates correctly because it can be properly initialized, and Q can be determined by D.

When CLK = 0 and NCK = 1, he latch works in hold mode. In this mode, the transistors in TGs connected to D are OFF. Simultaneously, the CG transistors in the inverters are ON so that Q can be only driven by CE25 through an inverter on the right-bottom side. With 25 interlocking CEs, many feedback loops can be constructed to store values. In the following, the SNU, 2NU, 3NU and 4NU self-recovery of the latch is discussed. Note that, if the output of an inverter suffers from an error, the error can output to its output; thus, the input and the output of an inverter in hold mode for the latch have equivalent error-sensitivity. Therefore, only the outputs of the inverters are considered for fault tolerance discussion. In other words, the latch only has 25 nodes that need to be considered.

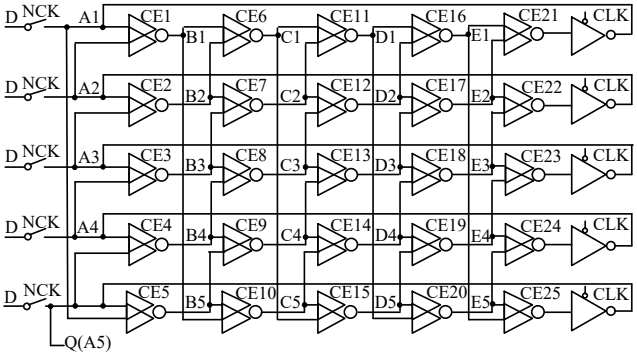

Figure 2: Schematic of the proposed QRHIL latch.

First, the 4NU self-recovery of the latch is discussed. Due to the symmetric structure of the latch, we only need to consider 5 possible cases, i.e., Q1 to Q5 in the following.

Case Q1: A 4NU impacts four nodes in the same row of the CE matrix. Due to the symmetric structure of the latch, the indicative key node-list is only <A1, B1, C1, D1>. When <A1, B1, C1, D1> is impacted by a 4NU, A1, B1, C1 and D1 are temporally flipped. Since D1 is the temporally-flipped single input of CE16 and CE20 and another single inputs of CE16 and CE20 (D2 and D5) are not impacted, CE16 and CE20 can still output correct values. Meanwhile, D2 to D4 are not impacted; thus, CE17 to CE19 can still output correct values. Therefore, the inputs of CE21 to CE25 are still correct. Since correct node values feed A1 to A5 through CE21 to CE25 and inverters, all errors in the latch can be removed. In other words, the latch can self-recover from 4NUs for Case Q1.

Case Q2: A 4NU impacts 3 nodes in the same row of the CE matrix and affects one node in another row of the CE matrix. Considering the worst case, all inputs of just one CE are simultaneously affected. Due to the symmetric structure of the latch, the indicative key node-lists are <A1, B1, C1, A2>, <A1, B1, C1, A5>, <A1, B1, C1, B2>, <A1, B1, C1, B5>, <A1, B1, C1, C2> and <A1, B1, C1, C5>.

When <A1, B1, C1, A2> is impacted by a 4NU, A1, B1, C1 and A2 are temporally flipped. Since the temporally-flipped A1 and A2 can flip B1, and the error at A2 cannot propagate to other nodes

through CE2, this case equals to a 3NU occurred at <A1, B1, C1>. Since <A1, B1, C1, D1> in Case Q1 can self-recover from a 4NU, <A1, B1, C1> can also self-recover. Therefore, <A1, B1, C1, A2> can self-recover from the 4NU. In a similar manner, <A1, B1, C1, B2> and <A1, B1, C1, C2> can also self-recover from 4NUs.

When <A1, B1, C1, A5> is impacted by a 4NU, A1, B1, C1 and A5 are temporally flipped. Since all inputs of CE5 are temporally flipped, B5 is temporally flipped. Thus, the temporally-flipped B1 and B5 can temporally flip C5 through CE10. Subsequently, the temporally-flipped C1 and C5 can temporally flip D5 through CE15. Since A5 is the temporally-flipped single input of CE4, B5 is the temporally-flipped single input of CE9, C1 is the temporally-flipped single input of CE11, C5 is the temporally-flipped single input of CE14, and D5 is the temporally-flipped single input of CE19 and CE20, these CEs can still output correct values. In other words, the errors are blocked by the single-input-affected or not affected CEs; thus, the inputs of CE21 to CE25 are still correct. Therefore, all nodes can self-recover through CE21 to CE25, respectively. In a similar manner, <A1, B1, C1, B5> and <A1, B1, C1, C5> can also self-recover from 4NUs.

Case Q3: A 4NU impacts 2 nodes in the same row of the CE matrix and also impacts 2 nodes in another row of the CE matrix. Considering the worst case, all inputs of 2 CEs are simultaneously impacted. Due to the symmetric structure of the latch, the indicative key node-lists are <A1, B1, A2, B2> and <A1, B1, A5, B5>.

When <A1, B1, A2, B2> is impacted by a 4NU, A1, B1, A2 and B2 are temporally flipped. Since the temporally-flipped B1 and B2 can flip C1 and also since the error at B2 cannot propagate to other nodes through CE7, this 4NU node-list is almost the same as the 3NU node-list <A1, B1, C1> that is mentioned in Case Q2. Therefore, <A1, B1, A2, B2> can self-recover from the 4NU.

When <A1, B1, A5, B5> is impacted by a 4NU, A1, B1, A5 and B5 are temporally flipped. Since B1 is the temporally-flipped single input of CE6 and CE10, B5 is the temporally-flipped single input of CE9 and CE10, and B2 to B4 are not impacted, CE6 to CE9 can still output correct values. Note that CE10 cannot output the correct value since its inputs are flipped. However, CE14 and CE15 can intercept the error at C5. In other words, the errors are blocked by CEs; thus, the inputs/outputs of CE21 to CE25 are still correct. Therefore, all flipped nodes can self-recover through CE21 to CE25, respectively. It can be seen that all these indicative key node-lists can self-recover from 4NUs. In other words, the latch can self-recover from 4NUs for Case Q3.

Case Q4: A 4NU impacts 2 nodes in the same row of the CE matrix and also impacts one node in each of the other 2 rows of the CE matrix. Considering the worst case, all inputs of 2 CEs are simultaneously impacted. Due to the symmetric structure of the latch, the indicative key node-lists are <A1, B1, A2, A3>, <A1, B1, A2, A5>, <A1, B1, B2, B3>, <A1, B1, B2, B5>, <A1, B1, A2, B5> and <A1, B1, A5, B2>.

When <A1, B1, A2, A3> is impacted by a 4NU, A1, B1, A2 and A3 are temporally flipped. Since all inputs of CE1 and CE2 are temporally flipped, B1 and B2 are temporally flipped; thus, C1 is also temporally flipped. Since A1 is the temporally-flipped single input of CE5, A3 is the temporally-flipped single input of CE3, B1 is the temporally-flipped single input of CE10, B2 is the temporally-flipped single input of CE7 and C1 is the temporally-flipped single input of CE11 and CE15 and also since any of these mentioned CEs has a correct input, these CEs can still output correct values. In other words, the errors are blocked by CEs; thus, the inputs/outputs of CE21 to CE25 are still correct. Therefore, all flipped nodes can self-recover through CE21 to CE25, respectively. In a similar manner, <A1, B1, B2, B3> can also self-recover from a 4NU. As for any other 4NU node-list, after investigation we can also see that there is at least one column of CEs that can still output correct values. Therefore, all flipped nodes self-recover through the column of CEs. In other words, the latch can self-recover from 4NUs for Case Q4.

Case Q5: A 4NU impacts 4 nodes in the same column of the CE matrix. Considering the worst case, all inputs of 3 CEs are simultaneously impacted. Due to the symmetric structure of the latch, the indicative node-list is only <A1, A2, A3, A4>.

When <A1, A2, A3, A4> is impacted by a 4NU, A1, A2, A3 and A4 are temporally flipped. Since all inputs of CE1, CE2 and CE3 are temporally flipped, these CEs cannot output correct values. This means that B1, B2 and B3 are also temporally flipped. In other words, all inputs of CE6 and CE7 are temporally flipped; thus, that C1 and C2 are also temporally flipped. In this way, D1 is also temporally flipped. However, the errors cannot propagate to E1 to E5 because of error interception of CEs; thus, the inputs of CE21 to CE25 are still correct. Therefore, all impacted nodes can self-recover through CE21 to CE25, respectively. In other words, the latch can self-recover from 4NUs for Case Q5.

In summary, the proposed QRHIL latch design can provide complete 4NU-recovery. Obviously, the proposed QRHIL latch design can also provide complete SNU, 2NU, and 3NU recovery.

2.2 Simulation Results

The QRHIL latch was designed in an advanced 22 nm CMOS technology from GlobalFoundries and extensive simulations using Synopsys HSPICE were performed. The PMOS transistors had the ratio W/L = 90/22nm, and the NMOS transistors had the ratio W/L = 45/22nm. The supply voltage was set to 0.8 V, and the working temperature was set to room temperature. Figure 3 shows the simulation result for the error-free case of the proposed QRHIL latch design. The simulation result shows that the normal operation of the latch in transparent and hold mode is similar to that of a traditional D-latch.

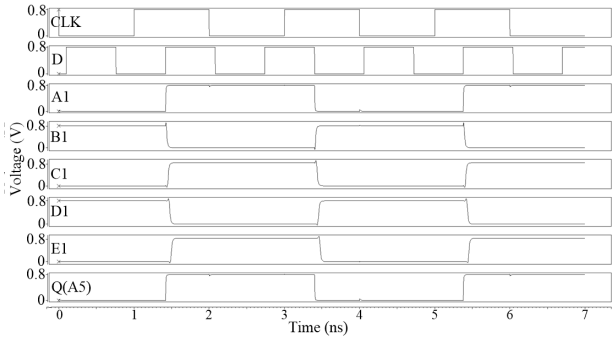

Figure 3: Simulation result for the error-free case of the proposed QRHIL latch.

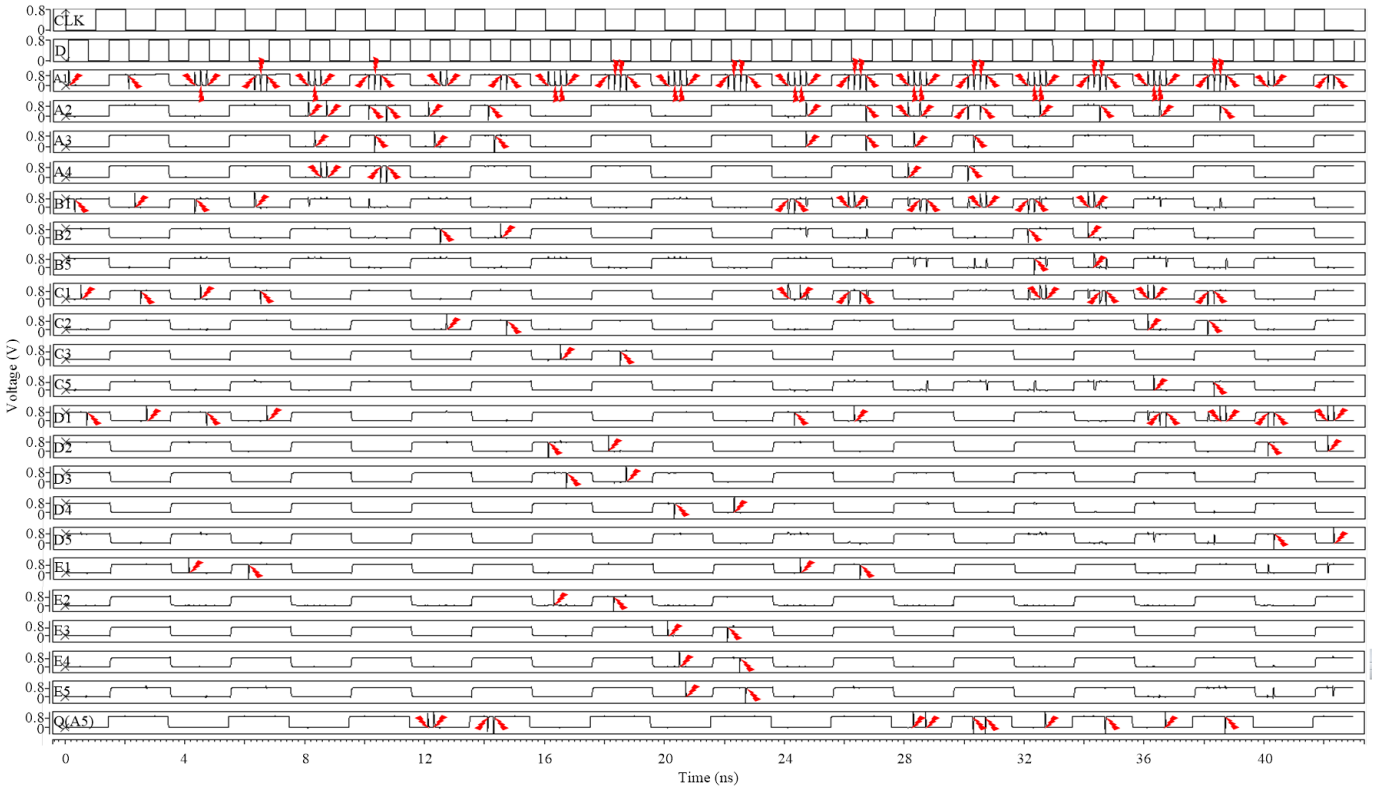

Figure 4. Simulation results for the key SNU, 2NU, and 3NU injections of the QRHIL latch.

In the following SNU/2NU/3NU/4NU injection simulations, a controllable double-exponential-current-source model was used as in [4, 17, 18, 21]. Figure 4 shows the simulation results for the key SNU, 2NU and 3NU injections of the QRHIL latch. Note that the lighting marks in Figure 4 denote the injected errors. Also note that, since B3, B4, C4 are not affected by the injections, the simulation results of these nodes are not shown for brevity.

Firstly, because of the symmetry construction of the latch, we need to consider the situations where 5 indicative nodes A1, B1, C1, D1 and E1 are affected by an SNU, respectively. As shown in Figure 4, when Q = 0, an SNU was injected on nodes A1, B1, C1, D1 and E1 at 0.1ns, 0.3ns, 0.5ns, 0.7ns and 4.1ns, respectively. Note that, for the reverse states of the above nodes, SNU-injections were also performed. It can be seen that the latch can self-recover from these SNUs.

Secondly, 2NUs are considered. After investigation, key node-pairs include <A1, B1>, <A1, C1>, <A1, D1>, <A1, A2>, <A1, A3>, <A1, A4>, <A2, A4>, <A2, A5>, <A3, A5>,<A1, B2>, <A1, C2>, <A1, D2>, <A1, E2>, <A1, C3>, <A1, D3>, <A1, E3>, <A1, D4>, <A1, E4> and <A1, E5>. In Figure 4, when Q = 0, a 2NU was injected to these pairs at 4.3ns, 4.5ns, 4.7ns, 8.1ns, 8.3ns, 8.5ns, 8.7ns, 12.1ns, 12.3ns, 12.5ns, 12.7ns, 16.1ns, 16.3ns, 16.5ns, 16.7ns, 20.1ns, 20.3ns, 20.5ns and 20.7ns, respectively. Note that, for the reverse states of the node-pairs, 2NU-injections were also performed. It can be seen that the latch can self-recover from these 2NUs.

Thirdly, 3NUs are considered. After investigation, key node-pairs include <A1, B1, C1>, <A1, B1, D1>, <A1, C1, E1>, <A1, A2, A3>, <A1, A2, A4>, <A1, A3, A5>, <A1, B1, A2>, <A1, B1, A5>, <A1, B1, B2>, <A1, B1, B5>, <A1, C1, A2>, <A1, C1, A5>, <A1, C1, C2>, <A1, C1, C5>, <A1, D1, A2>, <A1, D1, A5>, <A1, D1, D2> and <A1, D1, D5>. In Figure 4, when Q = 0, a 3NU was injected to these lists at 24.1ns, 24.3ns, 24.5ns, 24.7ns, 28.1ns, 28.3ns, 28.5ns, 28.7ns, 32.1ns, 32.3ns, 32.5ns, 32.7ns, 36.1ns, 36.3ns, 36.5ns, 36.7ns, 40.1ns and 40.3ns, respectively. Note that, for the reverse states of the node-lists, 3NU-injections were also performed. It can be seen that the latch can self-recover from these 3NUs.

Figure 5 shows the simulation results for the key 4NU injections of the QRHIL latch design. Note that statistic results for the 4NU injections of the QRHIL latch design according to Figure 5 is not shown due to page limitation. Based on the previous 4NU discussions, node-lists <A1, B1, C1, D1>, <A1, B1, C1, A2>, <A1, B1, C1, A5>, <A1, B1, C1, B2>, <A1, B1, C1, B5>, <A1, B1, C1, C2>, <A1, B1, C1, C5>, <A1, B1, A2, B2>, <A1, B1, A5, B5>, <A1, B1, A2, A3>, <A1, B1, A2, A5>, <A1, B1, B2, B3>, <A1, B1, B2, B5>, <A1, B1, A2, B5>, <A1, B1, A5, B2> and <A1, A2, A3, A4> were considered for 4NU injections, respectively. In Figure 5, when Q = 0, a 4NU was injected to these node-lists at 0.1ns, 0.3ns, 0.5ns, 0.7ns, 4.1ns, 4.3ns, 4.5ns, 4.7ns, 8.1ns, 8.3ns, 8.5ns, 8.7ns, 12.1ns, 12.3ns, 12.5ns and 12.7ns, respectively. Note that, for the reverse states of the node-lists, 4NU-injections were also performed. It can be seen that the latch can self-recover from these 4NUs.

In summary, all the above discussions show that the proposed QRHIL latch design can provide complete SNU, 2NU, 3NU, and 4NU self-recovery, thus providing very high reliability for reliable computing of safety-critical applications especially in harsh radiation environments.

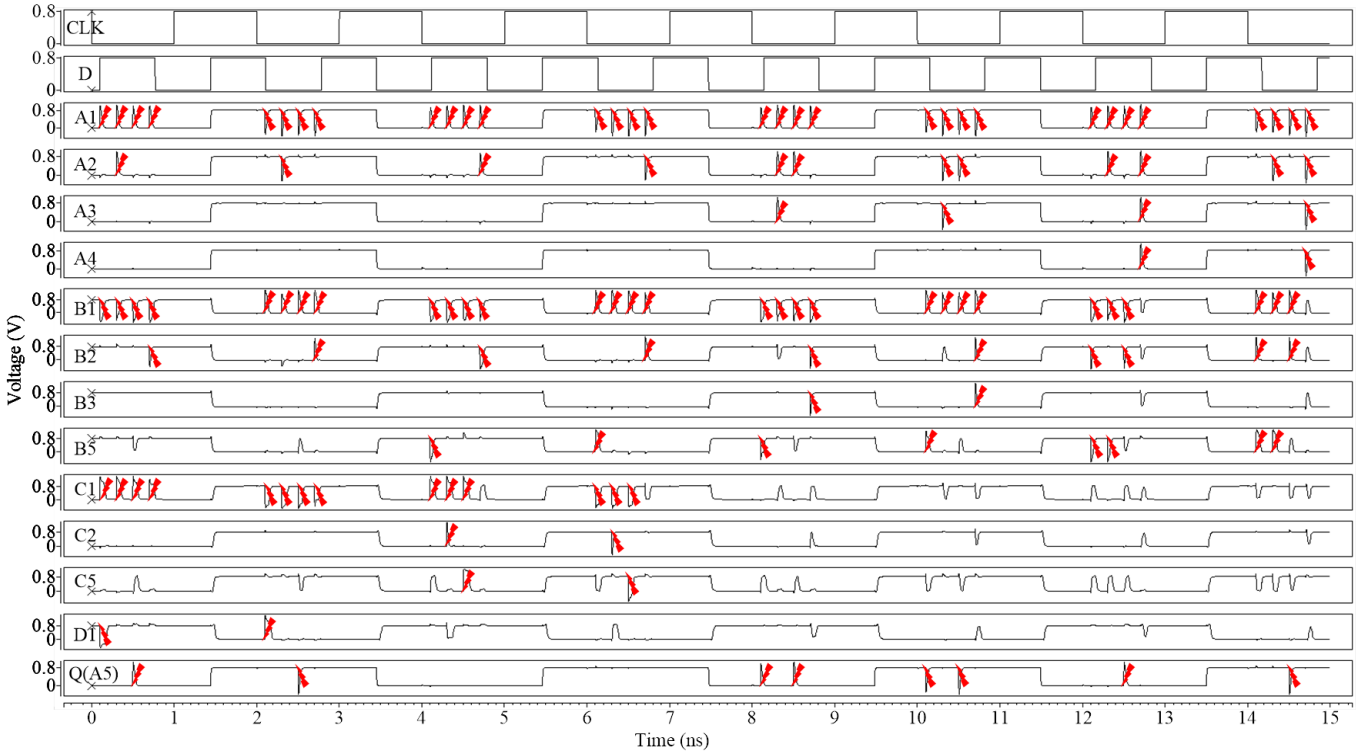

Figure 5. Simulation results for the key 4NU injections of the QRHIL latch.

TABLE 1: Reliability and Overhead comparisons Among the SNU, 2NU, 3NU and/or 4NU Hardened Latches.

Latch	SNU Tol.	SNU Rec.	2NU Tol.	2NU Rec.	3NU Tol.	3NU Rec.	4NU Tol.	4NU Rec.	HIS Ins.	D-Q Delay (ps)	CLK-Q Delay (ps)	Power (μW)	Area (μm2)
HRLC [12]	√	×	×	×	×	×	×	×	×	43.93	43.76	0.75	3.86
DICE [13]	√	√	×	×	×	×	×	×	√	7.08	7.15	0.49	2.38
HLDTL-EV [14]	√	×	√	×	×	×	×	×	×	1.63	1.64	0.77	6.53
DIRT [15]	√	√	√	×	×	×	×	×	√	6.73	6.63	1.12	5.35
RH [16]	√	√	√	×	×	×	×	×	×	1.61	1.63	0.83	5.45
DNURL [17]	√	√	√	√	×	×	×	×	√	3.12	3.12	1.18	9.80
LCTNUT [18]	√	√	√	×	√	×	×	×	×	1.63	1.66	0.67	7.13
TNUHL [19]	√	√	√	×	√	×	×	×	×	1.63	1.65	2.08	5.35
TNUTL [20]	√	√	√	×	√	×	×	×	×	97.85	97.51	1.35	12.18
TNURL [21]	√	√	√	√	√	√	×	×	√	5.44	5.47	1.18	19.01
QRHIL (proposed)	√	√	√	√	√	√	√	√	√	2.93	2.95	1.95	19.31

3 Comparison Results

For fair comparisons, typical SNU, 2NU, 3NU and/or 4NU hardened latches, such as the HRLC [12], DICE [13], HLDTL-EV [14], DIRT [15], RH [16], DNURL [17], LCTNUT [18], TNUHL [19], TNUTL [20] and TNURL[21], were implemented under in the same conditions as the proposed QRHIL latch (i.e., the transistor sizes of these latches were set to the same as those of the QRHIL latch, and the supply voltage 0.8V and the room temperature were also used for these latches).

Table 1 shows the reliability and overhead comparisons among these hardened latches. In Table 1, "Tol." means "tolerant", "Rec." means "recoverable", "Ins." means "Insensitive", "Area" means the silicon area measured through layout, "D-Q Delay" means the average of the delays (rise and fall) from D to Q, "Power" means the average of the power dissipation (dynamic and static), and "CLK-Q Delay" means the average of the delays (rise and fall) from CLK to Q. It can be seen from Table 1 that the proposed QRHIL latch has 9 "√" marks demonstrating that the proposed latch can provide the highest reliability compared to these hardened latches.

These latches are also compared in terms of overhead. For the proposed latch and some existing hardened latches, such as the HLDTL-EV, RH, DNURL, LCTNUT, TNUHL and TNURL, their D-Q delay is small since there is a high-speed path from D to Q for any of them. It can be seen from Table 1 that the CLK-Q delay is close to the D-Q delay since they are related to the used devices from D to Q. For the proposed latch and some existing hardened latches, their CLK-Q delay is small since their D-Q delay is small.

For power dissipation, the TNUHL latch consumes the highest power since the latch has much current competition to ensure complete node-upset recovery. Note that, when a latch has a large

area and/or does not use the CG approach, its power consumption is large. Since the proposed latch uses redundant silicon area to provide complete 4NU recovery, its power dissipation is not small. Indeed, compared with the TNURL latch that is not 4NU-tolerant/recoverable, the proposed latch consumes more power. For silicon area, compared with the HRLC, DICE, HLDTL-EV, DIRT, RH, DNURL, LCTNUT and TNUHL latches, the TNUTL, TNURL and the proposed QRHIL latch require more area since they use redundant transistors to achieve high reliability. In summary, the proposed QRHIL latch can provide complete 4NU-recovery but mainly at the cost of silicon area.

Among the compared hardened latches, the TNURL latch has 7 "√" marks. To show quantitative comparison results, we compared the TNURL latch with the proposed latch. We can draw a conclusion from Table 1 that the proposed QRHIL latch saves approximately 46.14% D-Q delay and 46.07% CLK-Q delay, compared with the TNURL latch. In summary, the proposed QRHIL latch can provide high reliability but at the cost of indispensable overhead.

4 Conclusions

This paper has for the first time proposed a novel and completely 4NU-recoverable latch (namely QRHIL) for harsh radiation environment. The QRHIL latch mainly consists of a 5×5 CE matrix. The latch can robustly store values since it can recover from any possible SNUs, 2NUs, 3NUs and 4NUs; thus, it is also HIS insensitive. Simulation results have demonstrated the SNU-, 2NU-, 3NU-, and 4NU-recovery of the QRHIL latch. Moreover, using a high-speed path and the clock-gating technology, the overhead of the QRHIL latch is moderate especially in terms of delay and power, compared with the state-of-the-art latches.

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