Dual-modular-redundancy and dual-level error-interception based triple-node-upset tolerant latch designs for safety-critical applications

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Dual-Modular-Redundancy and Dual-Level Error-Interception based Triple-Node-Upset Tolerant Latch Designs for Safety-Critical Applications

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***Abstract*—This paper presents a dual-modular-redundancy and dual-level error-interception based triple-node-upset (TNU) tolerant latch design (namely DDETT) for safety-critical applications. The DDETT latch comprises two parallel single-node-upset self-recoverable cells to store values and three C-elements to intercept errors. Both of the two cells are constructed from triple mutually-feeding-back 2-input C-elements, and the cells feed two internal C-elements for first-level error-interception. Moreover, the two internal C-elements feed an output-stage C-element for second-level error-interception, making the DDETT latch TNU-tolerant in that it can tolerate any possible TNU. This paper further presents a low-cost version of the DDETT latch, namely LCDDETT. The LCDDETT latch uses two dual-interlocked-storage-cells (DICEs) to store values and uses dual-level error-interception to tolerate any possible TNU with cost-effectiveness. Simulation results not only confirm the TNU-tolerance of the proposed latches but also demonstrate that the delay-power-area products of the DDETT and LCDDETT latches are reduced by approximately 34% and 58%, respectively.**

***Index Terms*—triple-node upset, latch design, self-recoverability, low-cost, fault-tolerance**

I. Introduction

With CMOS technology scaling, the strike of high-energy radiative particles, such as neutrons, protons, alpha particles, and electrons, can easily result in soft errors, such as single-node upsets (SNUs), double-node upsets (DNUs), and even triple-node upsets (TNUs) [1]. Soft errors are transient errors, meaning that the affected circuit is not physically damaged and the errors can be eliminated by data reloading or on-line self-recovering through the radiation-hardening-by-design (RHBD) approach. It is reported that, in advanced nano-scale CMOS technologies, the TNU issue is becoming more and more severe for circuit reliability [2]. This is because, under charge-sharing mechanisms, the logic state of adjacent circuit nodes are becoming more and more easily disturbed by high-energy-particle striking [2-3]. Therefore, not only SNUs and DNUs but also TNUs should be considered for radiation hardening in advanced safety-critical nano-scale circuits, such as memory cells [3-6], flip-flops [7-9], and latch designs [1-2, 10-27].

For high-reliability-required nano-scale circuits, RHBD is a widely used approach to mitigate soft errors. This paper mainly targets radiation-hardened latch designs. Previous hardened latch designs mainly focus on SNU and/or DNU hardening [10-15, 18-19] based on techniques, including Dual-Modular Redundancy (DMR), Triple-Modular Redundancy (TMR), Mutual-Interlock Construction for Nodes (MICN), and so on. Some of the latch designs, such as the FEedback Redundant SNU-Tolerant (FERST) [10], the Interlocking Soft Error Hardened Latch (ISEHL) [11], the TMR [12] and the Highly Reliable SEU/SET hardened (HRUT) [13], are typically SNU hardened. These designs employ the DMR, TMR, and MICN technologies, respectively. Since IC designers and researchers have already found that SNU mitigation only is insufficient for safety-critical applications, many DNU hardened latch designs have been proposed, including the Dual-input Inverter Radiation Tolerant (DIRT) [14], the Double-Node-Upset-Resilient (DNUR) [15], and the designs in [18-19]. Moreover, in the past three years, researchers have started to consider TNU hardening for safety-critical applications [1-2, 17, 26-27]. Although these schemes can provide complete TNU tolerance, they severely suffer from very large overhead, especially in terms of transmission delay and delay-power-area-product (DPAP).

Based on the RHBD approach, this paper presents a dual-modular-redundancy and dual-level error-interception based TNU-tolerant latch, namely DDETT. The DDETT latch mainly comprises two parallel SNU-self-Recoverable and Frequency-aware Cells (RFCs) for retaining values as well as

Manuscript received September 16, 2020; revised ???; accepted ???. Date of publication ???; This work was supported in part by the National Natural Science Foundation of China under Grants 61974001, 61874156, 61674048, 61872001, 61904001, 61834006, and 61604001. This work was also supported in part by Japan Society for the Promotion of Science (JSPS) under JSPS Grant-in-Aid for Scientific Research (B) #17H01716.

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three C-elements (CEs) for Dual-Level Error-Interception (DLEI), providing the latch with complete TNU/DNU/SNU tolerance. To reduce overhead, a low-cost version of the DDETT, namely LCDDETT, is further proposed. The LCDDETT latch has the same soft error tolerance as the DDETT latch. However, by using two dual-interlocked-storage-cells (DICEs) instead of RFCs to store values, the LCDDETT latch has smaller overhead in terms of power dissipation, silicon area and DPAP. Simulation results demonstrate the TNU/DNU/SNU tolerance and cost-effectiveness of the proposed latches compared with state-of-the-art TNU-tolerant latch designs.

The rest of the paper is organized as follows. Section II reviews typical latch designs. Section III presents the schematic, working principles, and verifications of the proposed latches. Section IV provides comparison and evaluation results. Section V concludes the paper.

II. Existing Latch Designs

This section reviews typical state-of-the-art latch designs, including the traditional unhardened latch, FERST [10], ISEHL [11], TMR [12], HRUT [13], DNUR [15], TNU-Tolerant Latch (TNUTL) [16], TNU Hardened Latch (RHLD) [17], Low Cost and TNU completely Tolerant (LCTNUT) [26], TNU-Hardened Latch (TNUHL) [27], and Triple-Node-Upset self-Recoverable Latch (TNURL) [2]. In these hardened latch designs, C-elements (CEs) are widely used. Figure 1 shows the schematics of 2-input and 3-input CEs including the clock-gating (CG) based CEs. When the input values of a CE are identical, the CE behaves as an inverter. However, when its input values change to be different, it retains the previous value on its output temporally (enters into high-impedance state). This means that if the change of values at the inputs of the CE is caused by an error, the CE can hence intercept this error. The CG based CEs can be controlled by the system clock (CLK) and negative system clock (NCK) signals. From Fig. 1, it is easy to create 4-input CEs.

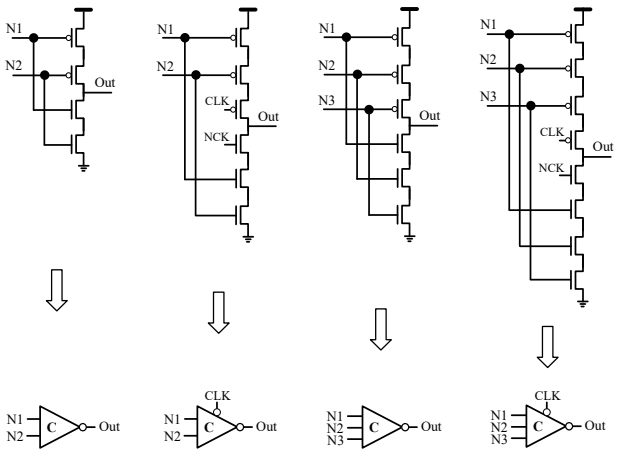

Fig. 1. Schematics of widely used C-elements. (a) 2-input, (b) Clock-gating based 2-input, (c) 3-input, and (d) Clock-gating based 3-input.

Figure 2 shows the schematics of typical latch designs. It should be noted that the switches marked with NCK or CLK are transmission gates (TGs). The TGs with input D marked with NCK denote that the gate terminals of pMOS and nMOS transistors of the TGs are respectively connected with NCK and CLK. This rule applies for all NCK-marked TGs in all latches in this paper. Figure 2-(a) shows the traditional unhardened latch. It simply uses two feeding-back inverters to create a feedback loop to retain values and thus it cannot effectively tolerate SNUs.

The FERST latch [10] in Fig. 2-(b) mainly uses an inverter and a CE on the left side to construct feedback loops, feeding an output-level CE. The latch employs DMR and CE-based single-level error-interception (SLEI). The output-level weak-keeper is used for avoiding high-impedance state (HIS) of the CE. However, the inputs of the output-level CE can be flipped due to a DNU. Therefore, the latch cannot provide complete DNU tolerance.

Figure 2-(c) shows the schematic of the SNU-self-recoverable ISEHL latch [11], which consists of three 2-input CEs and two inverters, and the inputs of each 2-input CEs are determined by the outputs of two other 2-input CEs. However, the inputs of the output-level CE can similarly be flipped due to a DNU. Therefore, the latch cannot provide complete DNU tolerance, either.

Figure 2-(d) shows the schematic of the TMR latch [12]. It employs triple unhardened latches with a voter. The voter consists of three 2-input AND gates and one 3-input OR gate, resulting in the use of 18 transistors. The TMR latch can tolerate SNUs, but cannot tolerate DNUs.

Figure 2-(e) shows the schematic of the HRUT latch [13], which consists of four 2-input CEs and three inverters. The HRUT latch can self-recover from SNUs. However, the inputs of the output-level CE can be flipped by a DNU. Therefore, the latch cannot provide DNU tolerance, either.

Figure 2-(f) shows the schematic of the DNUR latch [15], which is mainly constructed from triple interlocked RFCs [20] and every RFC is based on MICN to self-recover from any SNU. Thus, the latch can provide complete DNU tolerance. However, in the worst case where N2, N3 and N4 are simultaneously flipped by a TNU, the latch will output an incorrect value.

Figure 2-(g) shows the schematic of the TNUTL latch [16]. The latch mainly consists of a triple-level error-interception module (TEM) and an inverter. The TEM includes five input-split 3-input CEs and a 2-input CE. Due to the multiple-level error-interception of CEs, the TNUTL latch can tolerate SNUs, DNUs, and TNUs. However, the latch has no any feedback loop. As a result, it cannot store values for a long time.

To tolerate any possible TNU, the RHLD latch [17] in Fig. 2-(h) employs four 4-input CEs to construct many feedback loops to robustly retain values. Meanwhile, using multiple-level error-interception (MLEI) in the four CEs on the right, the latch can tolerate any possible TNU. However, the latch has large overhead in terms of area, power, and delay.

Figure 2-(i) shows the schematic of the LCTNUT latch [26]. The latch mainly consists of a storage module (SM) and a two-level soft-error-interceptive module (SIM). The SM includes eight input-split inverters that include four CG-based ones. The LCTNUT latch can tolerate any possible TNU.

However, the devices in the SM are adjacent, leading to high charge-sharing possibility. To alleviate this issue, we use two independent RFCs to construct an SM to lower the charge-sharing possibility that will be introduced in the next section.

Figure 2-(j) shows the schematic of the TNUHL latch [27]. The latch mainly consists of two restorer circuit (RC) cells and a CG based 2-input CE. The TNUHL latch can tolerate any possible TNU. However, the latch has large overhead, especially in terms of power, due to current competition among storage nodes.

Figure 2-(k) shows the schematic of the TNURL latch [2]. The latch mainly consists of seven SIMs so as to achieve TNU-recoverability. However, the latch has large overhead in

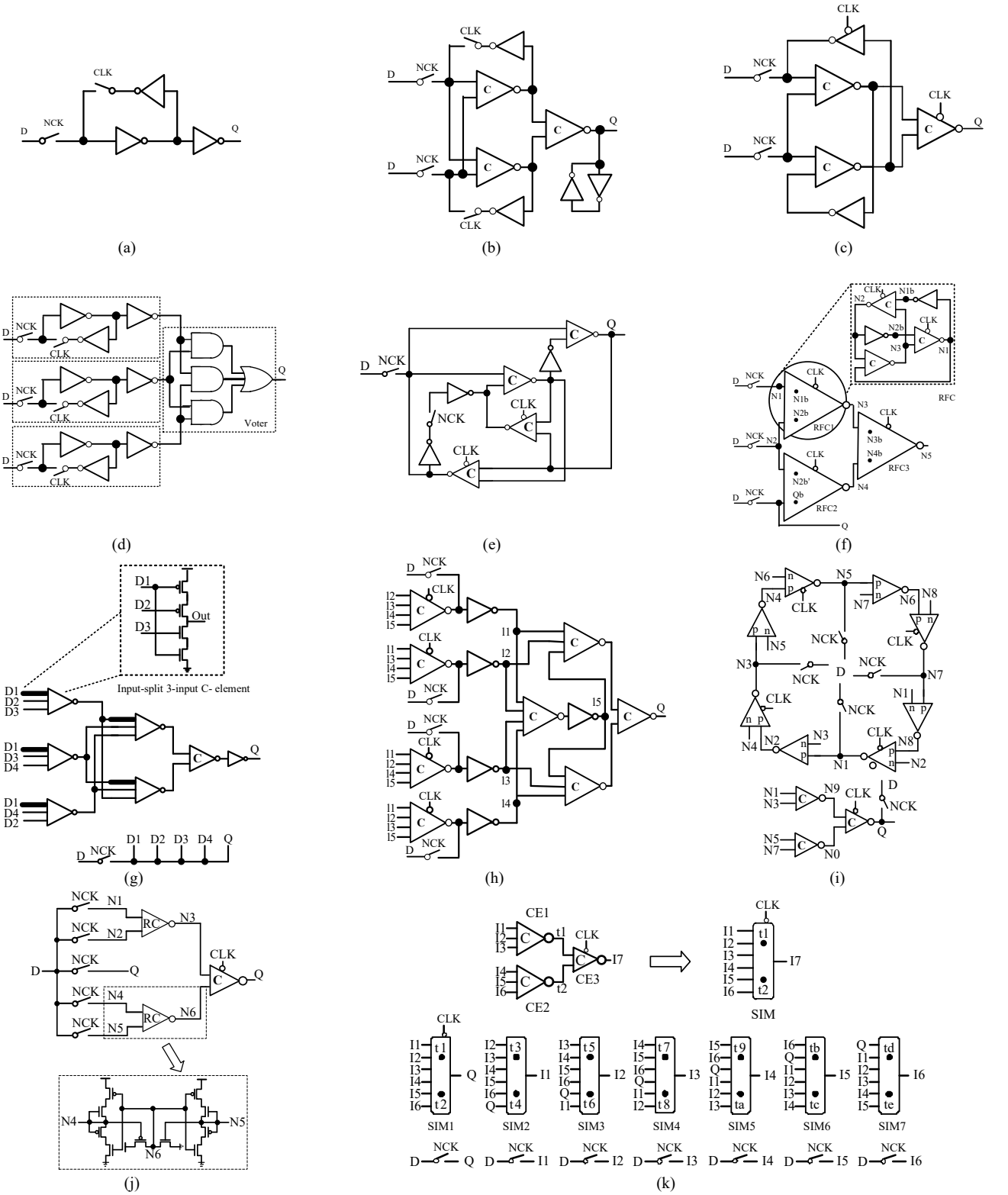

Fig. 2. Schematics of typical latch designs. (a) Unhardened, (b) FERST [10], (c) ISEHL [11], (d) TMR [12], (e) HRUT [13], (f) DNUR [15], (g) TNUTL [16], (h) RHLD [17], (i) LCTNUT [26], (j) TNUHL [27], and (k) TNURL [2].

terms of area, power, and delay. Detailed overhead discussions will be introduced in Section IV.

III. Proposed Latch Designs

A. Circuit Structure and Behavior of the DDETT latch

Figure 3 shows the circuit schematic of the proposed Dual-modular-redundancy and Dual-level Error-interception based TNU-Tolerant (DDETT) latch design. The DDETT latch consists of two parallel RFCs (RFC1 and RFC2) as shown in Fig. 2-(f), two 2-input CEs (CE1 and CE2) as shown in Fig. 1-(a), one CG-based 2-input CE (CE3) as shown in Fig. 1-(b), and five TGs as shown in the left part of Fig. 3. Based on MICN, each RFC is constructed from three mutually feeding-back CEs for retaining values, and two of these CEs are CG-based and used for avoiding positive feedback loops, leading to reduced power dissipation. CE1 and CE2 are used for first-level error-interception, CE3 is used for second-level error-interception, and the TGs are used for value initialization. In the DDETT latch, D, Q, CLK, and NCK are the input, output, system clock, and negative system clock ports, respectively. Figure 4 shows the layout of the proposed DDETT latch.

When CLK = 1 and NCK = 0, the latch works in transparent mode. The TGs are ON, and thus the internal nodes N1, N2, N4, N5 as well as Q are pre-charged. Subsequently, the signals of N1b, N2b, N4b, N5b, N3, and N6, N7, N8 can be obtained. Note that Q is only determined through a TG instead of the output of CE3 since the output of CE3 is blocked through CLK and NCK, to reduce current competition on Q and transmission delay from D to Q in transparent mode. In addition, to further reduce power dissipation, the current competition in the RFCs is also avoided by the CG technique.

When CLK = 0 and NCK = 1, the latch switches to hold mode. The TGs are OFF, and the CG-based transistors in the RFCs are ON, thus the feedback loops are constructed in the RFCs to retain values. Meanwhile, Q is only driven by N7 and N8 through CE3 and CE3 outputs the retained value to Q. Next, we discuss the SNU/DNU/TNU tolerance principles for the latch in hold mode. It can be seen that, if N1 is affected, N1b will also be affected. Hence, for the SNU/DNU/TNU tolerance discussion, we only need to consider the worst case in which N1 instead of N1b is affected. In other words, it is only necessary to consider N1 through N8 and Q in error tolerance discussion. Note that, similarly to the other papers, the cases where CLK and NCK have the same values or have soft errors are not considered either.

For SNUs, since the RFCs work as storage modules that are SNU-self-recoverable [20], the latch is also SNU-self-recoverable and obviously the latch can tolerate SNUs. For DNUs, since the RFCs are symmetrically constructed, only the following cases need to be considered. (a) No RFC is affected, and the key node-pairs are <N7, N8> and <N7, Q>. (b) Both RFCs are affected, and the key node-pairs are <N1, N4>, <N1, N5>, and <N1, N6>. (c) A single RFC is affected, and the key node-pairs are <N1, N2>, <N1, N3>, <N1, N7>, <N1, N8>, and <N1, Q>. The DNU tolerance principles are discussed below.

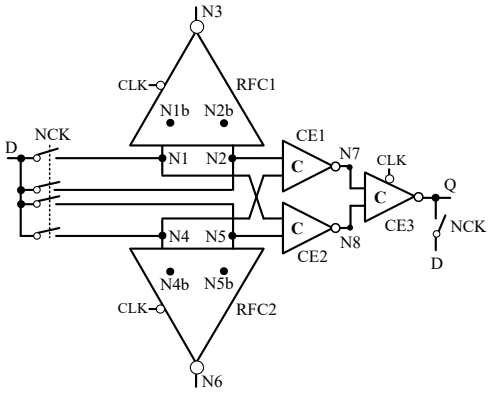

Fig. 3. Schematic of the proposed DDETT latch.

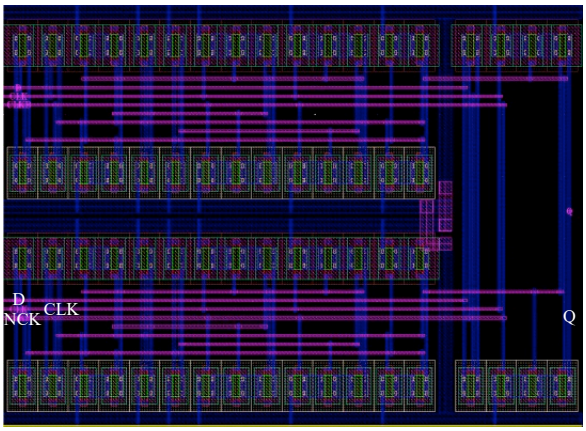

Fig. 4. Layout of the proposed DDETT latch.

In the case of (a), since the RFCs are error-free, they can refresh the errors in the downstream devices, i.e., the latch is DNU-self-recoverable in this case. In the case of (b), each RFC has to suffer from an SNU, but the RFCs are SNU-self-recoverable. Thus, the RFCs can remove the errors, i.e., the latch is DNU-self-recoverable in this case. In the case of (c), when any two of N1, N2, and N3 suffer from a DNU, all nodes in RFC1 will be flipped to wrong values since the affected RFC cannot provide DNU tolerance [20]. However, due to the SLEI mechanism provided from CE1 and CE2, the wrong values can be masked by CE1 and CE2, i.e., CE1 and CE2 can still output correct values. Thus, the latch still has correct values on Q. Moreover, when one node of one RFC together with one node among N7, N8 and Q are affected by a DNU, the latch can self-recover from the errors since the SNU-self-recoverable RFC can first self-recover and then the downstream nodes can be refreshed to correct states. In summary, the latch tolerates any possible DNU.

For TNUs, since the RFCs are symmetrically constructed, only the following cases need to be considered. (a) No RFC is affected, and the key node-list is only <N7, N8, Q>. (b) A single RFC is affected, and the key node list is only <N1, N2, N3>. (c) Both RFCs are affected, and the key node lists are <N1, N2, N4>, <N1, N2, N6>, <N1, N4, N7>, <N1, N4, Q>, <N1, N6, N7>, and <N1, N6, Q>. The TNU tolerance principles are discussed in the following.

In the case of (a), since the RFCs are error-free, they can

refresh the errors in the downstream devices, i.e., the latch is TNU-self-recoverable in this case. In the case of (b), as mentioned above, the affected RFC cannot provide DNU tolerance, and thus all nodes in a TNU-affected RFC will flipped to wrong values. However, the wrong values can be masked by CE1 and CE2, i.e., CE1 and CE2 can still output correct values. Thus, the latch still has correct values on Q. In other words, the latch tolerates any possible TNU in this case. In the case of (c), if the key node lists contain N1 and N2, this case is similar to the above case (b). Otherwise, there will be only one node in any RFC that is affected. However, since any RFC can self-recover from any SNU, the affected nodes N1 and N4 (or N1 and N6) can firstly self-recover from the TNU, making the RFCs refresh the errors on N7 and Q. In other words, the latch tolerates any possible TNU in this case. In summary, the latch tolerates any possible TNU.

B. Circuit Schematic and Behavior of the LCDDETT Latch

Figure 5 shows the circuit schematic of the proposed Low-Cost version of the DDETT (namely LCDDETT) latch design. The LCDDETT latch consists of two parallel CG-based DICEs (DICE1 and DICE2), two 2-input CEs (CE1 and CE2), one CG-based 2-input CE (CE3), and five TGs as shown in Fig. 5. The DICEs are used to retain values. CE1 and CE2 are used for first-level error-interception, CE3 is used for second-level error-interception, and the TGs are used for value initialization. In the LCDDETT latch, D, Q, CLK, and NCK are the input, output, system clock, and negative system clock ports, respectively. Figure 6 shows the layout of the proposed LCDDETT latch.

When CLK = 1 and NCK = 0, the latch works in transparent mode. The TGs are ON, and thus the internal nodes N2, N4, N6, N8 as well as Q are pre-charged. Subsequently, the signals of N1, N3, N5, N7, N9, and N10 can be obtained. Note that Q is only determined through a TG instead of the output of CE3 since the output of CE3 is blocked through CLK and NCK, to reduce current competition and transmission delay in transparent mode. In addition, to further reduce power dissipation, the current competition in the DICEs is also avoided by the CG technique.

When CLK = 0 and NCK = 1, the latch switches to hold mode. The TGs are OFF, and the CG-based transistors in the DICEs are ON, thus the feedback loops are constructed in the DICEs to retain values. Meanwhile, Q is only driven by N9 and N10 through CE3 and CE3 outputs the retained value to Q. Next, we discuss the SNU/DNU/TNU tolerance principles for the latch in hold mode.

For SNUs, since the DICEs work as storage modules that are SNU-self-recoverable [21], the latch is also SNU-self-recoverable and obviously the latch can tolerate SNUs. For DNUs, since the DICEs are symmetrically constructed, only the following cases need to be considered. (a) No DICE is affected, and the key node-pairs are <N9, N10> and <N9, Q>. (b) Both DICEs are affected, and the key node-pairs are <N2, N5>, <N2, N6>, <N2, N7>, and <N2, N8>. (c) A single DICE is affected, and the key node-pairs are <N1, N2>, <N1, N3>, <N2, N4> and <N2, N9>, <N2, N10>, and <N2, Q>. The DNU tolerance principles are discussed below.

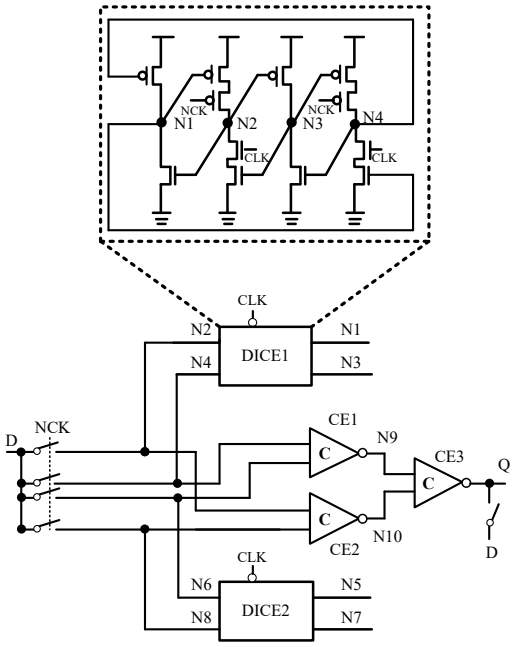

Fig. 5. Schematic of the proposed LCDDETT latch.

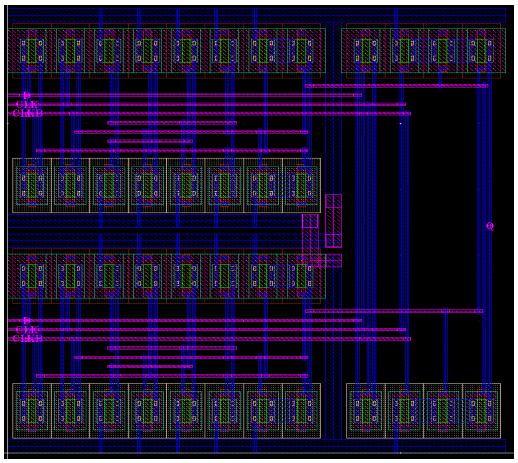

Fig. 6. Layout of the proposed LCDDETT latch.

In the case of (a), since the DICEs are error-free, they can refresh the errors in the downstream devices, i.e., the latch is DNU-self-recoverable in this case. In the case of (b), each DICE has to suffer from an SNU, but the DICEs are SNU-self-recoverable. Thus, the DICEs can remove the errors, i.e., the latch is DNU-self-recoverable in this case. In the case of (c), when two of N1, N2, N3, and N4 suffer from a DNU, all nodes in DICE1 will be flipped to wrong values since the affected DICE cannot provide DNU tolerance in the worst case [21]. However, due to the SLEI mechanism provided from CE1 and CE2, the wrong values can be masked by CE1 and CE2, i.e., CE1 and CE2 can still output correct values. Thus, the latch still has a correct value on Q. Moreover, when one node of one DICE together with one node among N9, N10 and Q are affected by a DNU, the latch can self-recover from the errors since the SNU-self-recoverable DICE can first self-recover and then the downstream nodes can be refreshed to correct states. In

summary, the latch tolerates any possible DNU.

For TNUs, since the DICEs are symmetrically constructed, only the following cases need to be considered. (a) No DICE is affected, and the key node-list is only <N9, N10, Q>. (b) A single DICE is affected, and the key node-lists are<N1, N2, N3> and <N1, N2, N4>. (c) Both DICEs are affected, and the key node-lists are <N2, N1, N6>, <N2, N4, N6>, <N2, N6, N9>, <N2, N6, Q>, <N2, N7, N9>, and <N2, N7, Q>. The TNU tolerance principles are discussed below.

In the case of (a), since the DICEs are error-free, they can refresh the errors in the downstream devices, i.e., the latch is TNU-self-recoverable in this case. In the case of (b), as mentioned above, the affected DICE cannot provide DNU tolerance in the worst case, and thus it is obvious that all nodes in a TNU-affected DICE will flip to wrong values. However, the wrong values can be masked by CE1 and CE2, i.e., CE1 and CE2 can still output correct values. Thus, the latch still has a correct value on Q. In other words, the latch tolerates any possible TNU in this case. In the case of (c), if the key node lists contain N2 and N6, this case is similar to the above case (b). Otherwise, there will be only one node in any RFC that is affected. However, since any DICE can self-recover from any SNU, the affected nodes N2 and N6 (or N2 and N7) can firstly self-recover from the TNU, making the DICEs refresh the errors on N9 and Q. In other words, the latch tolerates any possible TNU in this case. In summary, the latch tolerates any possible TNU.

C. *Simulation Results*

The proposed latches (DDETT and LCDDETT) were designed in a 22nm CMOS technology from GlobalFoundries. The supply voltage was set to 0.8V and the temperature was set to the room temperature. As in [1-2], pertinent simulations using Synopsys HSPICE were performed. For fault injections, a double exponential current source model was used and the rise and fall time constants of current pulses were set to be 0.1ps and 3.0ps, respectively [15]. The injected charge was up to 25fC, which is high enough to consider all the worst cases so as to validate the SNU, DNU, and TNU tolerance of the proposed latches. The transistor sizes of the proposed latches were optimized such that the pMOS transistors had W/L = 32/22nm and the nMOS transistors had W/L = 28/22nm.

Figure 7 shows the simulation results of error-free cases for the DDETT latch. It can be seen from Fig. 7 that, when CLK = 1 and NCK = 0, the signal on D can propagate to Q, and when CLK = 0 and NCK = 1, the sampled state of D can be stored in the latch, meaning that the operation of the latch is similar to that of a conventional latch. This validates the correct operation capability of the DDETT latch. Note that the NCK signal is omitted in subsequent figures for the sake of brevity.

Figure 8 shows the simulation results of the proposed DDETT latch considering all key SNUs on single nodes N1, N2, N3, N7, and Q. When Q = 0, SNUs were injected on these nodes at 0.35ns, 0.70ns, 4.25ns, 4.50ns, and 4.75ns, and when Q = 1, SNUs were injected on these nodes at 2.25ns, 2.50ns, 2.75ns, 6.25ns, and 6.50ns, respectively. The lighting symbols in Figs. 8 to 10 denote the injected errors. Note that a DNU/TNU was represented by simultaneously injecting double/triple SNUs at key nodes in the proposed latches. It can be seen from Fig. 8 that the DDETT latch can self-recover from any possible SNU. Therefore, the DDETT latch is

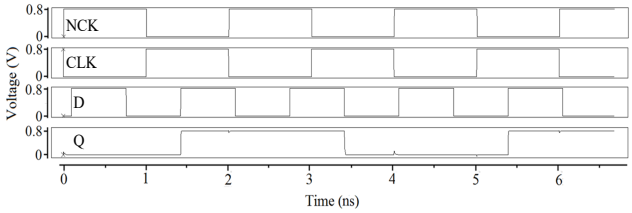

Fig. 7. Simulation results of error-free cases for the DDETT latch.

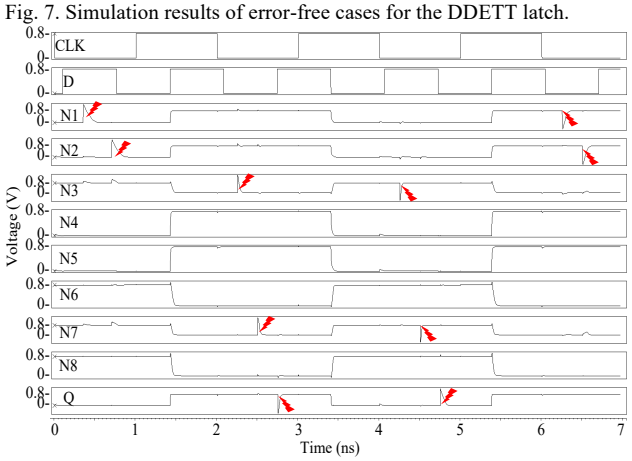

Fig. 8. Simulation results of SNU-injections for the DDETT latch.

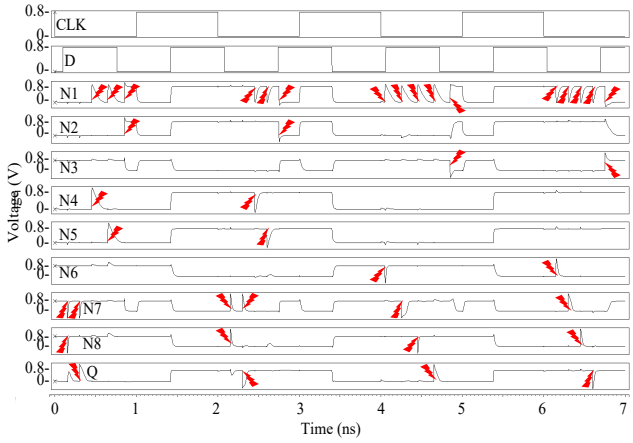

Fig. 9. Simulation results of DNU-injections for the DDETT latch.

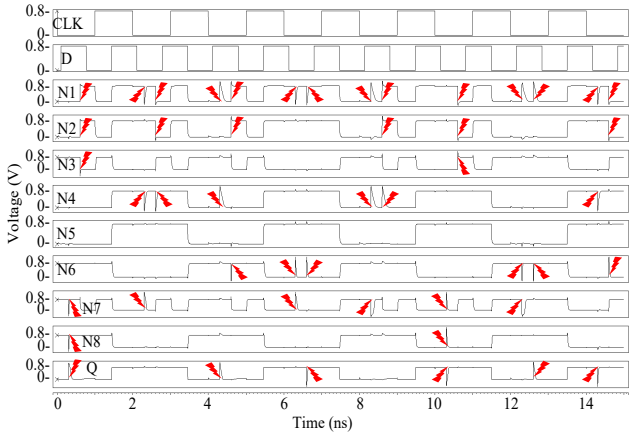

Fig. 10. Simulation results of TNU-injections for the DDETT latch.

SNU-tolerant.

Figure 9 shows the simulation results of the proposed DDETT latch considering all the above-mentioned key-DNUs on node-pairs <N7, N8>, <N7, Q>, <N1, N4>, <N1, N5>, <N1, N2>, <N1, N6>, <N1, N7>, <N1, N8>, <N1, Q>, and <N1, N3>. When Q = 0, DNUs were injected on these node-pairs at 0.15ns, 0.30ns, 0.45ns, 0.65ns, 0.85ns, 4.05ns, 4.25ns, 4.45ns, 4.65ns, and 4.85ns, and when Q = 1, DNUs were injected on these node-pairs at 2.15ns, 2.30ns, 2.45ns, 2.60ns, 2.75ns, 6.15ns, 6.30ns, 6.45ns, 6.60ns, and 6.75ns, respectively. It can be seen from Fig. 9 that the DDETT latch can either self-recover from these DNUs or finally output a correct value on Q although some nodes are flipped. Therefore, the DDETT latch is DNU-tolerant.

Figure 10 shows the simulation results of the proposed DDETT latch considering all the above-mentioned key-TNUs on node-lists <N7, N8, Q>, <N1, N2, N3>, <N1, N4, N7>, <N1, N2, N4>, <N1, N4, Q>, <N1, N2, N6>, <N1, N6, N7>, and <N1, N6, Q>. When Q = 0, TNUs were injected on these node lists at 0.30ns, 0.60ns, 4.30ns, 4.60ns, 8.30ns, 8.60ns, 12.30ns, and 12.60ns, and when Q = 1, TNUs were injected on these node lists at 2.30ns, 2.60ns, 6.30ns, 6.60ns, 10.30ns, 10.60ns, 14.30ns, and 14.60ns, respectively. It can be seen from Fig. 10 that the DDETT latch can either self-recover from these TNUs or finally output a correct value on Q although some nodes are flipped. Therefore, the DDETT latch is TNU-tolerant.

Figure 11 shows the simulation results of error-free cases for the LCDDETT latch. It can be seen from Fig. 11 that, when CLK = 1, the signal on D can propagate to Q, and when CLK = 0, the sampled state of D can be stored in the latch, meaning that the operation of the latch is also similar to that of a conventional latch. This validates the correct operation capability of the LCDDETT latch.

Figure 12 shows the simulation results of the proposed LCDDETT latch considering all key SNUs on single nodes N1, N2, N3, N4, N9, and Q. When Q = 0, SNUs were injected on these nodes at 0.30ns, 0.70ns, 1.10ns, 3.70ns, 4.20ns, and 4.70ns, and when Q = 1, SNUs were injected on these nodes at 1.70ns, 2.20ns, 2.70ns, 5.70ns, 6.20ns, and 6.70ns, respectively. It can be seen from Fig. 12 that the LCDDETT latch can self-recover from any possible SNU. Therefore, the LCDDETT latch is SNU-tolerant.

Figure 13 shows the simulation results of the proposed LCDDETT latch considering all the above-mentioned key-DNUs on node-pairs <N9, N10>, <N9, Q>, <N2, N5>, <N2, N6>, <N2, N7>, <N2, N8>, <N1, N2>, <N1, N3>, <N2, N4>, <N2, N9>, <N2, N10> and <N2, Q>. When Q = 0, DNUs were respectively injected on these node-pairs at 0.20ns, 0.40ns, 0.60ns, 4.30ns, 1.10ns, 1.25ns, 3.70ns, 4.90ns, 0.90ns, 4.60ns, 4.00ns and 5.20ns, and when Q = 1, DNUs were respectively injected on these node-pairs at 1.70ns, 6.10ns, 2.30ns, 2.60ns, 2.90ns, 3.20ns, 5.70ns, 5.90ns, 1.90ns, 6.30ns, 6.50ns, and 6.70ns, respectively. It can be seen from Fig. 13 that the LCDDETT latch can either self-recover from these DNUs or finally output a correct value on Q although some nodes are flipped. Therefore, the LCDDETT latch is DNU-tolerant.

Figure 14 shows the simulation results of the proposed

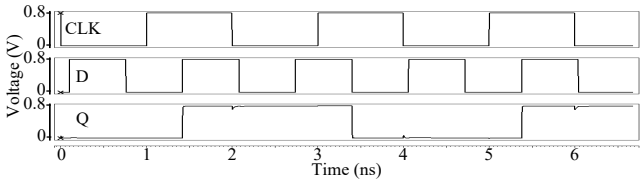

Fig. 11. Simulation results of error-free cases for the LCDDETT latch.

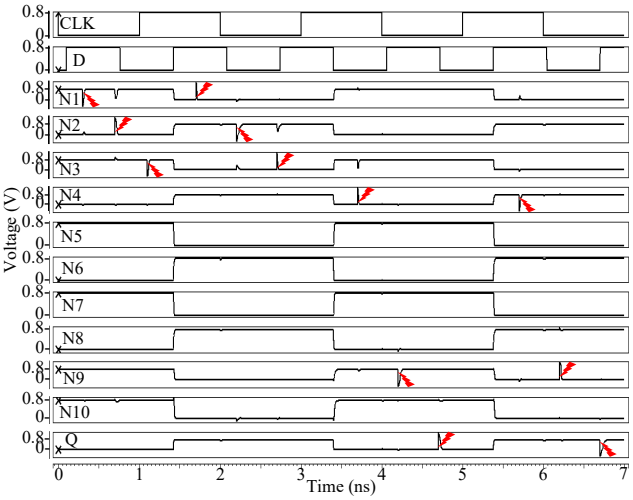

Fig. 12. Simulation results of SNU-injections for the LCDDETT latch.

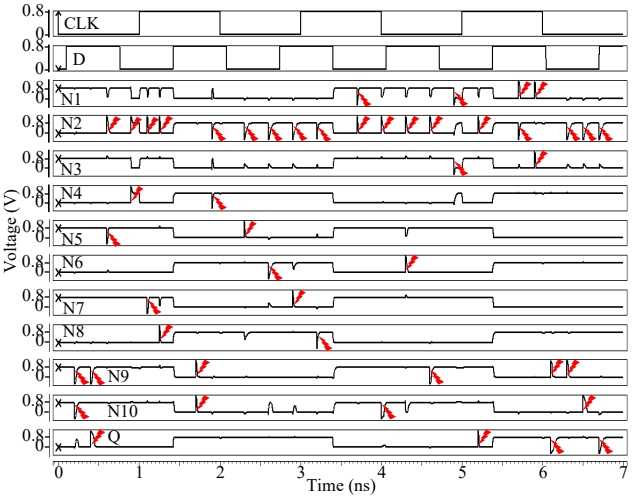

Fig. 13. Simulation results of DNU-injections for the LCDDETT latch.

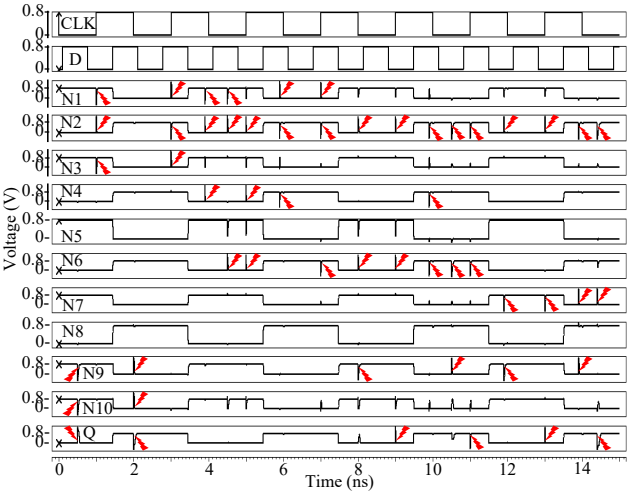

Fig. 14. Simulation results of TNU-injections for the LCDDETT latch.

LCDDETT latch considering all the above-mentioned key-TNUs on node-lists <N9, N10, Q>, <N1, N2, N3>, <N1, N2, N4>, <N2, N1, N6>, <N2, N4, N6>, <N2, N6, N9>, <N2, N6, Q>, <N2, N7, N9> and <N2, N7, Q>. When Q = 0, TNUs were injected on these node-lists at 0.50ns, 1.00ns, 3.90ns, 4.50ns, 5.00ns, 8.00ns, 9.00ns, 11.90ns, and 13.00ns, and when Q = 1, TNUs were injected on these node-lists at 2.00ns, 3.00ns, 5.90ns, 7.00ns, 9.90ns, 10.50ns, 11.00ns, 13.90ns, and 14.40ns, respectively. It can be seen from Fig. 14 that the LCDDETT latch can either self-recover from these TNUs or finally output a correct value on Q although some nodes are flipped. Therefore, the LCDDETT latch is TNU-tolerant. To summarize, the simulation results validate the SNU, DNU, and TNU tolerance of the proposed latches.

IV. Comparison

To make a fair comparison, the previously reviewed FERST [10], ISEHL [11], TMR [12], HRUT [13], DNUR [15], TNUTL [16], RHLD [17], LCTNUT [26], TNUHL [27], and TNURL [2] latches, including the unhardened latch (i.e., the traditional static D latch), were designed using the same parameters as the proposed (DDETT and LCDDETT) latches.

The node-upset tolerance comparison results for these alternative latch designs are shown in Table I. It can be seen from Table I that, the unhardened latch cannot provide SNU, DNU, or TNU tolerance, and hence it is not suitable for safety-critical applications. The FERST, ISEHL, TMR, and HRUT latches are SNU tolerant. However, they are not DNU or TNU tolerant, and hence they still cannot meet the very-high-reliability requirements for safety-critical applications. The DNUR latch can provide DNU tolerance. However, it is still not reliable with respect to TNUs. The TNUTL, RHLD, LCTNUT, TNUHL, TNURL latches, and the proposed DDETT and LCDDETT latches can provide complete TNU tolerance, and hence they and the proposed latches are of the same-type. However, the TNUTL latch cannot store values for a long time, because it does not have any feedback loop. For the other latches, they either have large overhead that will be discussed in the following or have high charge-sharing probability in the SM.

Table II shows the overhead comparison results for latch designs in terms of D to Q transmission delay, the average power dissipation (dynamic and static), silicon area, and DPAP (calculated by multiplying delay, power, and area), respectively. Note that the silicon area of these latch designs was measured using the method in [2]. It can be seen from Table II that, the D-Q delay of the RHLD latch is the largest. This is mainly due to the use of MLEI mechanism to provide TNU tolerance for the latch. Although the MLEI mechanism is not employed for the FERST, TMR, HRUT and TNUTL latches including the unhardened latch, since there are many devices from D to Q or there is a keeper at Q, their delay is still large. The delay of the ISEHL, DIRT and DNUR latches, including our proposed latches, is small, since a high-speed path from D to Q is used for them.

It can also be seen from Table II that, the power dissipation of the TNUHL latch is the largest and this is mainly due to the special structure of the latch (the RC modules can lead to large current competition). The power dissipation of the DIRT, DNUR and RHLD latches, including our proposed latches (DDETT and LCDDETT), is large mainly since their silicon area is large. However, compared with the DIRT, DNUR, and RHLD latches, the power dissipation of our proposed latches is lower.

It can be seen from Table II that the TNURL latch has the largest silicon area, since it employs the largest number of transistors (7 SIMs) to provide TNU tolerance. Compared with the TNURL latch, the silicon area of our proposed latches is smaller, since we employ fewer CEs to create the DLEI mechanism, which is sufficient to provide TNU tolerance. The other latches have comparable or smaller silicon area. However, most of them cannot provide complete TNU tolerance. This

TABLE I
Reliability Comparison Results For Latch Designs

Latch Type	Ref.	SNU Tolerant	DNU Tolerant	TNU Tolerant
Unhardened	-	×	×	×
FERST	[10]	√	×	×
ISEHL	[11]	√	×	×
TMR	[12]	√	×	×
HRUT	[13]	√	×	×
DNUR	[15]	√	√	×
TNUTL	[16]	√	√	√
RHLD	[17]	√	√	√
LCTNUT	[26]	√	√	√
TNUHL	[27]	√	√	√
TNURL	[2]	√	√	√
DDETT	Proposed	√	√	√
LCDDETT	Proposed	√	√	√

TABLE II
Overhead Comparison Results For Latch Designs

Latch Type	D-Q Delay (ps)	Power (μW)	10^{-4}× Area (nm^2)	10^{-6}× DPAP	CLK-Q Delay (ps)	Setup Time (ps)
Unhardened	11.80	0.11	0.66	0.009	11.79	7.10
FERST	41.39	0.20	1.85	0.153	41.31	14.79
ISEHL	2.90	0.12	1.58	0.005	2.93	17.40
TMR	46.42	0.70	3.70	1.202	46.45	6.79
HRUT	58.23	0.22	1.98	0.254	58.21	28.59
DNUR	3.01	0.44	4.36	0.058	3.06	26.91
TNUTL	21.95	0.19	2.38	0.099	21.60	3.48
RHLD	101.86	0.63	5.41	3.472	101.70	12.54
LCTNUT	1.67	0.25	3.17	0.013	1.69	11.82
TNUHL	1.66	0.94	2.38	0.037	1.69	23.13
TNURL	5.44	0.39	8.45	0.179	5.21	74.38
DDETT	1.67	0.31	4.22	0.022	1.68	13.38
LCDDETT	1.67	0.25	3.17	0.013	1.69	11.36

implies that high reliability of most latches is generally achieved at the cost of indispensable silicon area overhead.

It can be seen from Table II that the DPAP of the RHLD latch is the largest, and this is mainly due to its largest silicon area and delay. The DPAP of the TMR latch is still large and this is mainly due to its larger delay, power dissipation, and silicon area. The DPAP of the ISEHL latch is the smallest and this is mainly due to its small delay and silicon area.

Moreover, since latches become more sensitive to process, voltage and temperature (PVT) variation effects in deep nano-scale CMOS technologies [26, 28], PVT variation impacts on latches were also evaluated using the methods in our previous work [26]. Figure 15 shows the evaluation results of PVT variation impacts on delay and power of the SNU, DNU and/or TNU hardened latch designs that are listed in Table I/II. Note that the normal temperature was set to 25℃ and the temperature was varied from −25℃ to 125℃, the normal supply voltage was set to 0.8V and the supply voltage variation was varied from 0.65V to 0.95V, and the threshold-voltage increment was varied from 0.01V to 0.06V. Also note that the

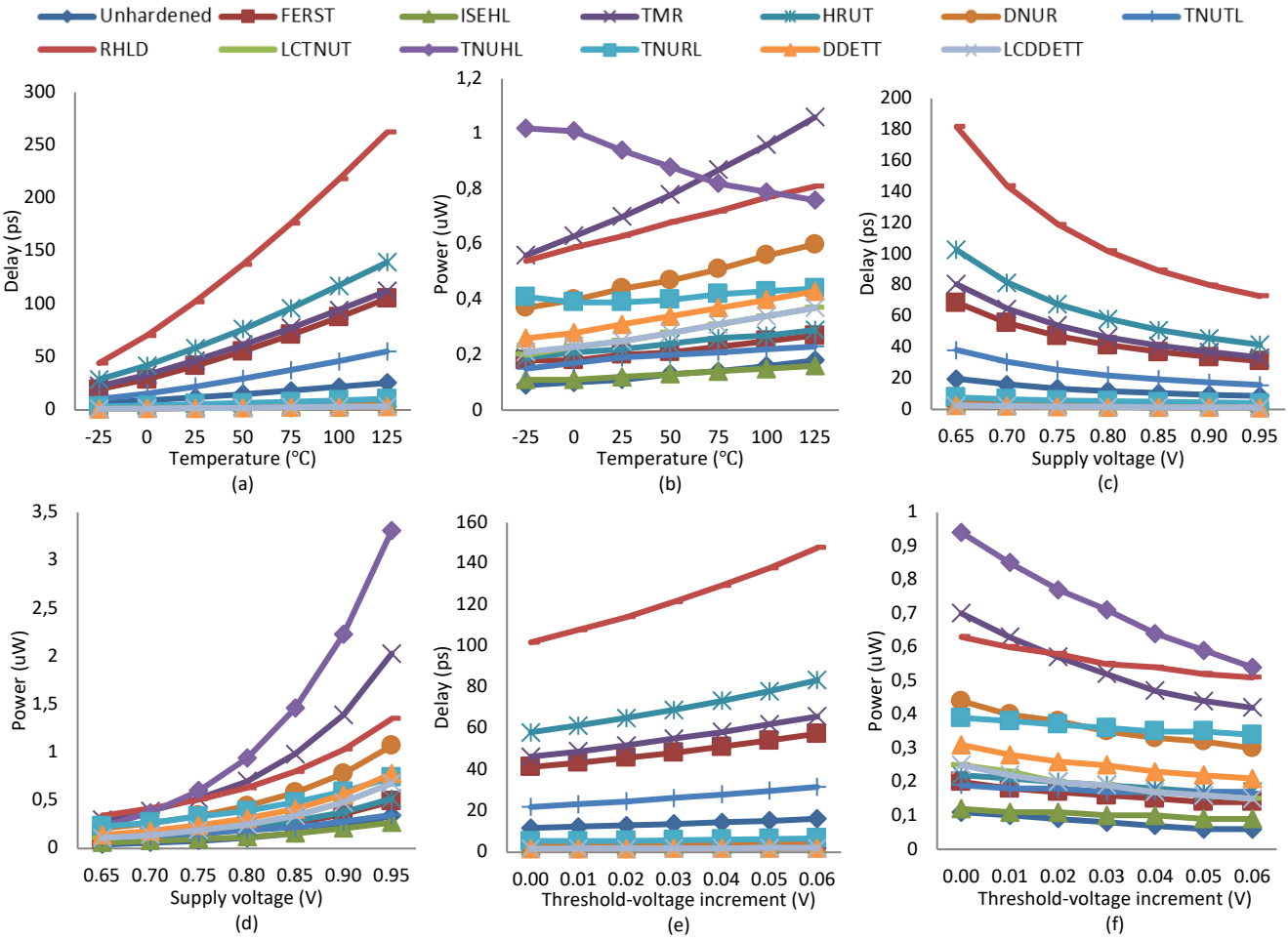

Fig. 15. Estimation results of PVT variation impacts on delay and power for the SNU, DNU and TNU hardened latch designs. (a) Impact of temperature variations on delay. (b) Impact of temperature variations on power. (c) Impact of supply-voltage variations on delay. (d) Impact of supply-voltage variations on power. (e) Impact of threshold-voltage variations on delay. (f) Impact of threshold-voltage variations on power.

TABLE III
NORMALIZED AVERAGE DEVIATION AND STANDARD DEVIATION FOR DELAY OF LATCHES

	Unhardened	FERST	ISEHL	TMR	HRUT	DNUR	TNUTL	RHLD	LCTNUT	TNUHL	TNURL	DDETT	LCDDETT
dev	1.00	2.17	1.05	1.12	1.47	0.94	1.04	1.25	0.70	0.87	1.06	0.94	1.01
σ	1.00	2.72	1.17	1.11	1.71	0.96	1.08	1.29	0.69	0.88	1.09	0.95	1.07

TABLE IV
NORMALIZED AVERAGE DEVIATION AND STANDARD DEVIATION FOR POWER OF LATCHES

	Unhardened	FERST	ISEHL	TMR	HRUT	DNUR	TNUTL	RHLD	LCTNUT	TNUHL	TNURL	DDETT	LCDDETT
dev	1.00	0.65	0.71	1.03	0.54	0.69	1.98	0.51	0.91	1.61	1.14	0.87	0.92
σ	1.00	0.76	0.74	1.02	0.61	0.76	2.73	0.58	0.93	1.60	1.27	0.92	0.97

D-Q delay is almost the same to the CLK-Q delay for latches, and thus in the following we use delay to represent D-Q delay only.

It can be seen from Fig. 15-(a) and (b) that the latches need to consume increasing delay and power in general when the temperature is rising, mainly since the carrier mobility will decrease when the temperature increases [29]. It can be seen from Fig. 15-(a) that the temperature variation has the largest impact on the delay of the RHLD latch, mainly due to its large silicon area that induces more decreased carrier mobility when the temperature is rising. However, the temperature variation has a low impact on the delay of the other latches such as the TNURL, and the proposed DDETT and LCDDETT latches. It can be seen from Fig. 15-(b) that the temperature variation has the largest impact on the power of the TMR latch since the power can highly increase when the temperature is rising and the TMR latch employs a redundant structure. However, the temperature variation has a low impact on the power of the other latches such as the ISEHL and the TNURL latches.

It can be seen from Fig. 15-(c) and (d) that the latches have decreasing delay and increasing power in general when the supply voltage is rising. Increasing supply voltage can reduce delays of transistors but can increase power dissipation [29]. It can be seen from Fig. 15-(c) that the supply voltage variation has the largest impact on the delay of the RHLD latch, mainly since it employs too many devices such as restore circuits (RCs) from its input to its output. However, the supply voltage variation has low impacts on the delay of the other latches such as the ISEHL, and the proposed DDETT and LCDDETT latches, since some of them uses a high-speed path from input to output and the other ones employs few devices from input to output. It can be seen from Fig. 15-(d) that the supply voltage variation has the largest impact on the power of the TNUHL latch since the power can highly increase when the supply voltage is rising. However, the supply voltage variation has a low impact on the power of the other latches such as the ISEHL and the TNUTL latches.

It can be seen from Fig. 15-(e) and (f) that the latches have increasing delay and decreasing power in general when the threshold voltage is rising. Increasing threshold voltage can increase delays of transistors but can decrease power dissipation [29]. It can be seen from Fig. 15-(e) that the threshold voltage variation has the largest impact on the delay of the RHLD latch, mainly since it employs too many devices such as RCs from its input to its output. However, the threshold voltage variation has a low impact on the delay of the other latches such as the TNUHL, and the proposed DDETT and LCDDETT latches, since some of them use a high-speed path from input to output and the other ones employs few devices from input to output. It can be seen from Fig. 15-(f) that the threshold voltage variation has the largest impact on the power of the TNUHL latch since the power can significantly decrease when the threshold voltage is rising. However, the threshold voltage variation has a low impact on the power of the other latches such as the ISEHL and the TNURL latches. In summary, the proposed latches have low or equivalent sensitivities to PVT variations compared with the state-of-the-art hardened latches.

To further investigate the PVT variation effects on latches, Monte Carlo simulations were also performed using the methodologies in [26]. To get parameters of average deviation (dev) and standard deviation (σ) for latches, 500 times' Monte Carlo simulations were performed. Table III/IV shows the normalized average deviation and standard deviation for delay and power of latches that are listed in Table I/II.

It can be seen from Table III that, compared with the unhardened latch, the DNUR, LCTNUT, TNUHL, and the proposed DDETT latches have lower sensitivity to the PVT variation effect for delay, since they all have a high-speed transmission path from D to Q. Other two conclusions can be drawn from Table III. First, the FERST latch has the largest sensitivity to the PVT variation effect for delay, mainly since the latch employs DMR and CE-based SLEI. Second, the proposed DDETT and LCDDETT latches have similar-and-lower sensitivity to the PVT variation effect for delay, compared with the TNURL latch. On the other hand, it can be seen from Table IV that, compared with the unhardened latch, the TMR, TNUTL, TNUHL and TNURL latches have larger sensitivity to the PVT variation effect for power, mainly since they have large area. Other two conclusions can be drawn from Table IV. First, the TNUTL latch has the largest sensitivity to the PVT variation effect for power, mainly since it employs a TEM and an inverter. Second, the proposed DDETT and LCDDETT latches have similar-and-lower sensitivity to the PVT variation effect for power, compared with the TNURL latch. In summary, the proposed latches have low and/or equivalent sensitivity on the PVT variation effects compared with the state-of-the-art hardened latches.

To make a quantitative comparison, we have calculated the ratios of overhead improvements (ROIs) of our proposed latches (DDETT and LCDDETT) compared with the other DNU and/or TNU tolerant latches. Eq. (1) shows the calculation formula of ROI for delay, and the average of ROI for delay can be obtained. Similarly, the calculation formulas for power dissipation, silicon area, and DPAP can be obtained. Obviously, the positive ROIs are better.

$$\mathrm{ROI}_{Delay} = \frac{Delay_{\mathrm{compared}} - Delay_{\mathrm{proposed}}}{Delay_{\mathrm{compared}}} \times 100\% \qquad (1)$$

It can be calculated that, compared with the DNU-tolerant DIRT latch, the ROI of DDETT is 79.74%, 37.78%, -77.31%, and 77.70% for delay, power, area, and DPAP, respectively. It means that we have to use extra 77.31% area to achieve TNU tolerance and small overhead in terms of delay, power and DPAP for the proposed DDETT latch. Similarly, compared with the DNU-tolerant DNUR latch, the DDETT latch respectively saves 45.74% delay, 28.21% power, 3.21% area and 62.50% DPAP. This shows that the proposed TNU-tolerant DDETT latch has smaller overhead. Moreover, compared with the TNU-tolerant TNUTL latch, it can be calculated that the DDETT latch saves 91.95% delay and 71.55% DPAP, while uses extra 100.00% power and 77.31% area. Similarly, compared with the TNU-tolerant RHLD latch, it can be calculated that the proposed DDETT latch saves 98.25% delay, 41.75% power, 22.00% area and 99.26% DPAP. On the other

hand, the proposed LCDDETT latch respectively saves 14.29% power, 24.88% area, and 36.36% DPAP compared with the proposed DDETT latch, which demonstrates the low-cost feature of the proposed LCDDETT latch.

V. Conclusions

Based on the RHBD approach, this paper has presented a novel dual-modular-redundancy and dual-level error-interception based TNU-tolerant (DDETT) latch. The latch can tolerate any possible TNU (as well as DNU and SNU) in a highly reliable and cost-effective manner. To even more reduce overhead, the low-cost version of the DDETT, namely LCDDETT, has further been proposed. The latch has the same soft error tolerance compared to the DDETT latch and can achieve very low overhead in terms of power dissipation, silicon area and DPAP. Simulation results have demonstrated the TNU-tolerance of the proposed latches as well as their cost-effectiveness, compared with state-of-the-art latch designs. The proposed latches are applicable to safety-critical applications where high-reliability and cost-effectiveness are both indispensable.

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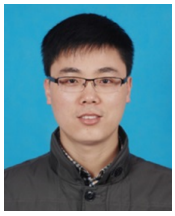

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