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Abstract—**With the reduction of technology nodes now reaching 2nm, circuits become increasingly susceptible to external perturbations. Thereby, soft errors, such as single-node-upset (SNU), single-event-transient (SET), double-node-upset (DNU), and even triple-node-upset (TNU), must be considered for safety-critical applications. This paper first presents four advanced circuit components (i.e., advanced voters), that have very small overhead compared with the traditional voters. The proposed Advanced Triple-Modular-Redundancy (ATMR) and Advanced Quadruple-Modular-Redundancy (AQMR) voters only consist of four and six inverters, respectively, to provide effective tolerance against SNUs and DNUs. To further filter SETs, a Schmitt-trigger (ST) instead of an inverter at the output-level is used to construct the ATMR-ST and AQMR-ST voters. These proposed voters can also be extended to tolerate TNUs. Next, these voters are used for latch hardening, so that this paper also presents a series of voter-based latch designs, to ensure high reliability with cost-effectiveness. Simulation results demonstrate the node-upset tolerance and/or SET-filterability of the proposed voters and voter-based latches, respectively. Simulation results also demonstrate that the proposed ATMR voter can reduce delay, power, and area by 55.2%, 32.8%, and 32.2%, respectively, compared with the traditional TMR voter; the proposed so-called HITTSFL latch can reduce delay, power, and area by 78.9%, 15.8%, and 28.6%, respectively, compared with the state-of-the-art TNU hardened latch (TNUHL).**

Index Terms—**voter design, voter based latch design, single-node upset, double-node upset, triple-node upset, single-event-transient**

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I. INTRODUCTION

With CMOS technology scaling, the advanced *integrated circuits* (*ICs*) and systems without design for radiation-hardening are becoming severely vulnerable to soft errors. Soft errors in ICs are dominantly caused by the strike of particles, such as α particles, heavy ions, neutrons and electrons [1-3]. *Single-node upset* (*SNU*), *single-event-transient* (*SET*), *double-node upset* (*DNU*), and *triple-node upset* (*TNU*), are typical soft errors. In an advanced nano-scale CMOS storage cell, the strike of a high-energy particle can invalidly change the logic value of a single node, and thus results in an SNU; in a combinational circuit module, the striking-particle can introduce a transient erroneous pulse at the output of a logic gate, and thus results in an SET. The SET can propagate to a downstream storage cell and can be captured by the cell if the SET cannot be masked, and thus results in erroneous-value retention [4]. Moreover, in highly-integrated nano-scale ICs, due to double-node charge collection [5], a radiative particle can simultaneously change the logic values of two nodes in a storage cell, and thus results in a DNU. The scenario that three nodes are simultaneously impacted is called a TNU [6-9]. Clearly, design for reliability against SNUs and/or SETs only are no longer sufficient for safety-critical applications. Therefore, it is crucial to design not only SNU/DNU/TNU-tolerant but also SET-filterable circuit components, such as voters and voter-based latches, to construct highly reliable circuits and systems for safety-critical applications. Note that, only a part of latches, e.g., the *Triple Module Redundancy Latch* (*TMRL*), is voter-based, for reliability design against soft errors.

To tolerate SNUs, DNUs, and/or TNUs, the traditional solutions, such as *triple-modular-redundancy* (*TMR*) and *quintuple-modular-redundancy* (*QMR*), are widely used. Among these solutions, voters have to be used. However, these employed voters have large overhead in terms of area, power and delay and this motivates us to propose novel cost-effective and highly reliable voters design for safety-critical applications. Note that based on a traditional voter, a traditional TMR latch and a traditional QMR latch can be constructed to tolerate SNUs and DNUs, respectively. However, the overhead of these latches would be significantly large, not only due to the large overhead of the employed voter, but also due to redundant copies of modules that need to be voted. Therefore, we propose cost-effective advanced voters and cost-effective advanced voter-based latches. For latch hardening against soft errors, the *radiation-hardening-by-design* (*RHBD*) approach is widely used. Based on RHBD, researchers

have proposed many circuit components such as *static random access memories* (*SRAMs*) [10-13], flip-flops [14-17], and latches [6-9, 18-28]. Note that this paper proposes two contributions, i.e., voter designs and latch hardening. Among these latches, temporal redundancies, such as introducing delay elements and/or SET-filterable components, are used, to filter SETs [20-21]; spatial redundancies, such as introducing extra storage nodes and extra-level error-interception, are used, to tolerate SNUs [18-19, 21, 25, 26] and even to tolerate DNUs and/or TNUs [6-9, 22-24, 26, 28]. After deep investigation, we found that existing solutions suffer from some severe problems such as the following.

1) Traditional voters have large overhead and they cannot filter SET pulses.
2) Existing latches can only provide a part of TNU tolerance [18-27] (this is because, for any of them, there is at least one combination of three nodes that retain invalid values if the latch is impacted by a TNU); some of them cannot filter SET pulses [6-9, 18-19, 22, 24-28] (This is because, for any of them, an SET pulse can unfortunately propagate from the input to the output); to the best of our knowledge, none of them can provide TNU-tolerance and SET-filterability simultaneously, except our proposed HITTSFL latch that is published in the conference version paper [30]. Note that some existing latches are sensitive to *high-impedance state* (*HIS*) because they use *C-elements* (*CEs*) to output values [6-7, 9, 18, 29]. Moreover, some latches consume large overhead since they have to use extra redundant devices.

Note that our solution proposed in [29] cannot filter SETs and is sensitive to the HIS. This paper first proposes a series of advanced voters that have very small overhead compared with the traditional voters. The values stored in the modules to be voted can converge at a common output node of three inverters, so that the proposed voters can still output correct values owing to current competition and signal strength by the output-level inverter/ST. Second, based on the proposed voters, this paper proposes a series of latches that can tolerate SNUs, SETs, and/or DNUs. To tolerate TNUs, more modules to be voted need to be used leading to large overhead, and thus this paper finally proposes a low-cost, *HIS-Insensitive, TNU-Tolerant and SET-Filterable Latch* (*HITTSFL*). The latch mainly consists of three SNU-recoverable *Dual-Interlocked-storage-Cells* (*DICEs*) to retain values and three inverters (to bring the retained values to the input of an output-level ST to tolerate any TNU and filter any SET). The proposed solutions are insensitive to the HIS since we do not use C-elements to output values, making them more robust for safety-critical applications. Simulation results demonstrate the SNU/DNU/TNU-tolerance and/or SET-filterability as well as cost effectiveness of the proposed solutions, respectively.

The main contribution of the paper is summarized as follows. A series of representative advanced voters and these voters based-latches are proposed to provide SNU/DNU tolerance and/or SET filterability with low cost. These voters and latches are insensitive to the HIS and can be extended to tolerate TNUs. Based on the proposed advanced TMR voter, a first-ever cost-effective, HIS-Insensitive, TNU-Tolerant and SET-Filterable latch is proposed. Extensive simulations and evaluations for all alternative solutions are provided.

The rest of the paper is organized as follows. Section II introduces widely used components and these components-based typical latches. Section III provides the schematics and working principles of the proposed voters and these-voters-based latches. Section IV presents verification results of the proposed solutions. Section V presents comparison and evaluation results. Section VI concludes the paper.

II. PRELIMINARIES

This section introduces widely used components for circuit hardening against SNUs/DNUs/TNUs/SETs for safety-critical applications. This section also introduces these components-based hardened latches.

A. Components

Many circuits hardened against SNUs, DNUs, TNUs, and/or SETs have been proposed in recent years. In these circuits, some components, such as CEs, STs, and DICEs, are widely used. Figure 1 shows schematics and symbols of them. Figure 1-(a) and (b) show the 2-input and 3-input CEs and thus the 4-input CE can be easily created. A CE behaves as an inverter if its inputs have the same value; however, if its inputs become different, its output will temporally retain the previous value due to capacitance. Moreover, if its inputs keep different values for an extended period of time, its output will enter into the HIS, floating to an unknown value. Note that CEs can be controlled by the *system clock* (*CLK*) and *negative system clock* (*NCK*) signals. Figure 1-(c) and (d) show the *clock-gating* (*CG*) based CEs. Figure 1-(e), (f), and (g) show the ST, the DICE, and the CG-based DICE. Details about STs and DICEs will be introduced in the next section. Figure 1-(h) shows the TMR voter that consists of three 2-input AND gates and one 3-input OR gate, totally leading to 18 transistors. This motivates us to propose advanced low-cost voters.

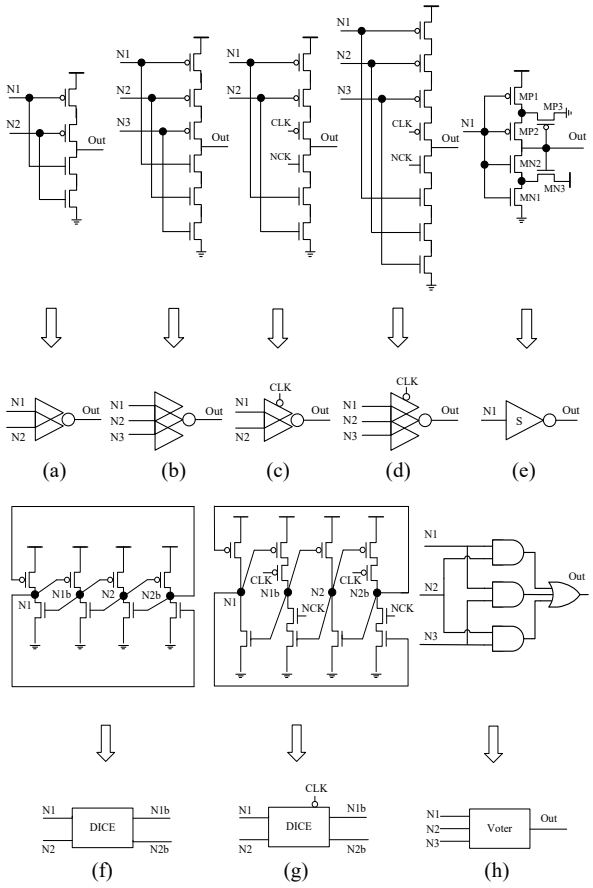

Fig. 1. Schematics and symbols of the widely used components in typical hardened circuits. (a) 2-input C-element. (b) 3-input C-element. (c) Clock-gating based 2-input C-element. (d) Clock-gating based 3-input C-element. (e) Schmitt-trigger. (f) Dual-interlocked-storage-cell. (g) Clock-gating based Dual-interlocked-storage-cell. (h) Triple Module Redundancy voter.

B. Existing Latches

This section reviews the above-mentioned-components based existing latches, such as the *TMRL*, *Low-Power Soft Error Hardened Latch* (*DET-SEHPL*) [20], *Low cost and Soft Error Hardened Latch* (*LSEH*) [21], *Double-node-resilient Latch* (*DNURL*) [22], *Temporally Double Node Upsets Hardened Latch Circuits* (*THLTCH*) [23], *Triple Node Upset Resilience DICE Latch* (*TNUDICE*) [7], and *Triple Node Upset Hardened Latch* (*TNUHL*) [6]. Figure 2 shows schematics of them. In Fig. 2, the switches marked with CLK/NCK are *transmission gates* (*TGs*).

Figure 2-(a) shows the TMRL latch. It employs triple unhardened latches with a voter to tolerate SNUs only. However, the voter consists of many transistors as introduced in the above section, leading to extra overhead. Figure 2-(b) shows the DET-SEHPL latch [20]. It uses an ST as well as a CE with input-delay-differential to filter SETs. It also uses the CE to tolerate SNUs. However, it cannot tolerate an SNU at Q since Q feeds inputs of the CE.

Figure 2-(c) shows the LSEH latch [21]. It uses a CE with input-delay-differential to filter SETs and uses double feedback loops feeding the CE to tolerate SNUs. Note that the output of the CE connects a keeper so as to avoid the sensitivity to an HIS. However, it is obvious that the latch cannot tolerate DNUs.

Figure 2-(d) shows the DNURL latch [22]. It uses triple *Self-Recoverable, Frequency-aware and Cost-effectives* (*RFCs*) [19] to provide DNU- recoverability. However, it cannot tolerate TNUs because there is a counterexample that the common-nodes among RFCs can be flipped by a TNU; moreover, it cannot filter SETs. Figure 2-(e) shows the THLTCH latch [23]. It

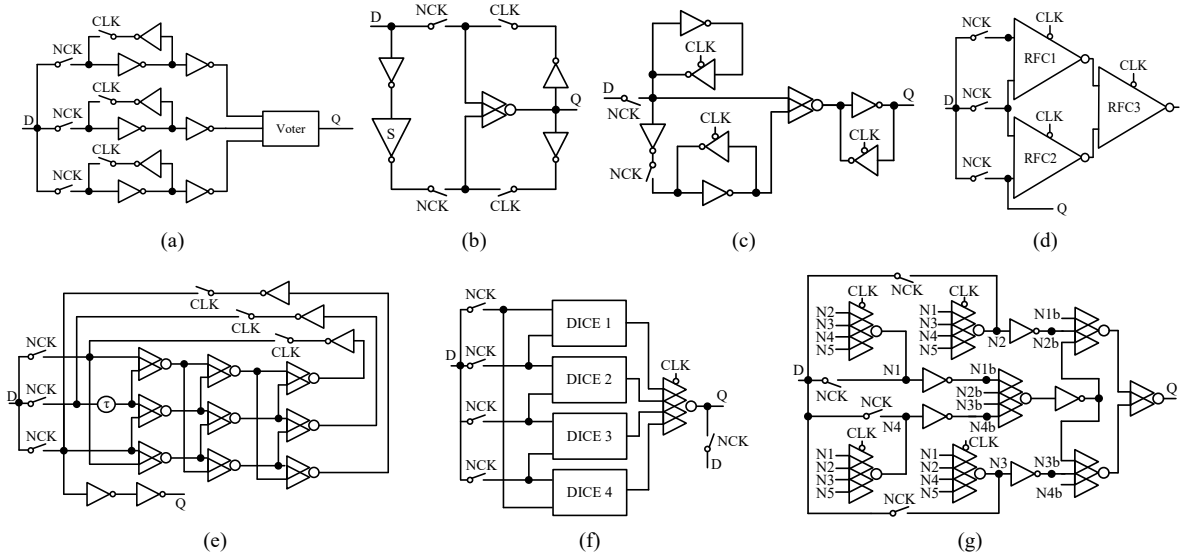

Fig. 2. Schematics of previous hardened latches. (a) TMRL. (b) DET-SEHPL [20]. (c) LSEH [21]. (d) DNURL [22]. (e) THLTCH [23]. (f) TNUDICE [7]. (g) TNUHL [6].

uses a delay element marked with τ to create delay-differential of inputs of some CEs to filter SETs. It uses nine interlocked CEs to tolerate SNUs and DNUs. However, it cannot tolerate TNUs, especially for the CEs in series-connection.

Figure 2-(f) shows the TNUDICE latch [7]. It uses many interlocked DICEs feeding an output-level CE to tolerate TNUs. However, it is sensitive to the HIS because a DICE suffering from a TNU can make inputs of the CE different; moreover, it cannot filter SETs. Figure 2-(g) shows the TNUHL latch [6]. It cannot filter SETs and is sensitive to the HIS (similarly to the TNUDICE latch); moreover, it consumes large overhead mainly because it uses many redundant transistors.

In this section, the widely used components, such as CEs, ST, and DICEs, for circuit hardening against SNUs/DNUs/TNUs/SETs, are introduced. These components-based hardened-latches are also introduced.

III. PROPOSED SOLUTIONS

As mentioned above, traditional voters, e.g., the traditional TMR voter shown in Fig. 1-(h), have large overhead and cannot filter SET pulse. So, in this paper we proposed advanced voters. This section introduces the proposed advanced voters and the corresponding voter-based latch designs.

A. Proposed voters

Figure 3 shows the proposed advanced voters, namely ATMR and ATMR-ST, based on current competition on a convergence node (i.e., Qb) and signal strength by an output-level inverter/ST. Layouts of these voters are also shown in the figure. It can be seen from Fig. 3-(a) that the ATMR voter only consists of four inverters, and thus has low overhead. The value of Qb can be determined by N1, N2, and N3 through three inverters and the value of Q can be determined by Qb through the output-level inverter. The proposed ATMR voter can output the correct value in case one input has an erroneous value. We take the case that N1 = N2 = N3 = 0 for an example. If "Module 3" is impacted by an SNU, N3 can be flipped to "1". Hence, Qb will receive two correct values from N1 and N2, and receive one incorrect value from N3. In other words, Qb will have more correct current to compete with the incorrect current. In this case, as time is flowing, the value of Qb will be jointly determined through three inverters and Qb will be close to the correct value "1" due to current competition. Hence, the output of the proposed ATMR voter can still be correct owing to the signal strength provided by the output-level inverter.

To filter SETs, we replace the inverter at the output level by an ST and propose the ATMR-ST voter. It can be seen from Fig. 3-(b) that the ATMR-ST voter only consists of three inverters and one ST. Note that, the ATMR-ST voter has the same fault-tolerance ability as the ATMR voter, but can additionally filter SETs. The SET-filtering principle of the ATMR-ST voter is as follows. If an SET arrives at nodes N1, N2, and/or N3, the SET will be reversed by inverters before Qb, converging at Qb. Therefore, the SET at Qb can be filtered by the ST. Here, a positive SET (low-high-low) at Qb is illustrated as an example for the SET-filtering principle. Since the previous correct value of Qb is low, i.e., the value of N1 in Fig. 1-(e) is low, transistors MP1 and MP2 are ON. Thus, the value of Out is high and MN3 is ON. As a result, when N1 changes from low to high (pulse rise stage) due to the SET, the value of Out will not change until the drain of MN1 is discharged from high to low. This needs a period of time especially when the aspect ratios of MN1 and MN3 are large. Within that period of time, D can change from high to low (pulse fall stage) due to the SET. Therefore, the value of Out will not change. In other words, this positive SET cannot pass through the ST. For a negative SET, we can get the similar scenario. To summarize, the proposed ATMR-ST voter can filter SETs. Note that we do not filter SETs in the modules to be voted and the inverters before node Qb due to large overhead of this method. Figure 3-(c)/(d) shows the layout of the ATMR/ATMR-ST voter. The layout width is 1.022 μm and the layout height is 1.290 μm for the ATMR voter. The layout width is 1.542 μm and the layout height is 1.290 μm for the ATMR-ST voter.

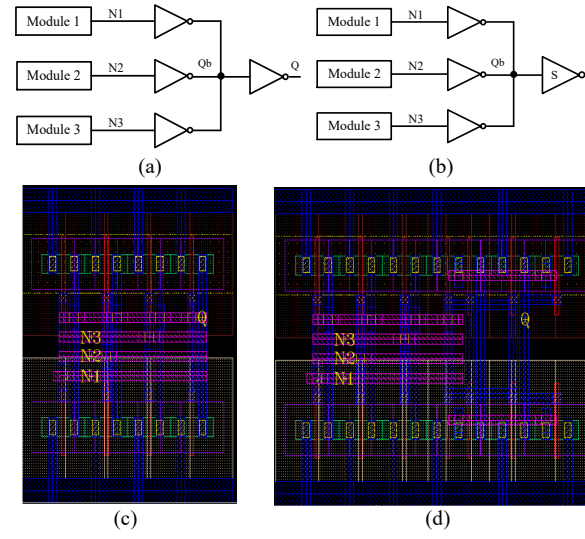

Fig. 3. Proposed advanced voter designs. (a) ATMR voter. (b) ATMR-ST voter. (c) Layout of the ATMR voter. (d) Layout of the ATMR-ST voter.

Figure 4 shows the traditional and the proposed QMR voters. It can be seen from Fig. 4-(a) that the traditional QMR voter is constructed from ten 3-input AND gates and one 10-input OR gate. Obviously, the

traditional QMR voter can output the correct value in case no more than two inputs have erroneous values. However, the traditional QMR voter has high overhead. To reduce overhead, we propose an Advanced QMR voter, namely AQMR, based on the same mechanism as the ATMR voter. It can be seen from Fig. 4-(b) that the AQMR voter only has six inverters and thus has low overhead. The value of Qb can be determined by N1, N2, N3, N4, and N5 through five inverters and the value of Q can be determined by Qb through the output-level inverter. The proposed AQMR voter can output the correct value in case no more than two inputs have erroneous value. This means that, in this case, as time is flowing, the value of Qb will still be jointly determined through five inverters and Qb will still be close to the correct value due to current competition. Hence, the output of the proposed AQMR voter can be correct owing to signal strength provided by the output-level inverter. Compared with the traditional QMR voter, the proposed AQMR voter has extremely small overhead. To filter SETs, we replace the inverter at the output level by an ST and propose the AQMR-ST voter. It can be seen from Fig. 4-(c) that the AQMR-ST voter only consists of five inverters and one ST. Due to the same SET-filtering principle as for the ATMR-ST voter discussed above, the proposed AQMR-ST voter can also filter SETs. Figure 4-(d)/(e) shows the layout of the AQMR/AQMR-ST voter. The layout width is 1.438 μm and the layout height is 1.450 μm for the AQMR voter. The layout width is 1.958 μm and the layout height is 1.450 μm for the AQMR-ST voter.

B. Proposed latches

Based on the voters proposed in the previous subsection, we replace the modules to be voted in voters by the traditional unhardened latches to propose four advanced latches and hence tolerate SNUs/DNUs and/or filter SETs. Figure 5 shows the schematics of the proposed latches, namely *ATMR based latch* (*ATMRL*), *ATMR and ST based latch* (*ATMRL-ST*), *AQMR based latch* (*AQMRL*), and *AQMR and ST based latch* (*AQMRL-ST*). According to the fault-tolerance discussion of the proposed voters, the proposed ATMRL and ATMRL-ST latches in Fig. 5-(a) and Fig. 5-(b) can output the correct value in case no more than one input has an erroneous value; the proposed AQMRL and AQMRL-ST latches in Fig. 5-(c) and Fig. 5-(d) can output the correct value in case no more than two inputs have erroneous values. In summary, ATMRL can tolerate SNUs, ATMRL-ST can filter SETs, AQMRL can tolerate DNUs, and AQMRL-ST can filter SETs. Note that layout of these proposed latches are omitted due to page limitation.

Note that each traditional unhardened latch has an inverter at its output-level as shown in Fig. 5-(a). To reduce overhead, we can reuse the inverter as an inverter of a voter. This means that the inverters of the voter before node Qb can be removed. However, one inverter has to be inserted at output node Q to ensure correct output logic of the proposed latches. Moreover, to further reduce overhead, we can only remove the inverters of a voter before node Qb. However, the nodes, such as A, B, and C in Fig. 5-(a), have to be used as inputs of the voter.

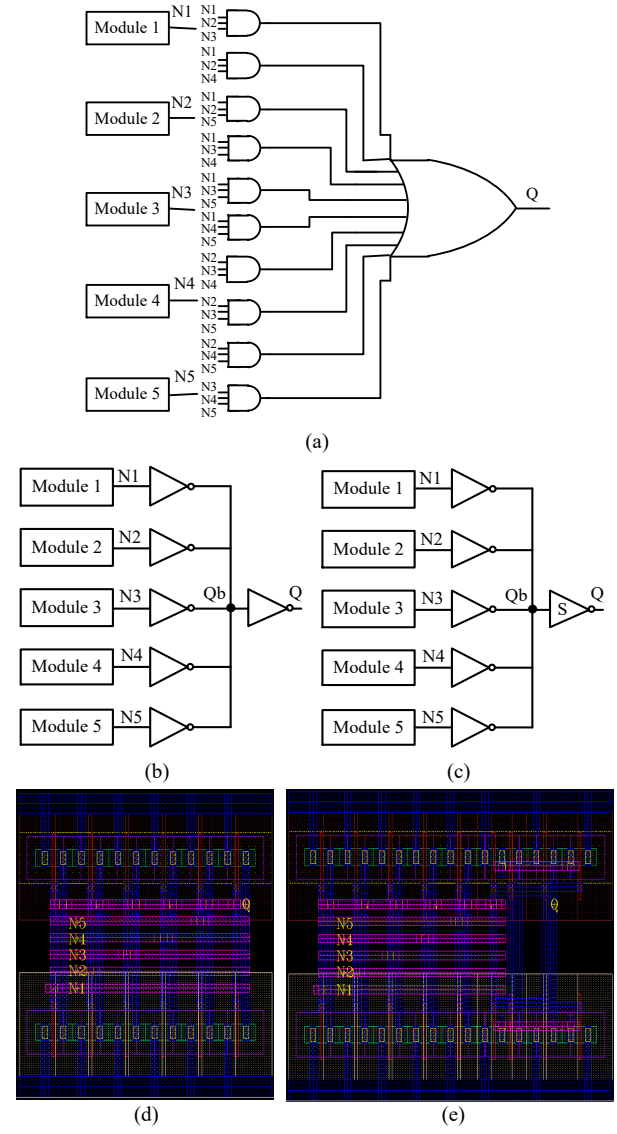

Fig. 4. QMR voter designs. (a) Traditional QMR voter. (b) Proposed AQMR voter. (c) Proposed AQMR-ST voter. (d) Layout of the AQMR voter. (e) Layout of the AQMR-ST voter.

It should be noted that providing an accurate and realistic calculation of the occurrence probability of a TNU is quite complex since many factors such as (1) technology data; (2) layout (to know effective area that can be affected by particles, spacing among adjacent nodes, etc.); (3) working conditions (hold mode duration, sup-

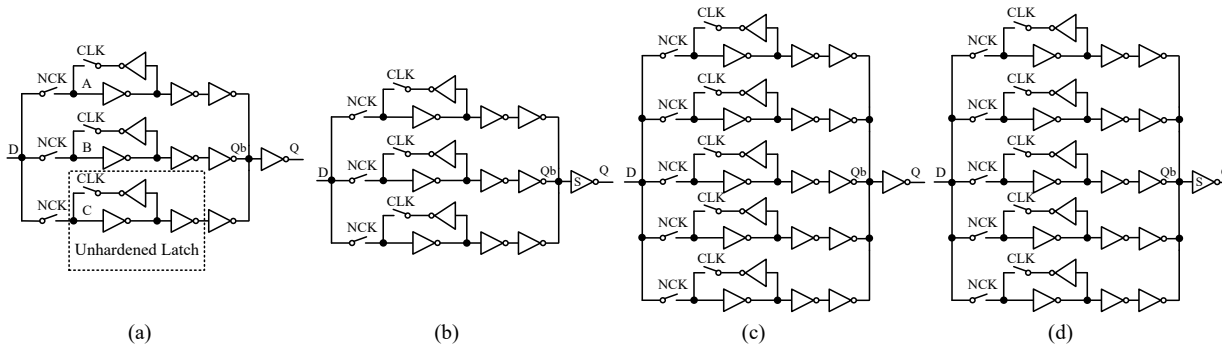

Fig. 5. Proposed latch designs. (a) ATMRL. (b) ATMRL-ST. (c) AQMRL. (d) AQMRL-ST.

ply voltage, working temperature, etc.); (4) particle types (neutron, proton, α-particle, heavy ion, etc.); (5) particle properties (flux distribution, effective hit rate, linear energy transfer, hit angle, etc.); (6) particle correlations, etc., should be known. Moreover, in safety-critical applications, to significantly save power dissipation, a latch can be switched into standby mode or its clock frequency can be aggressively reduced. In these cases, the hold mode duration of the latch can be long. During this time period, a series of particles can strike the latch if in harsh radiation environments, and hence provoke TNU errors.

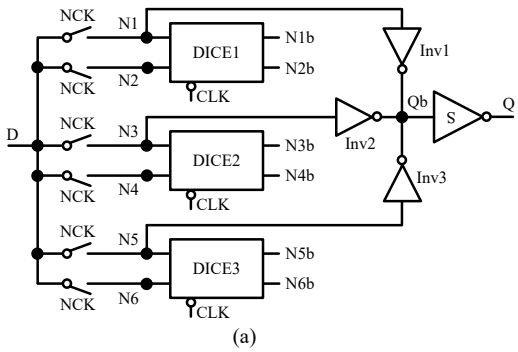

Fig. 6. Proposed so-called HITTSFL latch.

To simultaneously provide TNU-tolerance and SET filterability, the HITTSFL latch is proposed as shown in Fig. 6. The latch comprises six TGs to initialize values, three DICEs to retain values, three inverters to make values stored in DICEs converge at a common node (Qb), and an ST marked with 'S' to output the retained values. Figure 7 shows the layout of the HITTSFL latch. The layout width is 6.936 μm and the layout height is 2.090 μm. The error-free working principle of the latch is introduced in the following.

When CLK = 1 and NCK = 0, the latch works in transparent mode of operation. At this time, the TGs are ON, so that N1 through N6 can receive a value from D. Then, the value of Qb can be simultaneously determined by N1, N3, and N5 through inverters Inv1, Inv2, and Inv3. Thus, the ST can reversely output the value at Qb. Note that CG technologies are employed in DICEs to avoid the formation of feedback loops so as to reduce power dissipation in this mode. Therefore, the proposed latch can be correctly initialized and can output the value received from D. Note that the proposed latch can also filter SETs due to the use of an ST at the output level of the latch.

When CLK = 0 and NCK = 1, the latch works in hold mode of operation. At this time, the TGs are OFF, and the CG-based transistors in DICEs are ON, so that the feedback loops can be formed in DICEs to retain values. Then, the stored values in DICEs can propagate to Qb through inverters, and then to Q through the ST. In summary, the proposed latch can retain values and can output the retained values through Q.

The TNU-tolerance working-principle of the latch is introduced here. Due to the symmetric structure of

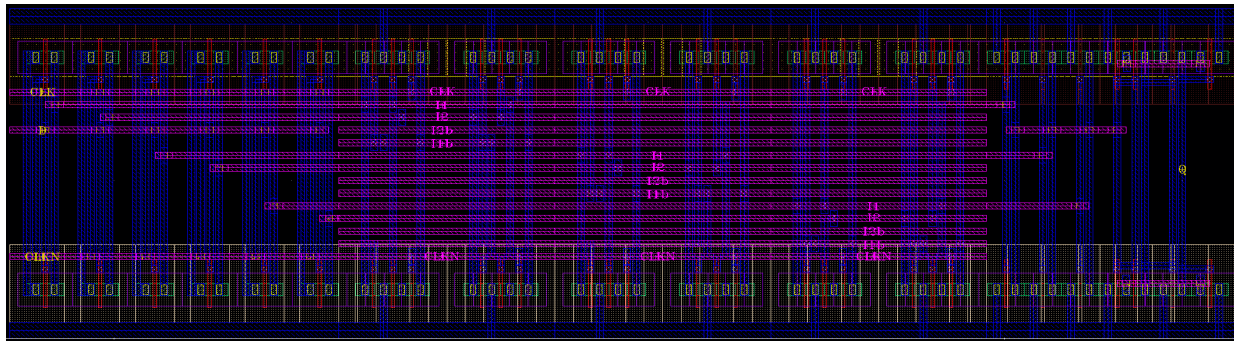

Fig. 7. Layout of the HITTSFL

the latch, there are only six cases need to be considered. **Case 1**: Qb or Q along with double nodes in a DICE are impacted by a TNU, and the key triple-nodes are <N1, N2, Qb>, <N1, N2, Q>, <N1, N1b, Qb> and <N1, N1b, Q> only; **Case 2**: Three nodes in a DICE are impacted by a TNU and the key triple-node is <N1, N1b, N2> only; **Case 3**: One node in a DICE and two nodes in another DICE are impacted by a TNU and the key triple-nodes are <N1, N1b, N3> and <N1, N2, N3> only; **Case 4**: One node in each DICE is impacted by a TNU and the indicative key triple-node is <N1, N3, N5> only; **Case 5**: Qb and Q along with one node in a DICE are impacted by a TNU and the indicative key triple-node is <N1, Qb, Q> only; and **Case 6**: Qb or Q along with single nodes in two DICEs are impacted by a TNU and the indicative key triple-nodes are <N1, N3, Qb> and <N1, N3, Q> only.

For Case 1, DICE1 can be considered for illustration. Note that <N1, N2> and <N1, N1b> cannot recover from DNUs when N1 is low [28]. Hence, the values stored in DICE1 will be flipped and a flipped value will feed Qb through Inv1. Fortunately, the values stored in DICE2 and DICE3 are not impacted and they will feed Qb through Inv2 and Inv3. Clearly, at the point when Qb is also impacted by the TNU, four values are converging at Qb, i.e., the first is the flipped value coming through Inv1, the second and the third are the correct values coming through Inv2 and Inv3, and the fourth is the invalid value induced by the direct particle-striking of the TNU. Fortunately, the fourth invalid value cannot be retained for an extended period of time. Therefore, as time passes, the value of Qb can be only determined through Inv1, Inv2 and Inv3, and thus Qb will be close to the correct value due to current competition. Consequently, the value of Qb will be reversed and strengthened to be a correct value by the ST, i.e., the latch can still output a correct value. Note that Qb cannot be impacted and Qb can remove the error at Q if Q is impacted by a TNU in Case 1. Note that <N1, N1b> can recover from a DNU when N1 is high [28]. At this time, if <N1, N1b, Qb> or <N1, N1b, Q> is impacted by a TNU, the values stored in DICE1 are still correct. Hence, the error at Qb or Q can be removed by DICEs through inverters, i.e., the latch can still output a correct value. Therefore, the latch can tolerate all key TNUs of Case 1.

For Case 2, DICE1 can still be considered for illustration. When the nodes suffer from a TNU, the flipped values in DICE1 will feed Qb through Inv1. Fortunately, the correct values stored in DICE2 and DICE3 will feed Qb through Inv2 and Inv3, respectively. Consequently, the value of Qb will be close to the correct value due to current competition and will be reversed and strengthened to be a correct value by the ST, i.e., the latch can still output a correct value. Therefore, the latch can tolerate TNUs for Case 2. For Case 3, the single-node-impacted DICE can self-recover [28], and thus the TNU downgrades to a DNU, so that this case is similar to Case 1. Therefore, the latch can tolerate TNUs for Case 3. For Cases 4 to 6, the single-node-impacted DICE can self-recover [28], so that the values stored in DICEs are still correct. Thus, the errors at Qb and/or Q can be removed by DICEs through inverters, i.e., the latch can tolerate all key TNUs of Cases 4 to 6. In summary, the above extensive discussions validate the complete TNU tolerance of the latch.

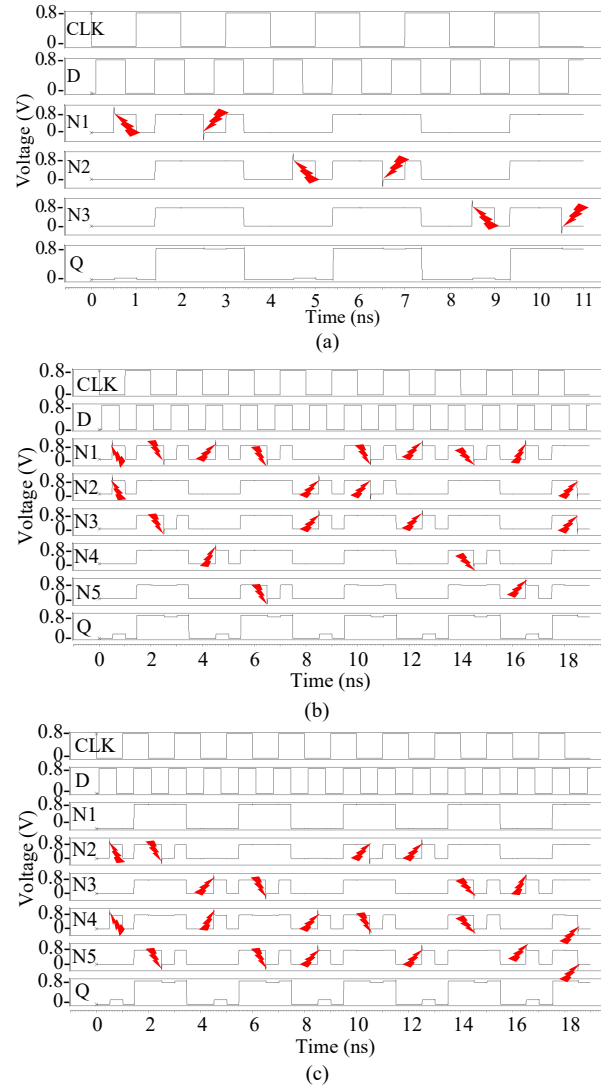

Fig. 8. Error-injection simulation results of the proposed voters. (a) ATMR voter. (b) Case D1 for AQMR voter. (c) Case D2 for AQMR voter.

IV. VERIFICATION RESULTS

The proposed voters and latches were implemented in the 22 nm CMOS technology from GlobalFoundries.

0.8V supply voltage and 25℃ working temperature were used for HSPICE simulations. The PMOS transistors' ratio was optimized to W/L = 90nm/22nm and the NMOS transistors' ratio was optimized to W/L = 45nm/22nm, respectively. In particle strike simulations, a double-exponential current source model was used [31] to simulate injected neutrons with large enough energy (the worst-case injected charge energy was up to 25fC). Note that the current source model is not available with HSPICE so that our own technical code was used. The time constants of the rise and fall periods of injected errors were set to 0.1 ps and 3.0 ps, respectively. Note that we choose the small rise time-period of injected errors so that the injected erroneous charge can have an immediate impact. The fall time-period is 30 times larger than the rise time-period so that 3.0 ps is sufficient enough for error injections.

Error-injection simulation results of the proposed ATMR and AQMR voters are shown in Fig. 8. The lighting marks in Fig. 8 denote the injected SNUs and DNUs. Note that we use two simultaneously injected SNUs to simulate a DNU. In Fig. 8-(a), an SNU was injected to N1, N2, and N3, respectively, irrespective of the value (0 or 1) of Q. It can be seen that Q was still correct. Similarly, it can be seen from Fig. 8-(b) and (c) that the AQMR voter can tolerate the injected DNUs (all possible DNUs were considered). This is because Q was still correct. In summary, the proposed ATMR voter is SNU-tolerant and the proposed AQMR voter is DNU-tolerant. Note that the SET-filtering ability of the ATMR-ST voter will be verified in the following (using the proposed HITTSFL latch).

Error-injection simulation results of the proposed HITTSFL latch are shown in Fig. 9. In Fig. 9-(a), a TNU was injected to <N1, N1b, Qb> and <N1, N1b, Q>, respectively. It can be seen that, no matter Qb was directly impacted or not, Qb was still or close to its correct value. Hence, Q was still correct. Similarly, it can be seen from Fig. 9-(b) and (c) that the latch can tolerate the injected key TNUs. In summary, the proposed latch can provide complete TNU-tolerance.

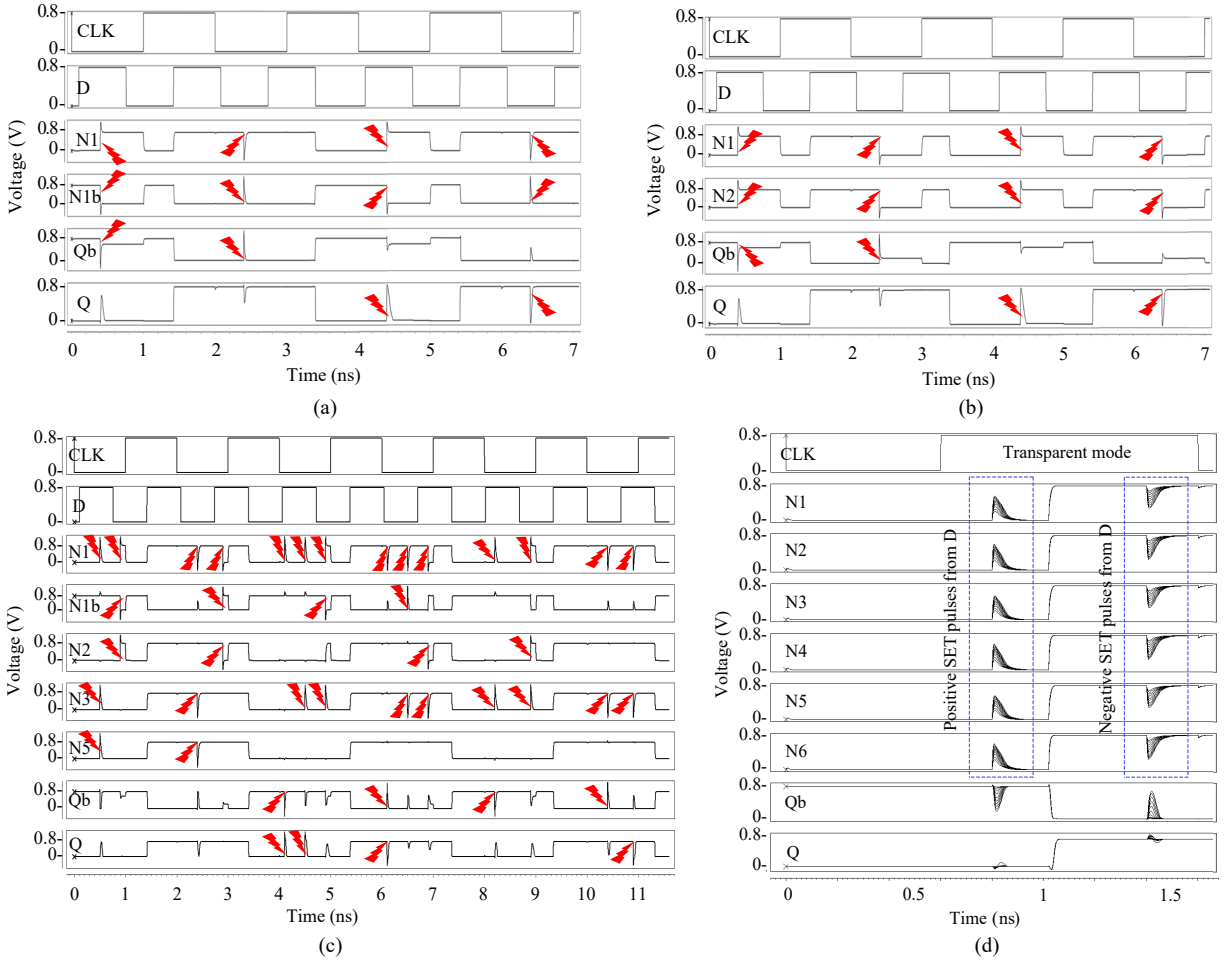

Fig. 9. Error-injection simulation results of the proposed HITTSFL latch. (a) Key TNU injections for <N1,N1b,Qb> and <N1,N1b,Q> of Case 1. (b) Key TNU injections for <N1,N2,Qb> and <N1,N2,Q> of Case 1. (c) Other key TNU injections. (d) SET injections.

Fig. 9-(d) shows SET-injection (to the latch-input) simulation results. The injected SETs passed through TGs arriving at N1 through N6. Then, the SETs were reversed through inverters and converged at Qb. It can be seen from Fig. 9-(d) that the SETs at Qb were effectively filtered by the ST (having almost no impact on Q). In summary, the proposed HITTSFL latch can provide SET-filterability. Clearly, simulation results demonstrated the TNU-tolerance and SET-filterability of the proposed HITTSFL latch.

V. COMPARISON RESULTS

To make a fair comparison, the reviewed voter and latch designs in Section II as well as the traditional unhardened latch were also implemented using the same conditions mentioned in the above section.

Table I shows the fault-tolerance capability and overhead comparison results among the traditional TMR and the proposed ATMR and ATMR-ST voters. Note that the Delay, Power and Area are the average of rise and fall delays from the voter input to Q), average power dissipation (dynamic and static), silicon area (measured with the same method as in [8]), respectively, and this is true for all solutions in this paper. It can be seen that the proposed ATMR-ST voter can additionally provide SET filtering capability. It can be also seen that the proposed ATMR voter has the smallest delay, area, and power, since it uses the least amount of transistors. Conversely, the traditional TMR voter has the largest delay, area, and power mainly since it uses the largest amount of transistors. Due to the use of ST, the overhead of the proposed ATMR-ST voter is higher than the ATMR voter. However, the ATMR-ST voter is still cost-effective compared to the traditional TMR voter that needs the largest amount of transistors. In other words, the overhead of the ATMR voter is smaller than the ATMR-ST voter and the overhead of the ATMR-ST voter is smaller than the TMR voter.

Table II shows the fault-tolerance capability and overhead comparison results among the traditional QMR voter and the proposed AQMR and AQMR-ST voters. Similarly, it can be seen from Table II that the proposed AQMR voter has the smallest delay, area, and power and the traditional QMR voter has the largest delay, area, and power. Therefore, the proposed voters have small overhead compared to the traditional QMR voter. In other words, the overhead of the AQMR voter is smaller than the AQMR-ST voter and the overhead of the AQMR-ST voter is smaller than the QMR voter.

Table III shows the reliability comparison results among the unhardened/hardened latches in terms of *SNU Critical charge (SNU Qcrit)*, *DNU Critical charge (DNU Qcrit)*, *TNU Critical charge (TNU Qcrit)*, *SET Filterability (SETF)*, and *HIS Insensitivity (HISI)*, respectively. For example, DNU Qcrit means the smallest Qcrit of all possible node pairs that can be flipped by a DNU, thus leading to error-retention for the latch. Note that, if a latch is not XNU tolerant, we only need to measure the XNU Qcrit where 'X' here means 'S', 'D' or 'T'. Also note that, if a latch is SNU-tolerant, its SNU Ocrit is '∞', because the latch can tolerate or self-recover from the SNU no matter is the energy level of the striking particle. Therefore, '∞' in Table III also

TABLE I
OVERHEAD COMPARISON RESULTS AMONG THE TRADITIONAL TMR VOTER AND THE PROPOSED TMR VOTERS

Voter	Capability	Delay (ps)	10^{-4}×Area (nm^2)	Power (uW)
TMR Voter	SNU	17.92	2.67	1.02
ATMR (Proposed)	SNU	5.03	1.19	0.56
ATMR-ST (Proposed)	SNU/SET	16.67	1.78	0.94

TABLE II
OVERHEAD COMPARISON RESULTS AMONG THE TRADITIONAL QMR VOTER AND THE PROPOSED QMR VOTERS

Voter	Capability	Delay (ps)	10^{-4}×Area (nm^2)	Power (uW)
QMR Voter	SNU	69.83	5.94	4.95
AQMR (Proposed)	SNU	4.92	1.78	0.81
AQMR-ST (Proposed)	SNU/SET	16.09	2.38	1.18

TABLE III
RELIABILITY COMPARISON RESULTS AMONG THE SNU, DNU, TNU, AND/OR SET UNHARDENED/HARDENED LATCHES

Latch		Qcrit			SETF	HISI
		SNU	DNU	TNU		
Unhardened		5.13	-	-	NO	YES
TMRL		∞	6.42	-	NO	YES
QMRL		∞	∞	9.51	NO	YES
DET-SEHPL [20]		5.34	-	-	YES	YES
LSEH [21]		∞	12.78	-	YES	YES
DNURL [22]		∞	∞	18.75	NO	YES
THLTCH [23]		∞	∞	25.00	YES	YES
TNUDICE [7]		∞	∞	∞	NO	NO
TNUHL [6]		∞	∞	∞	NO	NO
ATMRL	Proposed	∞	6.36	-	NO	YES
ATMRL-ST		∞	6.34	-	YES	YES
AQMRL		∞	∞	9.57	NO	YES
AQMRL-ST		∞	∞	9.39	YES	YES
HITTSFL		∞	∞	∞	YES	YES

means XNU tolerance. Similarly, if a latch is DNU/TNU-tolerant, its DNU/TNU Qcrit is '∞' and vice versa. It can be seen from Table III that only the proposed HITTSFL latch can get three ∞ and two YES, i.e., the proposed HITTSFL latch is the most robust.

The overhead comparison results for alternative latches in terms of delay, area, power, and power-delay product (PDP) which is measured with multiplying power and delay, are shown in the left part of Table IV.

For delay comparisons, it can be seen from Table IV that, the QMRL and TNUHL latches consume a large delay since they use many devices from D to Q; however, they cannot filter SET pulses. Conversely, the DNURL and TNUDICE latches consume a small delay since they use a few devices from D to Q; however, they cannot filter SET pulses either. Note that, to filter SET pulses, an extra delay has to be introduced. Therefore, the SET-filterable latches consume extra delay.

For area comparisons, it can be seen from Table IV that the QMRL latch consumes the largest area mainly since it uses many transistors. Note that, RHBD latches have to use extra transistors, and thus the unhardened latch has the smallest area. Generally, a TNU-tolerant latch has to consume large area. However, the proposed HITTSFL latch consumes the smallest area compared to the TNU-tolerant latches.

For PDP comparisons, it can be seen from Table IV that, the QMRL and TNUHL latches consume a large PDP since they consume extra delay and/or power. Conversely, the Unhardened, DNURL, and TNUDICE latches consume a small PDP since their delay and/or power is reduced. In summary, the above comparisons demonstrate the cost-effectiveness of the proposed HITTSFL latch especially in terms of area and power consumption compared to the state-of-the-art TNU-tolerant latches.

$$\text{POR} = \frac{Compared_{\text{delay}} - Proposed_{\text{delay}}}{Compared_{\text{delay}}} \times 100\% \quad (1)$$

Based on delay of latches in Table IV, *percentages of overhead reduction* (*PORs*) for delay of the proposed HITTSFL latch compared to the alternative latches are measured with Eq. (1), so that the PORs for area and power can be similarly measured (see the right part of Table IV). It can be seen from the right part of Table IV that, in terms of delay, compared to the TNUDICE latch, the HITTSFL latch has to consume an extra 1272.39% delay to ensure SET-filterability; compared to the TNUHL latch, the HITTSFL latch can reduce 78.85% delay; however, these compared latches cannot provide SET-filterability. In terms of area, compared to the TNU-tolerant latches, the HITTSFL latch can reduce 3.26% and 28.55% area, respectively. In terms of power, compared to the TNU-tolerant latches (i.e., TNUDICE and TNUHL), the HITTSFL latch can reduce 44.09% and 15.75% power, respectively. In summary, the above comparisons demonstrate the cost-effectiveness of the proposed HITTSFL latch especially in terms of area and power.

The *process, voltage and temperature* (*PVT*) variations can seriously affect the performance of latches in deep nano-scale CMOS technologies [29]. Figure 10

TABLE IV
OVERHEAD COMPARISON RESULTS AMONG THE SNU, DNU, TNU, AND/OR SET UNHARDENED/HARDENED LATCHES

Latch		Overhead				POR (%)			
		Delay (ps)	10^{-4}×Area (nm^2)	Power (uW)	PDP	ΔDelay	ΔArea	ΔPower	ΔPDP
Unhardened		12.36	1.49	0.35	4.33	-80.99	-497.99	-251.43	-535.57
TMRL		45.46	8.32	1.92	87.28	50.79	-7.09	35.94	68.47
QMRL		99.13	22.57	5.60	555.13	77.43	60.52	78.04	95.04
DET-SEHPL [20]		61.23	3.56	1.20	73.48	63.47	-150.28	-2.50	62.55
LSEH [21]		46.90	4.16	0.64	30.02	52.30	-114.18	-92.19	8.33
DNURL [22]		3.12	9.80	1.18	3.68	-616.99	9.08	-4.24	-647.83
THLTCH [23]		12.38	9.50	1.58	19.56	-80.69	6.21	22.15	-40.70
TNUDICE [7]		1.63	9.21	2.20	3.58	-1272.39	3.26	44.09	-668.72
TNUHL [6]		105.79	12.47	1.46	154.45	78.85	28.55	15.75	82.18
ATMRL	Proposed	20.37	5.64	1.29	26.28	-9.82	-57.98	4.65	-4.72
ATMRL-ST		31.74	6.24	1.40	44.44	29.52	-42.79	12.14	38.07
AQMRL		20.08	9.21	2.09	41.97	-11.40	3.26	41.15	34.43
AQMRL-ST		30.99	9.80	2.20	68.18	27.82	9.08	44.09	59.64
HITTSFL		22.37	8.91	1.23	27.52	-	-	-	-

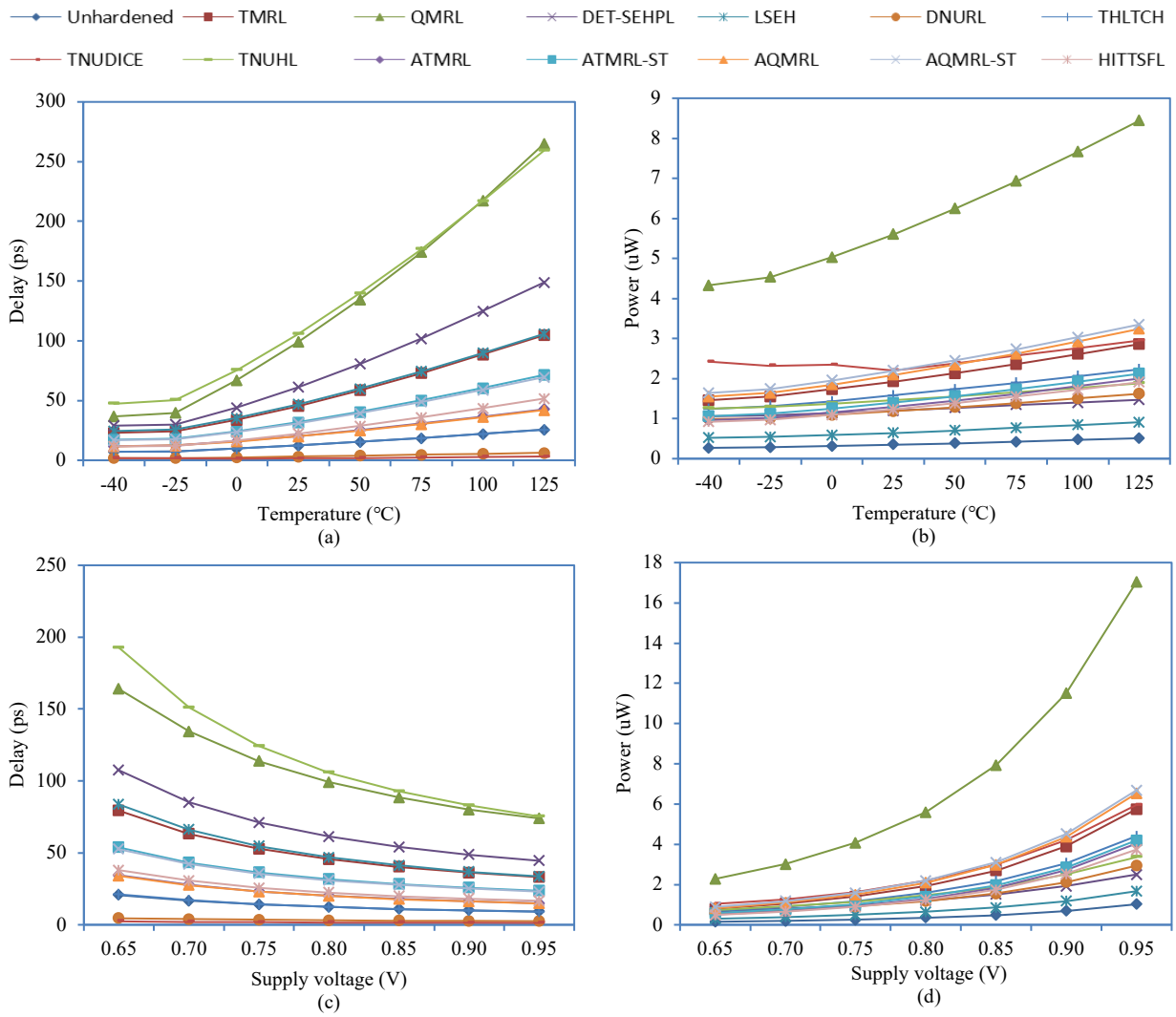

Fig. 10. Estimation results of PVT variation impacts on delay and power for the SNU, DNU and TNU hardened latch designs. (a) Impact of temperature variations on delay. (b) Impact of temperature variations on power. (c) Impact of supply-voltage variations on delay. (d) Impact of supply-voltage variations on power.

shows the results of PVT variation impacts on delay and power for alternative latches. Note that, the normal temperature was set to 25°C and the temperature was ranged from −40°C to 125°C; the normal supply voltage was set to 0.8V and the supply voltage variation was varied from 0.65V to 0.95V.

Figure 10-(a) and (b) show that the alternative latches need to consume more delay and power in general when the temperature is rising, mainly since the carrier mobility will decrease when the temperature increases [29]. It can be seen from Fig. 10-(a) that the QMRL and TNUHL latches are more sensitive to temperature variation on delay, mainly because the carrier mobility decreases rapidly when the temperature increases. However, the TNUDICE and DNURL latches are less sensitive to temperature variation on delay. It can be seen from Fig. 10-(b) that the QMRL latch is the most sensitive to temperature variation on power. However, the Unhardened and LSEH latches are less sensitive to temperature variation on power mainly because the carrier mobility decreases slowly when the temperature increases.

Figure 10-(c) and (d) show that the alternative latches have decreasing delay and increasing power in general when the supply voltage is rising, mainly since the increasing supply voltage can speed up transistor switching but can increase power dissipation [29]. It can be seen from Fig. 10-(c) that the supply voltage variation has the largest impact on the delay of the TNUHL latch, mainly since it uses many devices from its input to its output. However, the supply voltage variation has low impacts on the delay of the other

latches, such as the TNUDICE, DNURL, Unhardened, and the proposed HITTSFL latch, since some of them uses a high-speed path from input to output and the other ones uses fewer devices from input to output. It can be seen from Fig. 10-(d) that the QMRL latch is the most sensitive to supply voltage variation on power, but the other latches such as the Unhardened and LSEH latches are less sensitive to supply voltage variation on power. The reason is that the QMRL latch has the largest area, thus leading to rapid power consumption increment when the supply voltage is increasing. In summary, the proposed latches have moderate sensitivities to variations of supply voltage and temperature, compared to the state-of-the-art hardened latches.

Moreover, to investigate the process variation effect on latches, Monte Carlo simulations were performed using the PVT estimation methodologies from [28]. The threshold voltage and oxide thickness of transistors are generated randomly using the normal distribution with ±5% maximum deviations from the original [28]. Note that, the negative varied values (less than the original ones) on the normal distribution curves for the effective channel length of transistors are mapped to positive ones by coordinate transformation in the HSPICE netlist file, since these variations are almost impossible [28]. To get parameters of average deviation (dev) and standard deviation (σ) for latches, 500 times' Monte Carlo simulations were performed, and the calculation formulas for these parameters are given in the following.

$$\mathrm{dev} = \frac{\sum|X_i - \varphi|}{N} \quad (2)$$

$$\sigma = \sqrt{\frac{\sum(X_i - \varphi)^2}{N}} \quad (3)$$

In Eq. (2)-(3), N, Xi and φ denote, respectively, the number of sample values (equal to 500), the sample values and the standard value (equal to 1 due to the normalization). Accordingly, the normalized average deviation (dev) and standard deviation (σ) for power and delay of latches are calculated and shown in Table V.

From Table V, three conclusions can be drawn. First, compared with the unhardened latch, all the hardened latches have a larger sensitivity to the process variation effect on power, which is mainly due to the increased area for hardening. Second, the QMRL latch has the largest sensitivity to the process variation effect on power mainly since its area is the largest. Third, the DET-SEHPL and LSEH latches have a similar-and-lower sensitivity to the process variation effect for power, compared with most of the other hardened latches. From Table V, three conclusions can still be drawn. First, compared with the unhardened latch, the DNUR and TNUDICE latches have a lower sensitivity to the process variation effect on delay, which is mainly due to the employment of the high-speed transmission path from D to Q. Second, the QMRL latch has the largest sensitivity to the process variation effect on delay, which is mainly because there are many devices from D to Q. Third, the THLTCH and HITTSFL latches have a lower sensitivity to the process variation effect on delay, compared with most of the other hardened latches. In summary, the proposed latches have a moderate sensitivity on the PVT variation effects, compared with most of the state-of-the-art hardened latches.

TABLE V
NORMALIZED AVERAGE DEVIATION (DEV) AND STANDARD DEVIATION (Σ) FOR POWER AND DELAY OF LATCHES

Latch		dev		σ	
		power	delay	power	Delay
Unhardened		1.00	1.00	1.00	1.00
TMRL		3.11	1.89	3.14	1.92
QMRL		4.95	4.19	5.00	4.21
DET-SEHPL [20]		1.53	3.08	1.55	3.12
LSEH [21]		1.14	2.17	1.17	2.20
DNURL [22]		3.16	0.97	3.20	0.99
THLTCH [23]		2.97	1.31	3.03	1.33
TNUDICE [7]		3.87	0.93	3.90	0.96
TNUHL [6]		3.21	4.13	3.23	4.07
ATMRL	Proposed	3.34	2.44	3.36	2.46
ATMRL-ST	Proposed	3.47	1.72	3.50	1.73
AQMRL	Proposed	3.26	1.98	3.30	2.01
AQMRL-ST	Proposed	3.46	1.82	3.47	1.83
HITTSFL	Proposed	3.20	1.68	3.23	1.71

VI. CONCLUSIONS

Due to the high integration and aggressive shrinking of transistor sizes, radiative-particle-induced node-upsets and SETs are becoming severe issues in circuits and systems for safety-critical applications. This paper has proposed a series of voters and those voters based latches (e.g., the first-ever TNU-tolerant HIS-insensitive and SET-filterable latch) to provide high robustness with cost effectiveness. The proposed voters and latches use many inverters to propagate the values stored in the modules to be voted on a common node feeding an SET-filterable ST to provide node-upset-tolerance SET-filterability and HIS-insensitivity. Simulation results have demonstrated the robustness, cost-effectiveness, and moderate PVT-variation sensitivity of the proposed solutions compared to the alternative solutions.

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