On the scaling of EMFI probes

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Outline

- Context & Motivation
- EM fault induction principle
- Scaling factor (theoretical calculation)
- EMFI platform
- Experimental results
- Conclusion

Introduction

- Main drawbacks of EMFI are:
  - Its limited spatial resolution
  - Impact on several blocks leading to IC crashes

- Increasing the spatial resolution implies reducing the EM probes dimension
  - $\Rightarrow$ Reducing their self inductance
  - $\Rightarrow$ Reducing the EM coupling between the probe and the circuit
  - $\Rightarrow$ More powerful voltage pulse generator

What is the cost?

How to choose the appropriate pulse generator?

How to reduce the probes dimension?

How to set the appropriate pulse when changing the probe?

EM fault induction principle

- EMFI exploits the EM coupling between a probe and the power and ground networks of ICs

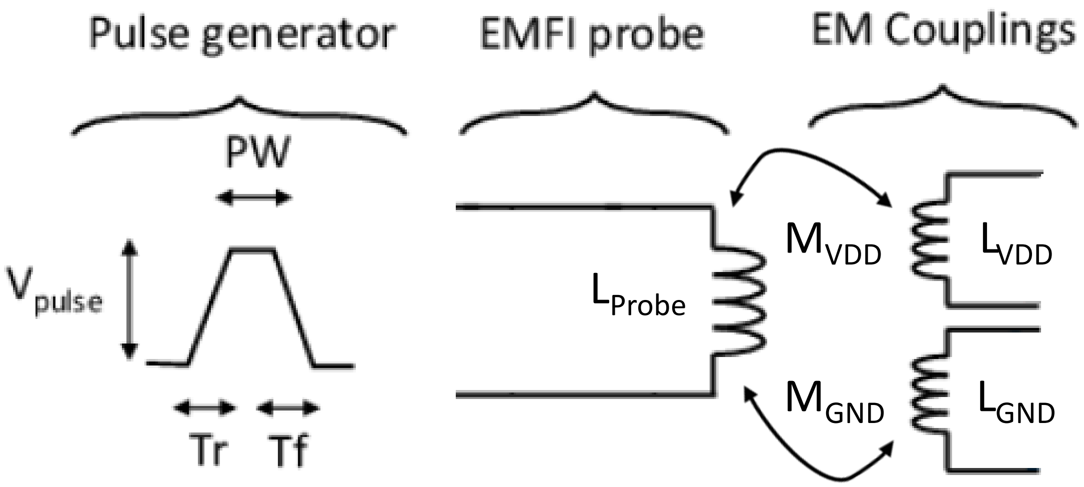
- EM couplings modelling: $M = k \cdot \sqrt{L_P \cdot L_G}$

- V_p applied to the probe induces V_{ind} along each square loop of the power and ground networks:

$$V_{ind} = M \cdot \frac{1}{R_P} \cdot \frac{\Delta V_P}{\Delta t} = M \cdot \frac{1}{R_P} \cdot \frac{V_P}{\Delta t}$$

- Having the same effect with probe 1 and 2:

$$\frac{M_1}{M_2} = \frac{\Delta V_{P2}}{\Delta V_{P1}} = \frac{V_{P2}}{V_{P1}}$$



Scaling down of EMFI probes dimension

- Self inductance of a **<u>square</u>** shape probe of side length W:

$$L_p = \frac{2 \cdot N \cdot \mu_0 \cdot W}{\pi} [log(\frac{W}{R}) - 0.524]$$

- Same effect if :

$$\frac{V_{P2}}{V_{P1}} = \sqrt{\frac{W_1 \cdot [\log(\frac{W_1}{R}) - 0.524]}{W_2 \cdot [\log(\frac{W_2}{R}) - 0.524]}}$$

- An approximation of the scaling factor is:

$$\boxed{\frac{V_{P2}}{V_{P1}} \simeq \sqrt{\frac{W_1}{W_2}}}$$

- Self inductance of a **<u>circular</u>** shape probe of diameter a:

$$L_p = \frac{N \cdot \mu_0 \cdot a}{\pi} [\log(\frac{8 \cdot a}{R}) - 1.75]$$

- Same effect if :

$$\frac{V_{P2}}{V_{P1}} = \sqrt{\frac{a_1 \cdot [\log(\frac{a_1}{R}) - 1.75]}{a_2 \cdot [\log(\frac{a_2}{R}) - 1.75]}}$$

- An approximation of the scaling factor is:

$$\boxed{\frac{V_{P2}}{V_{P1}} \simeq \sqrt{\frac{a_1}{a_2}}}$$

The power of pulse generator of EMFI platforms must be scaled proportionately to the square root of the probe dimensions

EMFI platform equipment

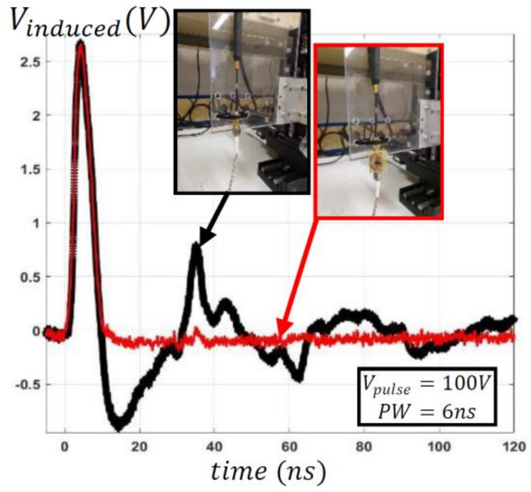
- Voltage pulse generator
  - AVRK4 from Avtech
  - Pulse ranging from 100V to 750V
  - Designed to drive 50Ω loads

- Device under EMFI
  - Xilinx FPGA (spartan3E-1600)
  - Decapsulated
  - Integrating a 128 bits AES running at 50 MHz

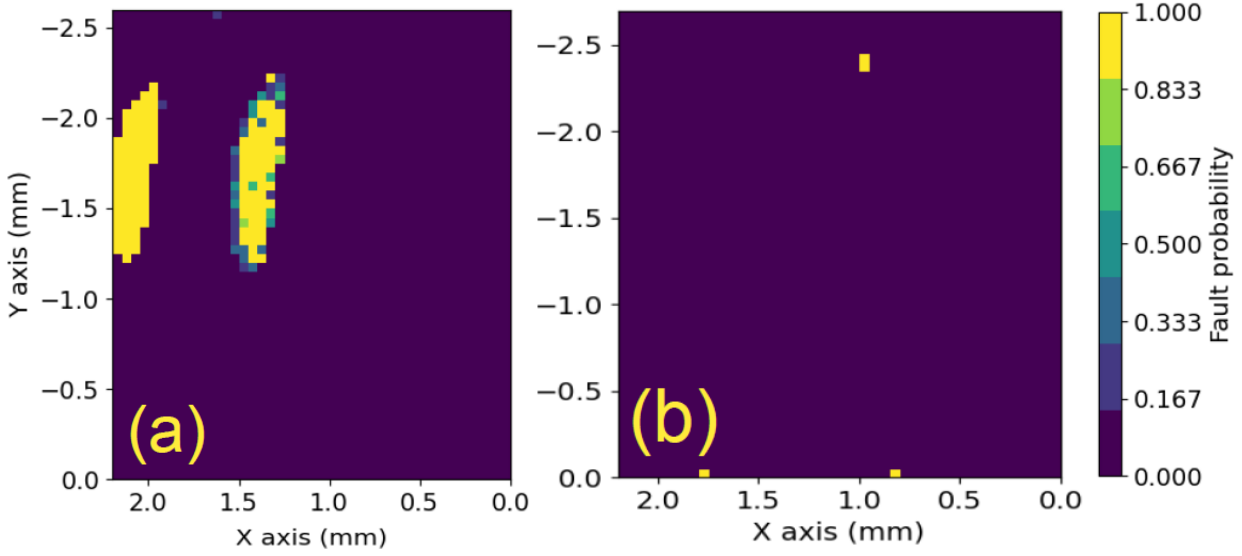
- **Anti-bounce system**
  - Impedance of the EM probes below 1Ω => Impedance mismatch with the pulse generator
  - Signal bounces between the output of the generator and the input of the probes
  - Limitation of the timing resolution of the platform

Anti-bounce system

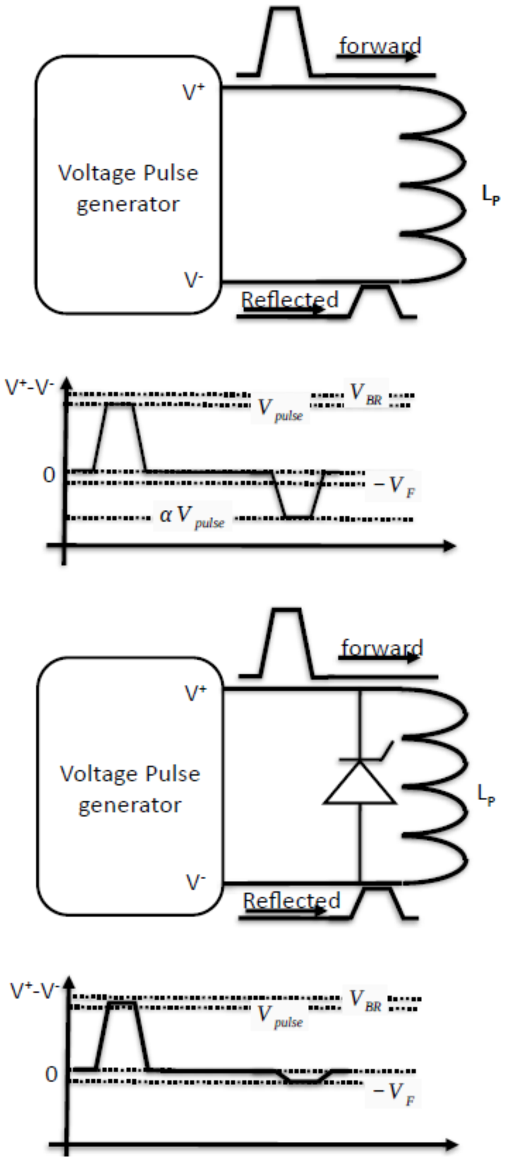
- High speed unidirectional Transil diode: V_{BR} = 570V V_{clamp} = 860V V_F = 1V
- The pulse propagating from V^+ to V^- still gets across the probe if: $V_p = (V^+ - V^-) < V_{BR}$
- The reflected pulse is dissipated by the Transil diode if: $\alpha \cdot V_p = (V^- - V^+) > V_F$ with α Є [0,1]



Measured perturbations induced in a RF3mini probe from Langer (with the same voltage pulse generator settings)

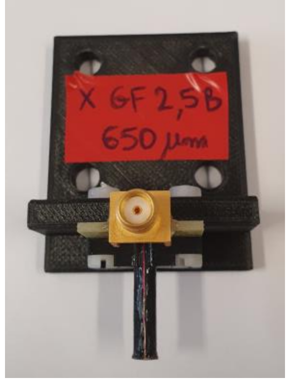


Fault probability maps obtained (a) with and (b) without the anti-bounce system for Vp=450V and PW=10ns

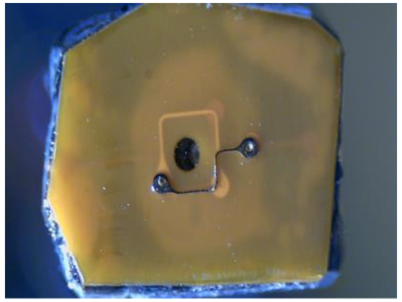


Probes

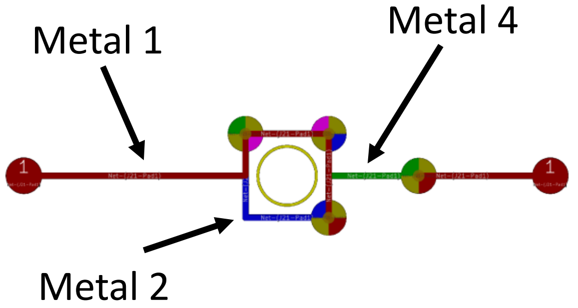
- Advanced flexible electronic technology
- Flexible PCB characteristics:
  - 50µm metal lines
  - 50µm metal spacing
  - 4 layers
- Initial probes for EM fault injection:
  - 2.5 rectangular turns
  - Side length W=300µm, 400µm & 650µm
  - With and without a ferrite core
- Additional probes:
  - 1 or 2 loops
  - Side length W=150µm, 100µm & 50µm
  - Without ferrite core because initially designed for electromagnetic analysis



<u>*Ø 650µm probe*</u>

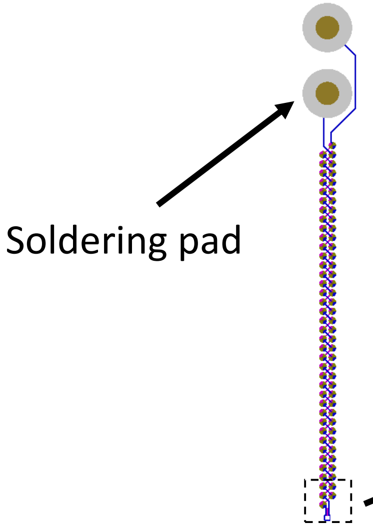


<u>*Ø 650µm*</u>

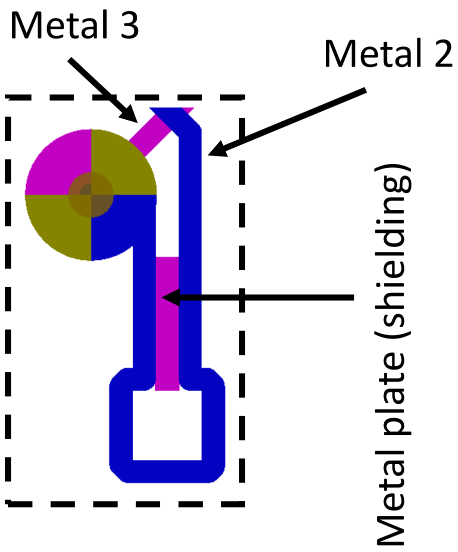


<u>*Flexible PCB layout*</u>

<u>*Ø 150µm probe*</u>



<u>*Flexible PCB layout*</u>



<u>*Probe end*</u>

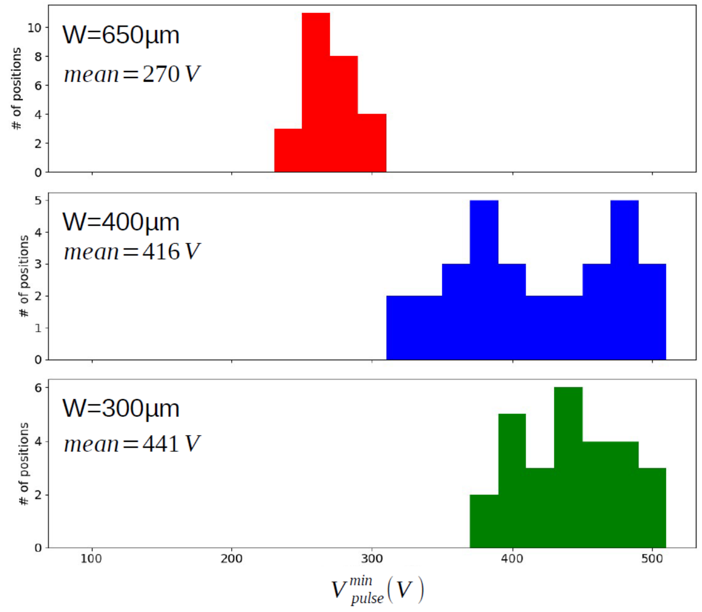
Vp_{min} maps

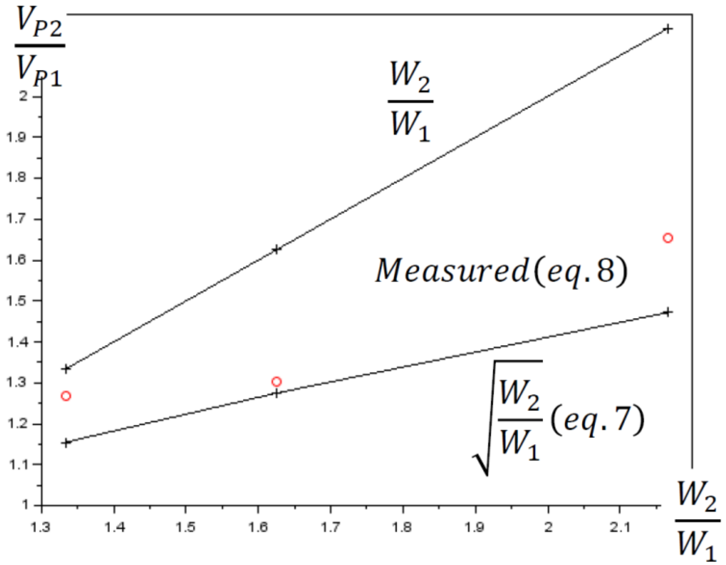
- Near field scans of the same part of the IC surface with the 3 initial probes for EMFI

- Measurement of Vp_{min} to be applied to the probe, at each coordinate, to induce a fault:
  - Displacement step: 100µm
  - Vp range: [100V;500V]
  - Vp step: 20V

- We consider the minimum of Vp_{min} values of each histogram as values robust to map misalignment, so we computed:

$$\frac{V_{P2}^{Exp}}{V_{P1}^{Exp}} \simeq \frac{min(V_{P2}^{min})}{min(V_{P1}^{min})}$$



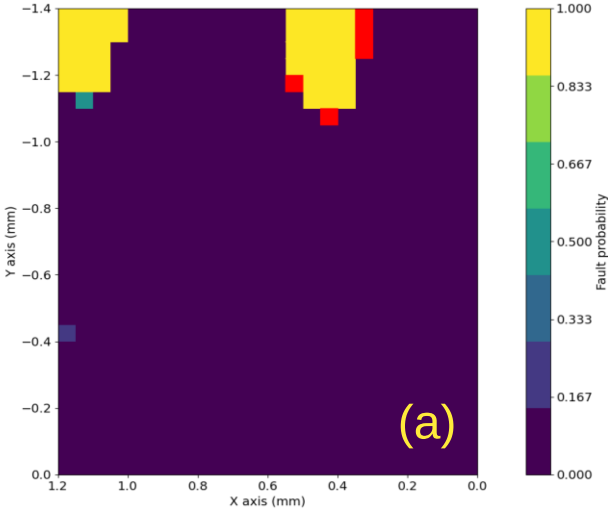


Fault probability maps with different probes

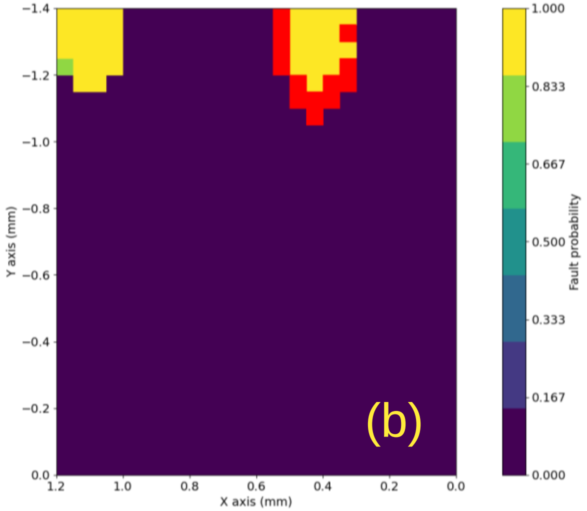
- <u>Circuit scan:</u>

- 6 EMFI at each probe position
- Displacement step of 50µm
- 6 probes (650µm, 400µm, 300µm, 150µm, 100µm and 50µm)
- Probe placed at a distance Z = 50µm from the IC surface
- Reprogramming of the FPGA after the occurrence of each fault to avoid the effect of persistent faults
- Red pixels correspond to positions where EMFI induces a crash (no response) of the device under EMFI

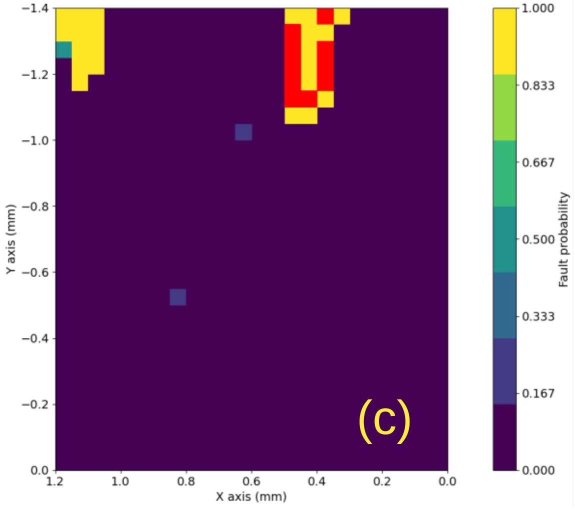
Fault probability maps with different probes



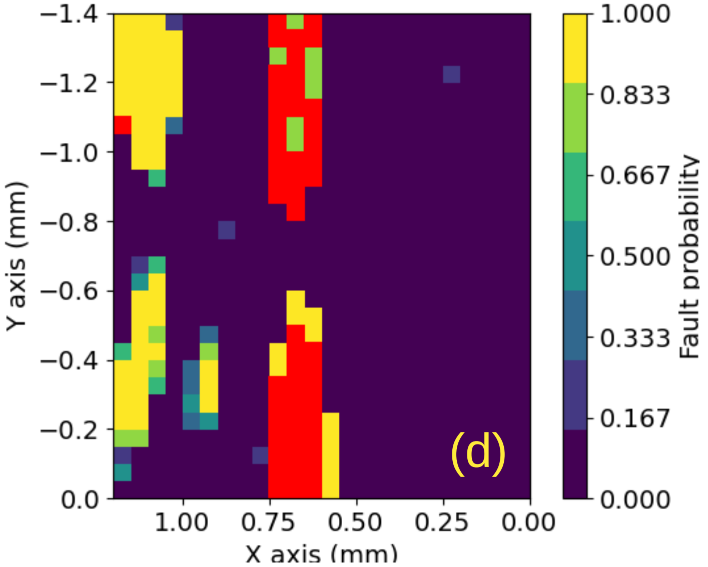
$W = 650\mu m$ $V_P = 240V$



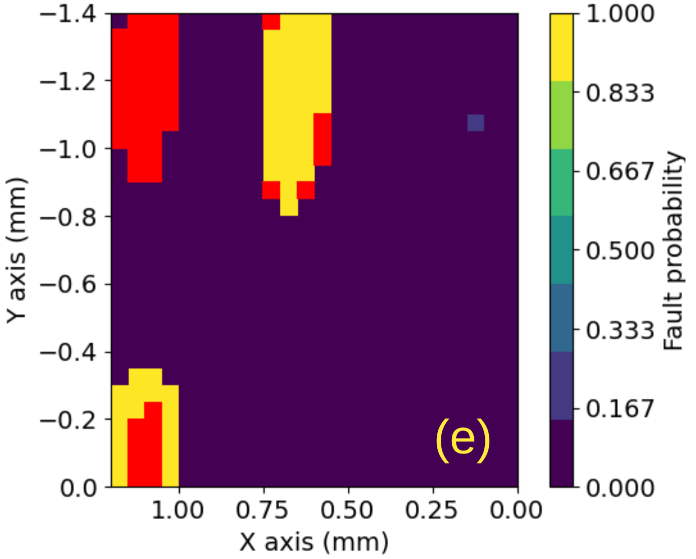
$W = 400\mu m$ $V_P = 330V$



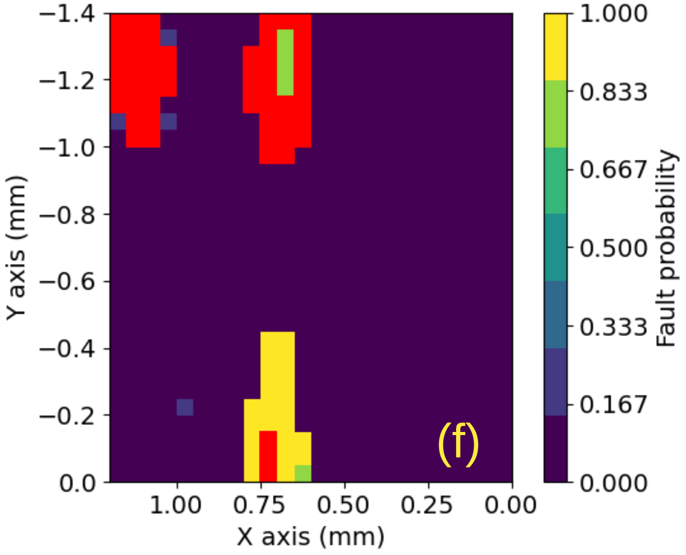
$W = 300\mu m$ $V_P = 400V$



$W = 150\mu m$ $V_P = 520V$



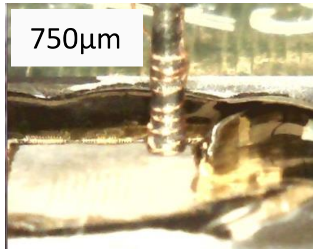
$W = 100\mu m$ $V_P = 630V$

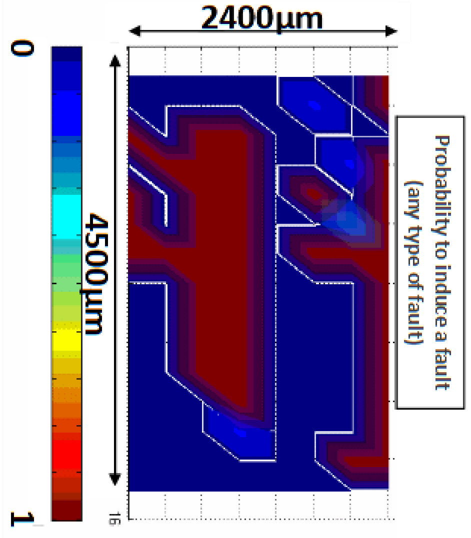


$W = 50\mu m$ $V_P = 780V$

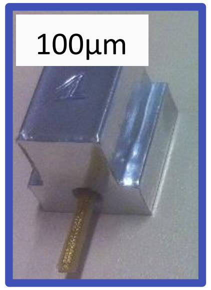
LIRMM progress

2014

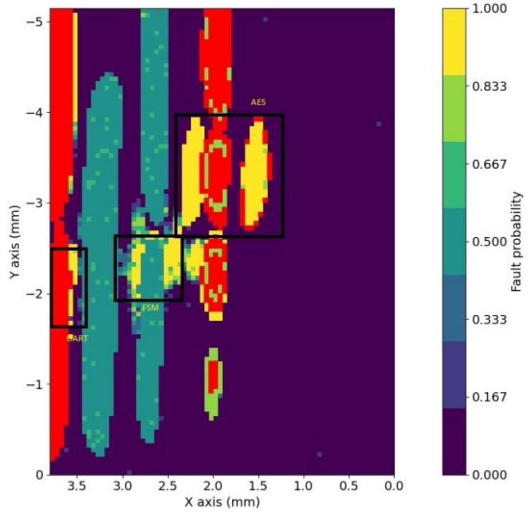




2021



Same device
Same experimentation



Conclusion

- The effect of scaling down the dimension of EMFI probes has been studied both theoretically and experimentally
- It is possible to increase EMFI spatial resolution
- It is possible to design low cost EMFI probes using flexible electronics combined with 3D printing
- The power of pulse generator required to use such probes is not so high
  - $\Rightarrow$ The scaling with probe dimension follows a square root law

Thank you for your attention !

Any questions ?