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Carbon Nanotube SRAM in 5-nm Technology Node Design, Optimization, and Performance Evaluation—Part I: CNFET Transistor Optimization

Rongmei Chen, Lin Chen, Jie Liang, Yuanqing Cheng, *Senior Member, IEEE*, Souhir Elloumi, Jaehyun Lee, Kangwei Xu, *Graduate Student Member, IEEE*, Vihar P. Georgiev, Kai Ni, *Member, IEEE*, Peter Debacker, Asen Asenov, *Fellow, IEEE*, and Aida Todri-Sanial, *Senior Member, IEEE*

***Abstract*— In this article, we propose a carbon nanotube (CNT) field-effect transistor (CNFET)-based static random access memory (SRAM) design at the 5-nm technology node that is optimized based on the tradeoff between performance, stability, and power efficiency. In addition to size optimization, physical model parameters including CNT density, CNT diameter, and CNFET flat band voltage are evaluated and optimized for CNFET SRAM performance improvement. Optimized CNFET SRAM is compared with state-of-the-art 7-nm FinFET SRAM cell based on Arizona State University [ASAP 7-nm FinFET predictive technology models (PTM)] library. We find that the read, write EDPs, and static power of the proposed CNFET SRAM cell are improved by 67.6%, 71.5%, and 43.6%, respectively, compared with the FinFET SRAM cell, with slightly better stability. CNT interconnects both inside and in-between CNFET SRAM cells are considered to compose an all-carbon-based SRAM (ACS) array which will be discussed in the Part II of this article. A 7-nm FinFET SRAM cell with copper interconnects is implemented and used for comparison.**

***Index Terms*— Carbon nanotube field-effect transistor (CNFET) static random access memory (SRAM) cell, energy-delay-product (EDP), FinFET SRAM cell, read delay, static noise margin (SNM), static power, write delay.**

I. Introduction

As CMOS technology continues to scale down, the supply voltage of integrated circuits (ICs) decreases while the density of transistors increases. For the conventional CMOS transistors, as the channel length enters into the nanometer regime, short channel effect like drain-induced barrier lowering (DIBL) threatens the performance of CMOS circuits, including degraded subthreshold slope and increased leakage current. Several emerging technologies have shown good potential of mitigating these problems and extended the lifetime of Moore's law: the transition from planar Si FET to 3-D FinFET enables better control of channel electro-static field, which reduces the impact of short channel effect significantly; another way of reducing the impact is decreasing the thickness of channel region with emerging technologies and materials such as 1-D material [carbon nanotube (CNT), graphene nanoribbon (GNR)]-based field effect transistor (FET) [1], [2], and 2-D semiconductor materials (transition metal dichalcogenides, etc.)-based FET [3]. Insightful comparisons between these two different ways of reducing short channel effect have been investigated in the device, circuit, and architecture level, which shows that the reduced channel layer thickness-based FET allows better-scaled device to extend the Moore's law, and hence higher density and high performance than the FinFET scenario. For example, carbon nanotube FET (CNFET)-based designs can have better performance and density compared to their FinFET counterparts if the fabrication process of CNFET is well-controlled [4]. Up to now, there have been tremendous efforts in improving the controlled syntheses and postgrowth treatments of CNTs, leading to CNFET intrinsic performance approaching the ballistic limit [5]–[7] and highly purified semiconducting CNT (∼99.99%) of narrow diameter distribution [8]. In [9], a total CNFET-based modern microprocessor called RV16X-NANO has been realized and demonstrated after overcoming the intrinsic CNT defects and variations. Furthermore, it has been demonstrated that through well developed CNT growth and transfer techniques, low-temperature integration of CNFET circuits on the conventional silicon substrate is viable and shows high-performance [10], which also enables 3-D heterogeneous integration of CNFETs with CMOS technology [11], [12]. Different from the CNFET (1-D FET), the 2-D FETs such as MoS_2 and WSe_2 still suffer from the large contact resistance between the channel and source/drain of the devices leading to very limited on current and device drive capability [13]. They are, however, of potential applications in low power and flexible electronics.

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Static random access memory (SRAM) is one of the most critical element in ICs where about 70% of the on-chip area is occupied by memory arrays in the modern high-performance microprocessors [14]. Meanwhile, SRAM is also the first element to be investigated in a new technology node. Hence, abundant studies are focusing on FinFET SRAM performance and stability research such as [15]–[17], including both modeling and experimental characterizations. Likewise, some studies analyze the performance and variability of CNFET SRAM and compare it with CMOS SRAM, including both FinFET and planar technologies [18]–[20]. It has been shown that CNFET SRAM has overall advantages over FinFET SRAM in terms of power consumption, read/write performance, and static noise margin (SNM). Moreover, through decoupling the high-temperature CNT synthesis from the SRAM wafer, a low-temperature CNFET SRAM fabrication process was achieved, which also enables the use of buried power rails to potentially further increase the density of CNFET SRAM [21]. There are also some studies that focus on different CNT SRAM cell structure comparisons without optimizing the CNTFET device itself, such as [22]. However, up to now, no study has optimized the CNFET SRAM cell at an advanced technology node (such as 7 nm/5 nm) by comprehensively considering different physical parameters such as CNFET gate size, CNT density, and diameter and CNFET flat band voltage given that these parameters can have a significant impact on SRAM cell performance and stability. For the 2-D FET-based SRAM, there were some works that demonstrated its scalability, good noise margin, and low power such as MoS_2 and WSe_2-based SRAMs [23], [24] and hence it could be well suited for some special application such as IoT (Internet of Things) and medical devices. However, due to the aforementioned huge contact resistance existing in the 2-D-FET it is not a good comparison between the 2-D FET SRAM and the high-performance counterparts as the FinFET and CNFET SRAMs and hence it will not be used as a reference in this work.

In this article, we use the virtual-source CNFET compact model developed by Lee *et al.* [25], [26] to design a six-transistor SRAM cell at the 5-nm technology node where we first optimize the size ratios between pull-up (U), pull-down (D), and access (A) transistors. The compact model has been calibrated either by numerical simulation using non-equilibrium Green's function formalism or experimental data. It is capable of capturing the device parasitic and dimensional scaling effects [25]. In this article, the definition of 5-nm technology node is based on the International Technology Roadmap for Semiconductors (ITRS) 2013 [27] predictions where the contacted gate pitch is 31.1 nm and the minimum ON-state and maximum OFF-state currents are 1.33 mA/μm and 100 nA/μm, respectively [26]. The corresponding optimized CNFET compact model parameters will be introduced in Section II-A. However, it should be noted that these optimized parameters are targeted for logic application at the 5-nm node. For SRAM application, lower power and high density are of more priority than the performance. It will be shown in later part of this article that the number of CNT for each CNFET in SRAM cell, CNT diameter and flat band voltage are three main parameters that need to be adjusted to obtain the desired CNFET SRAM.

Next, we investigate the impact of several physical parameters on CNFET device and optimize them to obtain the best performance (including read/write energy and delay) and static power consumption while preserving acceptable read SNM and write SNM. For comparison reasons, we use the 7-nm FinFET technology from Arizona State University [28], [29] to build a FinFET SRAM cell where the device model parameters have been optimized for the optimal tradeoff between performance and reliability. In other words, the obtained optimized FinFET SRAM results (i.e., SNM, etc.) are used as optimization boundaries as in [30]. The selected 7-nm FinFET technology node is a representation of one of the most advanced technology nodes of silicon. FinFET SRAM of a more advanced node like 5 nm or below will enable it to have more advantage in power, performance, and area compared to the studied CNFET SRAM. For more accurate and efficient exploration of CNFET SRAM performance, power, and SNM optimization, algorithms such as genetic [30], [31] or particle swarm [32]-based optimization can be applied, which are beyond the scope of this article.

Furthermore, in this article, the CNFET SRAM cell is analyzed without considering variability of CNT diameter and chirality (semiconducting or metallic CNTs), doping, and alignment of CNTs in CNFET device or wafer-level [18], [33], [34]. These variations are in addition to the traditional variations in silicon CMOS. However, there are plenty of demonstrated techniques to reduce these variations during circuit design as in [18], [33], and [34]. Similarly, the 7-nm FinFET SRAM variability such as threshold voltage and write driving circuit variation as in [35] are not discussed in this article.

The rest of this article is organized as follows. In Section II, we introduce CNFET and FinFET technologies, and their applications to SRAM design. In Section III, the size optimizations of CNFET SRAM and FinFET SRAM cells are presented. In Section IV, the physical parameters of CNFET SRAM are optimized to get the optimal tradeoff among performance, power, and SNM. Section V concludes this article. SPICE simulations (including Cadence specter and Synopsys HSpice tools) were applied to obtain the various metrics in this article.

II. FinFET and CNFET SRAM Cell Design Methodology

A. General SRAM Cell Optimization Methodology

For an SRAM to have both good read stability and writability, its transistors must satisfy some size (or fin number for FinFET) constraints. In general, the pull-down (D) n-type transistors in the cross-coupled inverters must be the strongest, the pull-up (U) p-type transistors should be the weakest, and the access (A) n-type transistors should be of intermediate strength [36]. As shown in Fig. 1, the transistor pairs T4–T6, T3–T5, and T1–T2 are D-, U-, and A-type transistors, respectively. To achieve the most compact SRAM cell, in this work we set the U transistors to have the smallest baseline size while the D and A transistors are adjusted with size ratios of $\sigma =$ A/U and $\beta =$ D/A, respectively. Both σ and β are varied in the range of 1–3 to search for the optimal size ratios. There are three metrics for the stability or SNM evaluation of an

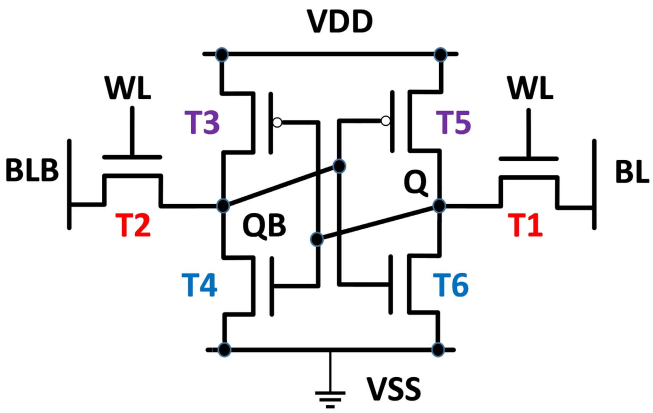

Fig. 1. SRAM cell illustration.

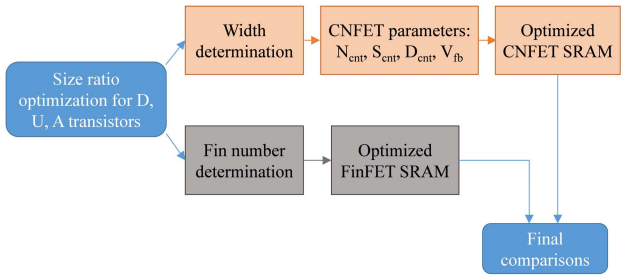

Fig. 2. SRAM optimization flow for both CNFET and FinFET SRAM cells. It should be noted that FinFET device model parameters have been optimized for FinFET SRAM in [28].

SRAM cell, i.e., hold, read, and write margins. Hold noise margin is always larger than the read noise margin, which can then be used as a conservative and representative metric for them. Hence, in this article, only read and write SNMs are evaluated to characterize and assess the stability of an SRAM cell comprehensively. The dc method described in [37] is used to extract these values. Such a method has the same accuracy with the conventional butterfly method, but it is more efficient on parameter extraction. We also apply the performance and power efficiency characterization methods as in [37].

B. FinFET and CNFET SRAM Cell Optimization

Different from conventional planar CMOS technology where nMOS and pMOS transistors have significantly different driving capabilities [38], CNFET and FinFET technologies tend to have similar driving capabilities for n-type FET and p-type FET [25], [28]. Besides, the width of FinFET transistors cannot be adjusted continuously but instead discretely with the number of fins while the driving capability of a CNFET is proportional to the number of CNTs underneath the CNFET. Hence, conventional size recommendation values for planar CMOS SRAM may not apply to CNFET or FinFET SRAM cells; thus, their size reoptimization is essential to get an optimal tradeoff between performance, power efficiency, and stability.

The overall design optimization flow for FinFET and CNFET-based SRAM cells is shown in Fig. 2. The design flow starts with optimization of the pull-up, pull-down, and access transistors size through tuning their width ratio for CNFETs and the number of fins for FinFETs. We utilize

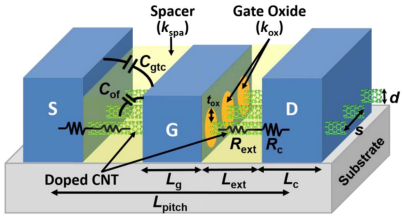

Fig. 3. Reprinted from Lee *et al.* [25] in page of number 3062. Copyright (2021) obtained from the corresponding author of this article, Deng and Wong [39] illustration of CNFET structure and its compact model parameters including the fringe capacitance between gate and CNT (C_{of}) and plate capacitance between gate and source/drain electrodes (C_{gtc}) as analytically modeled. The substrate is assumed to be a thick SiO_2 insulator, which makes the substrate/body have no impact on the performance of CNFET, i.e., no parasitic capacitance between body and electrodes. More detailed description of the CNFET modeling including the contact resistance (R_c), source/drain extension resistance (R_{ext}) [40], and parasitic capacitances are available in [25] and [26].

TABLE I

OPTIMIZED CNFET COMPACT MODEL PARAMETERS AT THE 5-nm TECHNOLOGY NODE. THE ORIGINAL NUMBER OF CNTS UNDERNEATH THE GATE IS 10

Parameters	Symbols	Values
Gate length	L_g	11.7 nm
Electrode-CNT contact length	L_c	12.9 nm
Heavily doped source/drain extensions	L_{ext}	3.2 nm
Electrode height	H_g	20 nm
Gate oxide thickness	t_{ox}	3 nm
Gate oxide dielectric constant	k_{ox}	23
Substrate dielectric constant	k_{sub}	3.9

the optimized FinFET SRAM model at 7-nm technology node available in [28] where the equivalent oxide thickness EOT = 1 nm, gate length $L_{gate} = 21$ nm, and the fin width, height, and pitch are $W_{fin} = 6.5$ nm, $H_{fin} = 32$ nm, and $f_{pitch} = 27$ nm, respectively. Whereas for CNFET SRAM cell, we utilize a baseline model with the parameters of CNFET (n-type/p-type) as illustrated in Fig. 3. The corresponding optimized parameters from [25], [26] for the 5-nm technology node are listed in Table I and are used in this article as well. These parameters are technology node-dependent and are not focused in this study though a more comprehensive evaluation and optimization of CNFET SRAM performance should also consider these parameters impact. The studied and focused parameters in this work include CNT diameter d or $D_{cnt} = 1.2$ nm, CNT center-to-center distance s or $S_{cnt} = 10$ nm (meaning the CNFET has a CNT density of 100 CNTs/μm under its gate), the gate width $W = 100$ nm, and the flat band voltage $V_{fb} = 0.015$ V. We assume that each CNFET contains only semiconducting CNTs, i.e., without the existence of metallic CNTs, of the same diameter. As shown by Mintmire and White [41], semiconducting CNTs with similar diameters have similar density of states and physical properties. The experimental work in [42] has achieved up to 99.9999% semiconducting CNTs which paves the way for large scale CNT circuit manufacture. We further optimize CNFET SRAM with respect to the W, D_{cnt}, S_{cnt}, and V_{fb}. The number of CNTs in the FET channel is estimated by the ratio of gate width, W to CNT spacing, S_{cnt}. Thus, there are ten CNTs in the baseline CNFET device. It should be noted that except for W and V_{fb}, the D_{cnt} and S_{cnt} parameters

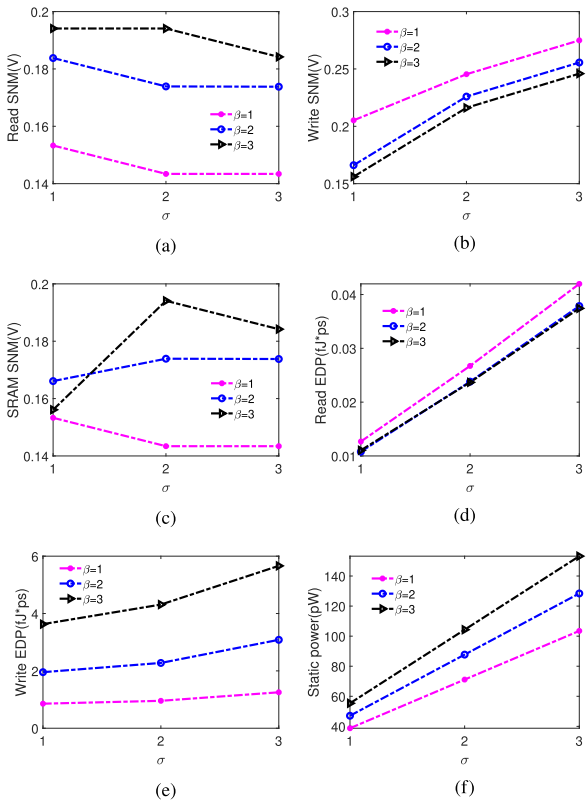

Fig. 4. 7-nm FinFET SRAM cell size optimization results. The fin count of the pull-up p-type transistor is fixed to 1 while other transistor fin counts vary according to σ and β. σ = A/U and β = D/A. (a) Read SNM. (b) Write SNM. (c) Overall SNM. (d) Read EDP. (e) Write EDP. (f) Static power.

are the same and tuned simultaneously for all the D, U, and A transistors in an SRAM cell. Once these model parameters are optimized by trading-off performance, power and noise margin, we compare the 5-nm CNFET SRAM to the 7-nm FinFET SRAM cell.

III. SRAM Cell Optimization

A. FinFET SRAM Cell Optimization

We start by investigating FinFET transistor sizes and their impact on 7-nm FinFET SRAM cell. Power supply voltage was set to 0.7 V for both the FinFET and CNFET SRAMs. We show the read and write SNMs and their dependence on the size of transistors in Fig. 4(a) and (b), respectively. The smaller values of read and write SNM for each case are shown in Fig. 4(c) which represent the most conservative SNM values. Furthermore, the write and read energy-delay products (EDPs) and static power consumptions are shown in Fig. 4(d)–(f), respectively. By trading-off the stability (the larger SNM values mean more stability) and performance (the smaller EDP and static power values the better), we can easily find that values of $\beta = 2$ and $\sigma = 1$ render an optimized SRAM cell size, which indicates that the fin number of U, A, and D FinFET transistors are 1, 1, and 2, respectively. As shown in Fig. 4(c), for SNM values larger than 0.16 V, $\beta = 2$ and $\sigma = 1$ provide the minimum EDP and static power consumption. The corresponding metrics of the FinFET SRAM cell are listed in Table II, which are also used as a baseline case for CNFET SRAM cell optimization.

TABLE II

Optimized Metrics of FinFET SRAM Cell With Nfin_p = 1, Nfin_a = 1, Nfin_n = 2, Which Will Be Used as References for the Optimized CNFET SRAM Results in Table III. The Supply Voltage Is 0.7 V

Metrics	Read	Write
SNM (V)	0.184	0.166
Delay (ps)	0.854	9.795
Energy (aJ)	12.88	199.6
EDP (aJ·ps)	10.79	1955
Static power (pW)	47.07	

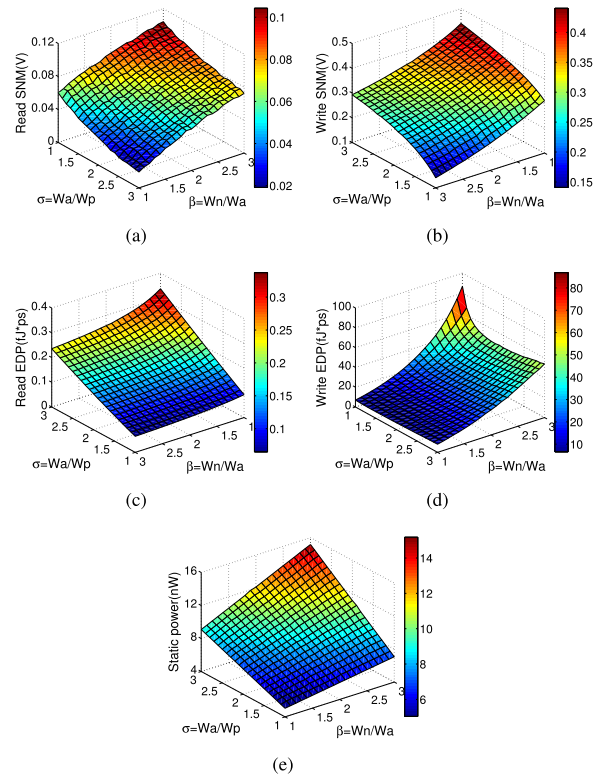

Fig. 5. CNFET SRAM cell size optimization results. The gate width of the U transistors is fixed as 100 nm while the D and A transistors gate widths vary according to the σ and β. Note that for better visualization of the results, the σ and β are scanned from 1 to 3 or the opposite way. σ = A/U and β = D/A. (a) Read SNM. (b) Write SNM. (c) Read EDP. (d) Write EDP. (e) Static power.

B. CNFET SRAM Cell Optimization

The size optimization results for CNFET SRAM cell are shown in Fig. 5. Different from FinFET, here we can tune the width of CNFET gates W for D, U, and A transistors continuously. However, similar to FinFET SRAM cell, we find that the values of $\beta = 2$ and $\sigma = 1$ are an optimum choice for CNFET SRAM cell after trading-off performance and stability. As both CNFET and FinFET, their n-type and p-type transistors have similar driving capabilities, and they directly impact SRAM cell performance and stability during size optimization. However, when comparing these metrics, as shown in Figs. 4 and 5, we find that except the write SNM, the size-optimized CNFET SRAM cell is much worse than the FinFET counterpart. To further optimize the CNFET SRAM cell, we will tune CNFET device physical parameters as described in Section IV.

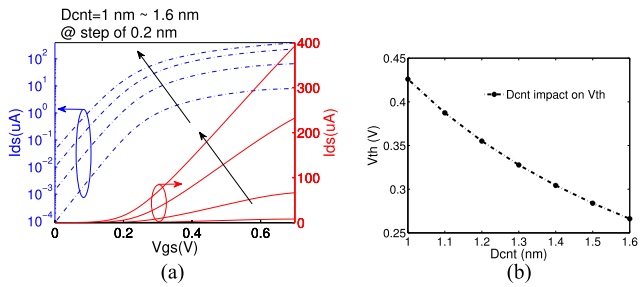

Fig. 6. N-type CNFET I_{ds}–V_{gs} curves ($V_{ds} = 0.7$ V) and V_{th} dependence on CNT diameter. P-type CNFET has a similar behavior. It is assumed that CNFETs only contain semiconducting CNTs, with the closest and representative diameters plotted here. (a) I_{ds}–V_{gs}. (b) V_{th}.

IV. Physical Parameters Optimization for CNFET SRAM Cell

A. CNFET Diameter Optimization

We start by varying the CNT diameter and study its impact on CNFET SRAM performance while other model parameters are the same as those listed in Section II-B. We calculate analytically the CNTFET V_{th} as in (1) [25] considering the short channel effects and the impact of CNT band gap E_g

$$V_{th} = E_g/2 + dV_{th0} + V_{fb} \tag{1}$$

where $E_g = 2E_p * a_{cc}/d$, with the parameters $E_p = 3$ eV, $a_{cc} = 0.142$ nm, and d representing the tight-bonding parameter [41], carbon-to-carbon distance in the CNTs, and the CNT diameter, respectively. dV_{th0} is the roll off threshold voltage resulting from the short channel effects, including the DIBL [25]. V_{fb} is the flat band voltage with positive sign for n-type FET and negative sign for p-type FET [43]. In Fig. 6, we show the simulated results of I_{ds} versus V_{gs} and the corresponding V_{th} versus CNT diameter. Because the CNT bandgap is inversely proportional to its diameter [25], we find that as CNT diameter increases from 1 to 1.6 nm, the CNFET threshold voltage, V_{th} decreases from 0.42 to 0.26 V while increasing I_{ds} on and off currents. However, it should be noted that the CNT diameter has not only impact on the CNFET threshold voltage as (1) describes, it also impacts the contact and extension resistances of the CNTFET as shown in Fig. 3. In general, the contact resistance $R_C \propto e^{(1/d)}$ (when $1/d$ is small) or $\propto e^{(1/2d)}$ (when $1/d$ is large) and the extension resistance is $R_{ext} \propto 1/d^2$. For example, the contact resistance of CNT of 1.1-nm diameter is 106.4k ohm while it is only 38.9k ohm for CNT of 1.2-nm diameter. The details of the relationships between these resistances and CNT diameter can be found in [26]. This is different from the flat band voltage which only changes the threshold voltage of the CNFET and will be discussed in Section IV-B. Moreover, the applied CNFET model has Ohmic metal-CNT contacts which provides better performance and could be realized by heavily doping the source/drain (S/D) extensions [44]. Previous efforts on modeling the Schottky-barrier CNTFETs can be found in [45].

In Fig. 7, we show the results of CNFET SRAM performance with diameter variation. We note a slight increase in write SNM but almost no change in read SNM. Normally an increase in device threshold voltage or on current can lead to an increase in read SNM while write SNM is decreased with

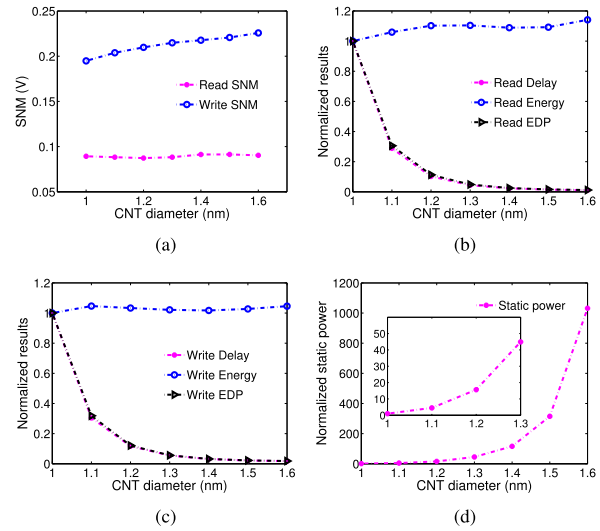

Fig. 7. CNFET SRAM SNM and performance dependence on CNT diameter. It is assumed that CNFETs only contain semiconducting CNTs, with the closest and representative diameters plotted here. (a) SNM. (b) Read performance. (c) Write performance. (d) Static power.

the device threshold voltage but not sensitive to the on current variation [46]. Hence, the CNT diameter increase induced on current increase and threshold voltage reduction can cancel out each other's impact on the read SNM. Nevertheless the write SNM can be increased due to the threhold voltage reduction. Both read and write energy are not sensitive to CNT diameter change, whereas, write/read latencies and EDPs are decreased significantly, especially when CNT diameter increases from 1 to 1.2 nm. This is because the read and write energy is more dependent on the parasitic capacitance in the SRAM cell and bitline than the on current of CNFETs while the read/write speed is directly impacted by the drive current if we assume the same parasitic capacitance. So if on current of CNFET is increased with CNT diameter, the write/read energy will be changed slightly while their speed can be improved significantly. Static power consumption increases as CNT diameter is increased from 1 to 1.6 nm as shown in Fig. 7(d), especially after 1.1 nm (see the inset plot). Hence, to tradeoff CNFET SRAM performance (CNT diameter $\geq$ 1.1 nm) and static power consumption (CNT diameter $<$ 1.2 nm) without degrading its read and write noise margins, we choose 1.1-nm CNT diameter, which will be used for other parameters optimization afterward. It should be noted that, the speed of CNFET SRAM can be improved significantly by increasing the CNT diameters as illustrated in Fig. 7 at the price of slightly increased dynamic read and write power but a significant increase in static power. For example, if the diameter of CNT is increased from the optimized 1.1 to 1.2 nm, the speed of CNFET SRAM will be similar to the FinFET-SRAM. The dynamic read and write energy will be increased by 8% (but still much better than the FinFET one) while the static power will be around 3.5 times of the FinFET counterpart. Moreover, in the current CNFET compact model, the band to band tunneling (BTBT) current is not fully modeled because phonon-assist and trap-assist tunneling are not considered and the inelastic BTBT effect is not taken into account as well [47], [48]. Hence, an increase in leakage

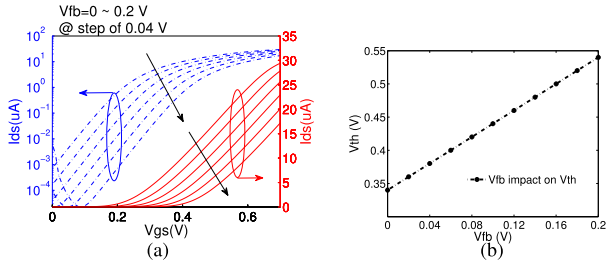

Fig. 8. N-type CNFET I_{ds}–V_{gs} curves ($V_{ds} = 0.7$ V) and V_{th} dependence on flat band voltage V_{fb}. The p-type CNFET has the similar trends with a negative V_{fb}. (a) I_{ds}–V_{gs}. (b) V_{th}.

current is expected in a realistic CNFET SRAM with the same parameter configuration to the work here.

B. CNFET V_{fb} Optimization

The work function difference between the gate metal and CNTs determines the flat band voltage, and it can impact the device performance. Different gate metal materials such as aluminum and palladium can be used to adjust the work function of metals [49], which will further modulate the CNFET threshold voltage as shown in (1). In Fig. 8(a), we show the impact of flat band voltage V_{fb} on I_{ds}–V_{gs} curves. The explored range of V_{fb} is from -0.2 to 0.2 V, which is within the experimentally tested range (-1 to 1 V) [43]. The analytically calculated results of V_{th} as a function of V_{fb} are shown in detail in Fig. 8(b). As shown in Fig. 9(a), with the V_{fb} increase, the SNM of SRAM is improved significantly by bringing closer the read and write SNMs. As it was shown in Fig. 5(a), this phenomenon implies that the V_{fb} increase leads to higher ratio of driving capability of the pull-down CNFETs to that of the pull-up CNFETs due to not symmetric impact of V_{fb} on n-type and p-type CNFETs. Notably, at $V_{fb} = 0.18$ V, read and write SNMs are the same ~0.185 V, which is higher than the FinFET SRAM SNM of 0.166 V.

However, as V_{fb} increases, the performance of CNFET SRAM degrades. For example, both read and write delays increase with V_{fb} despite a slight decrease in their dynamic power consumptions [as in Fig. 9(b) and (c)]. For the static power consumption, as shown in Fig. 9(d), we observe first a decreasing and then an increasing trend, with minimum power at $V_{fb} = 0.12$ V. Such V_{fb} corresponds to read SNM of 0.156 V, which is slightly lower than the FinFET SNM of 0.166 V. Hence, to optimize CNFET SRAM, we try to find the minimum V_{fb} that corresponds to an SNM not less than that of FinFET in order to attain the best available access stability. We select the value of $V_{fb} = 0.16$ V, which has read and write SNM of 0.167 and 0.181 V, respectively.

C. CNT Count and Density Optimization

To explore the best performance of CNFET SRAM while making a fair comparison to FinFET SRAM, we reduced the number of CNTs for the pull-up CNFET from the default ten tubes to the minimum one tube. This also corresponds to the number of fins in FinFET, where the CNFETs access and pull-down transistors have one and two tubes, respectively, to satisfy the $\beta = 2$ and $\sigma = 1$ optimal device size ratios.

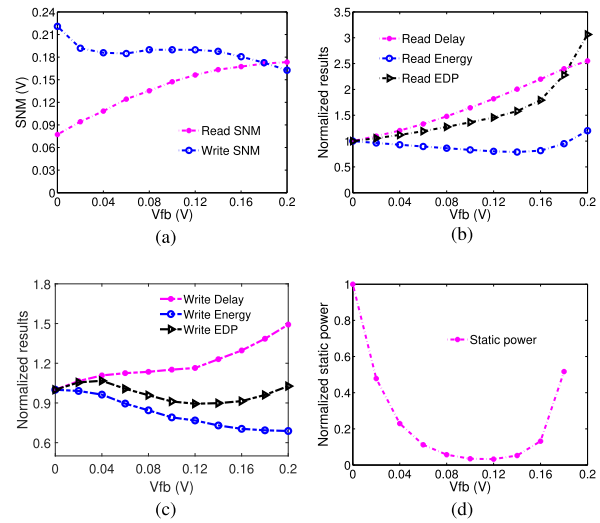

Fig. 9. CNFET SRAM SNM and performance dependence on flat band voltage V_{fb} of n-type CNFET. P-type CNFET has the same trend but with negative V_{fb} values. (a) SNM. (b) Read performance. (c) Write performance. (d) Static power.

We also change the CNT density by adjusting the spacing between tubes from $S_{cnt} = 10$ to 2.5 nm [43], which leads to a decrease in gate width and further the gate–drain and source capacitances. Because the CNT number for each CNFET in the SRAM is kept constant, the CNT density change has a negligible impact on I–V characteristics of CNFET, and neither SNM nor static power consumption of CNFET SRAM is affected by CNT density. Nonetheless, thanks to the increase in CNT density (while fixing the number of CNTs), the decrease in parasitic capacitance leads to improved read and write performances, as shown in Fig. 10.

Once each physical parameter is optimized through the simulation steps mentioned above, the final extracted metrics are listed in Table III. The normalized results correspond to the ratio of CNFET SRAM's metrics to those of FinFET SRAM (as listed in Table II) to quantify their differences. By comparison, CNFET SRAM has a considerable advantage over FinFET SRAM in both static and dynamic power consumptions, with static power, read and write energy only 56.4%, 11.4% and 13.2% of the optimized 7-nm FinFET SRAM cell, respectively. Thanks to this power efficiency advantage, read and write EDPs are also better for the CNFET SRAM (32.4% and 28.5% those of FinFET SRAM, respectively) despite the speed degradation. Furthermore, the optimized CNFET SRAM has similar stability to the FinFET SRAM, with even slightly higher write SNM. It should be noted that for the optimized physical parameters (including gate length, CNT diameter, CNFET work function, etc.) in Table III, all of them have been experimentally demonstrated to be achievable/achieved in the articles [25], [26]. The only exception is the CNT density under the gate. However, it has been proven that the CNT density under the gate of 500/μm can be realized by using the methods of Langmuir–Schaefer based [50], and so on. Meanwhile, the recent article [42] also shows high density (~200/μm) and high semiconducting CNT purification (>99.9999%) wafer level production of CNFET. In addition, similar to the stacked MOS transistor, the CNFET can also

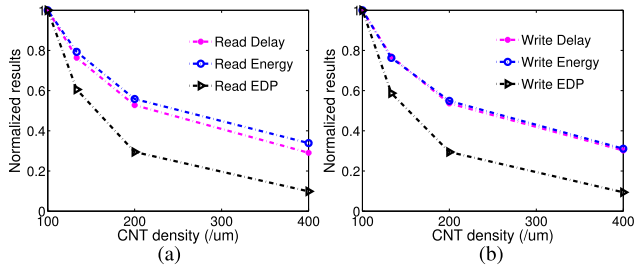

Fig. 10. CNFET SRAM performance dependence on CNT density ranging from 100 to 400 CNTs/μm, corresponding to S_{cnt} of 10–2.5 nm. (a) Read performance. (b) Write performance.

TABLE III

EXTRACTED METRICS FOR OPTIMIZED CNFET SRAM CELL WITH THE NUMBER OF CNTS 1, 1, AND 2 FOR PULL-UP, ACCESS AND PULL-DOWN CNFETS, RESPECTIVELY. THE SUPPLY VOLTAGE IS 0.7 V

Metrics	Read (normalized)	Write (normalized)
SNM (V)	0.167 (0.91)	0.181 (1.09)
Delay (ps)	2.38 (2.79)	21.22 (2.17)
Energy (aJ)	1.468 (0.114)	26.29 (0.132)
EDP (aJ·ps)	3.50 (0.324)	557.9 (0.285)
Static power (pW)	26.53 (0.564)	
Leakage current /CNT (pA)	2.3 (4.96 for 1 fin FinFET)	
CNFET physical parameters		
D_{cnt}=1.1 nm, V_{fb}=0.16 V, S_{cnt}=2.5 nm (400 CNTs/μm), R_C=106.4k ohm		

be stacked with more two or more layers of CNT array in a CNFET gate [51] to achieve several times increase in the equivalent CNT density under the gate of CNFET.

D. Variability Discussion of CNFET SRAM

As mentioned in the introduction of this article, the variability of SRAM is not covered in this article. However, it should be noted that the CNFET devices are sensitive to various sources of parameter variations which are very different from the CMOS counterparts and these variations can further lead to CNFET-based logic gate delay variation [52], [53] and also impact CNFET SRAM performance, variability and reliability. Two big sources are the CNT diameter and the purity of semiconducting CNTs at the wafer level. In CNFET, the variation in V_{th} is mostly attributed to the diameter of CNTs in CNFETs as illustrated in Fig. 6 of this article. To obtain a narrowly distributed CNT diameters, the process of CNT manufacture needs to be continuously improved. The metallic CNT will lead to large leakage current in CNFET SRAM and meanwhile degrade performance/noise margin for the CNFET SRAM. In the work [42], up to 99.9999% semiconducting CNTs is achieved with 1.45 ± 0.23-nm diameter. Besides the control of CNFET SRAM cell variability at the process level and in the cell design stage, the peripheral circuit can also be designed and optimized to improve read and write noise margins. As demonstrated in [54], a negative bitline scheme (NBL) can be used as a write-assist technique and a disturbance-noise reduction (DNR) scheme is effective to assist read operation for high density and high performance SRAM arrays at 14-nm node, respectively. These techniques can also be applied to the studied CNFET SRAM in this article as they are not very technology dependent.

V. CONCLUSION

This article provides comprehensive evaluations and optimizations of 5-nm CNFET SRAM cell by determining the optimal parameters of CNFET devices including CNT diameter, flat band voltage, CNT spacing, and density. The optimized 5-nm CNFET SRAM cell has overall better or comparable metrics than the optimized 7-nm FinFET SRAM cell. Notably, the write and read EDPs, and static power consumption of CNFET SRAM cell are improved by 67.6%, 71.5%, and 43.6%, respectively compared with the optimized 7-nm FinFET SRAM cell, with even slightly better stability. The optimized gate widths for the pull-down, access and pull-up transistors in CNFET SRAM are 5, 2.5, and 2.5 nm, respectively, and the CNFET physical parameters are $D_{\text{cnt}} = 1.1$ nm, $V_{\text{fb}} = 0.16$ V, and $S_{\text{cnt}} = 2.5$ nm (400 CNTs/μm). In Part II of this article [55], a CNT SRAM array will be proposed using the optimized 5-nm CNFET SRAM cell and CNT interconnects [56]–[62] to emulate an all carbon-based SRAM (ACS) array. The ACS will be compared with a FinFET SRAM array composed of the optimized 7-nm FinFET SRAM cell with copper interconnect in the perspectives of area, performance, stability, and power efficiency.

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