Iterative Method for Performance Prediction Improvement of Integrated Circuits

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***Abstract*— Currently, the design flow of digital integrated circuits relies on the use of pre-characterized libraries. These libraries, pre-calculated outside of any context, are used at each step of the design flow to predict the performance of the circuit. They are necessary for the calculation of a wide variety of characteristics, including the IR Drop. However, the behavior of the logic gates described in these libraries is not representative of the real power supply of the standard-cells and this difference is even more important as the number of logic gates in the circuits increases. In this paper, we will show that with the current design flow, the use of these libraries leads to an underestimation of the circuit performances. To remedy this, we propose an iterative approach based on a new use of voltage-adaptive libraries that allows to compute the IR Drop more precisely and thus to better predict the performances of the circuits.**

Keywords—Design flow, IR Drop, libraries, performances.

I. INTRODUCTION

Nowadays, for designing a digital integrated circuit, the expert must verify the correct operation of the circuit at each step of the design flow and with regard to the different parameters. The main external parameters are called PVT and refer to the variations of manufacturing Process (P), supply Voltage (V) and Temperature (T). Ever-increasing number of components in circuits, manufacturing transistor fluctuations, power supply and temperature, which are stochastic phenomenons, move towards an increasing impact on integrated circuit performances especially in advanced semiconductor technology nodes [1].

These parameters are included in the design flow through the use of pre-characterized libraries. This is called the corner method. This conventional design method consists in using simple best- and worst-case combinations of the PVT parameters to predict the circuit performances. Indeed, with the help of CAD tools, the designer implements the application by ensuring, at each step of the flow, the achievement of the specifications but also the correct circuit operation regarding both transistor manufacturing fluctuations and circuit environment (power supply, temperature). However, this worst-case modelling is considered unrealistic and tends to be rejected [2]. The necessity to adopt a better approach is demonstrated in [1].

Moreover, the logic gates in a circuit are not supplied directly by the external power supply (V_{DD}), know generally at ±2%, but by the same source delivered through a power grid. This power grid is resistive, and the resistivity increases significantly as the size of the technologies is reduced [3]. As the process reduced from 28nm to 7nm, conductor resistance through the power grids has increased by factor 10. This resistivity induces voltage Drop and, as a result, each logic gate has a proper local supply voltage (Vi) lower than the one available at the regulator's output. It is well known that power grids can cause timing errors. For this purpose, IR Drop analysis [4] helps the designer to counteract the negative effects of the latter.

IR Drop is included in common design closure by a fixed limit of 10% of external supply. In our case, IR Drop estimations are made with Voltus IC Power Integrity Solution [5]. As a rule of the thumb, if the IR Drop of a circuit is over 10%, it is admitted that its impact on the delays will be too important and therefore the circuit, as it stands, is not validated. This margin is fixed in this way, and its application has shown that it is intended to be pessimistic. The value of IR Drop is calculated from libraries, but we will see in this article that there is a misuse of those libraries which leads to an over-estimation of the IR Drop.

The libraries describe the behavior of each standard-cell of the used technology. These files describe mainly the consumption and the delays of the standard-cells and are classified according to the PVT parameters. Then, using these libraries impose to work with a fixed supply voltage, temperature and manufacturing process for all the gates in the circuit. This procedure is not suitable for working with unknown and variable Vi. Therefore, we propose in this paper a new approach which assign to each gate a corresponding part of library. For this study, we focused on variations of voltage supply, manufacturing process and IR Drop. Temperature is considered constant.

The remainder of this paper is organized as follows. In sect. II, we will give more details about libraries and IR Drop in actual design flow. Then, we propose a new iterative approach in sect. III. The results will be described in sect. IV. Conclusion and perspectives of this article are provided in sect. V.

II. LIBRARIES AND IR DROP IN DESIGN FLOW

In this section we will explain the use of libraries and IR Drop in the current design flow. We will also demonstrate why we consider libraries to be inaccurate and how their use leads to an over-estimation of the IR Drop.

A. Libraries use in the current design flow

The logic gates of the libraries are pre-characterized a priori, i.e., before their integration within a logic path. The libraries are composed of look-up tables. These look-up tables allow to describe the behavior of the logic gates according to the parameters of the library (PVT) and also the input net transition and output net capacitance. At each step of the design flow, the designer uses these look-up tables to ensure the achievement of the specifications and the correct circuit operation (see Fig. 1). The tools used by designers are becoming more and more precise and complex in their calculations. This is in order to have results that are closer to reality. But whatever the level of calculation, the data used are those found in the look-up tables. However, for calculations of more complex phenomena, we notice that these data are not adapted anymore.

As seen on Fig. 1, the IR Drop is calculated at almost the end of the design flow. The designer uses the library corresponding to the corner with the worst IR drop, i.e., high voltage, best process, and high temperature to estimate the IR Drop in the circuit. The result is then compared to the fixed margin of 10% to determine if the circuit is validated or not. At this stage, the supply grid has been considered. Each logic gate actually sees a proper supply voltage Vi provided by the power grid and depending on the IR Drop generated in its area. However, the library used to deal with this the IR Drop, at gate-level, is still the same and characterized for only one value of V_{DD} (high). Moreover, only one library is used for all the gates in the circuit. This does not correspond to the fact that Vi varies over the entire surface of the circuit, and that each standard-cell has its own power supply Vi. In this paper, it will be shown that it is possible to use several libraries for the same simulation with a single circuit.

B. Libraries misuse

The use of libraries in the usual design flow is not adapted to the variations of IR Drop. Indeed, the designer calculates the IR Drop using a library that describes the behavior of the logic gates in the circuit for a given power supply.

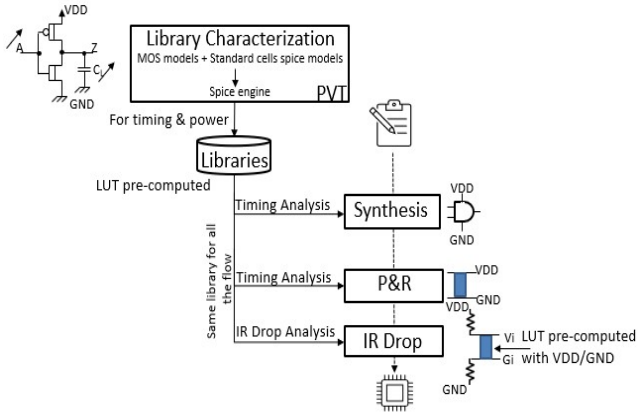

Fig. 1. The different stages of the current design flow.

However, as an activity necessarily induces IR Drop, it is impossible for a logic gate to receive all the expected power supply. Its real performances will be lower than those described in the library. In other words, it is impossible to precharacterize the performance of a logic gate as a function of VDD. This is because it depends on the IR Drop, generated by the gate itself and also by the standard cells surrounding it. Then, as the IR Drop is overestimated in the actual design flow, a more realistic estimation of the IR Drop in the circuit will give a lower value. This concept is illustrated on Fig. 2. As it is shown, with precharaterized standard-cell libraries, the IR Drop is overestimated compared to reality. With this overestimation, the 10% rule is troublesome. Indeed, it shows that a circuit could appear to be below the 10% margin when in reality it is not the case. This prediction error is also linked to the process. In fast process, the logic gates commute faster and consume more power. So, the IR Drop generated will be higher. And the error between the theoretical supply voltage used in the libraries and the actual supply voltage will also be greater.

Then, the overestimation of IR Drop calculated in the usual way will also be higher. However, it is precisely in this case (fast process) that the IR Drop is calculated with the actual design flow to be compared to the 10% limit. Finally, the risk is again to have to rework unnecessarily the design.

By using libraries adapted to the context of each standard-cell, we could therefore gain in precision on the estimation of the IR Drop and obtain a more realistic IR Drop value. This decrease of the IR Drop leads to a gain on the temporal performances of the circuit and could allow to improve the efficiency, the power consumption or the surface of the circuit. The objective of the second part is to describe the method that will allow to estimate more precisely the IR Drop.

III. ITERATIVE APPROACH

In this part, a new approach to the use of libraries is proposed as a solution to the problems outlined above. This method is iterative. Indeed, it consists in repeating the classical design flow several times. We will describe the modifications to be made to the flow and how to link these cycles together.

A. Working environment

The first step is to design the circuit with CAD tools. The most important point is the library file. It must contain the libraries corresponding to the usual corners.

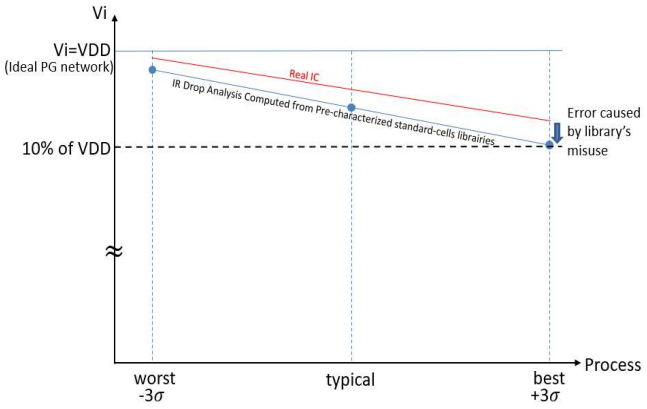

Fig. 2. Impact of the misuse in libraries on IR Drop calculation

For example, the library corresponding to the worst-case corner used for setup timing calculations is the low voltage, worst process and high temperature library: *wc_LV_HT.lib*. The difference with the current design flow (fig.1) is that the libraries must be available on several power supply values. The purpose is to have libraries that can cover all possible values of Vi, the value of the supply voltage delivered to the standard cell from the power grid, i.e., the value after deducting the IR Drop. The power supply values of the libraries must go from V_{DD}-$Drop_{max}$ to V_{DD}-$Drop_{min}$ with a step that will depend on the needs. The work in this paper shows that a step of about 10 mV seems to be consistent. In order to replace permute active libraries during the design flow, the logic gates in the different libraries must not have the same name; the names of the logic gates of a library must be specific to this library. In this way, two different libraries can be assigned to two physically identical gates. For instance, *NAND2X4* can be declined to *NAND2X4_0.9* and *NAND2X4_0.8* if they belong to libraries characterized for 0.9V and 0.8V respectively .

The second step is to correctly set up these logic gates and libraries in the initialization files. It must contain all the names of the standard-cells for all Vi values, but their physical LEF description remains the same. The corners also need to be assigned to the corresponding libraries. Once the environment is set up, the circuit can be placed and routed the usual way with design tools. In this paper, the method is applied with Genus [6] and Innovus [7].

B. Method

Once all the libraries are ready for use and the circuit is placed and routed, the IR drop is calculated using Voltus. So, Fig. 3 shows the result of an IR Drop analysis. Each square represents a standard cell, so this figure shows the IR Drop at the supply point of each cell. This first analysis is done with the usual way. For this example, the IR drop varies from 88mV to 99mV. These results must then be retrieved in a log file. If the method is applied on Voltus, the *report_power_rail_result* command can be used to obtain a file giving the IR Drop value for each instance in the circuit. The next step is to process this file. In this paper, the process is done with Python. The objective is to create an Innovus tcl command file that will replace the standard cells of each instance by those corresponding to their new supply voltage value after deduction of the IR Drop. This step, as well as all the steps of the method, can be seen in the Fig. 4. Processing the IR Drop report in Python allows to both list all the standard-cells and assign them their new power supply value, which is closer to reality.

For instance, the IR Drop analysis indicates that a NAND2X4 logic gate instantiated as g1516 has an IR Drop value of 98.1 mV. The supply value of the new library associated with g1516 will therefore be 801.9mV (V_{DD} - 98.1 = 801.9). If there is a step of 5 mV between the libraries, the library used will be the one with the closest value. Then, we will find the following command in the Innovus tcl command file:

```
EcoChangeCell -cell NAND2X4_0.800 -inst g1516
```

Once the file is fully written, it can be sourced in Innovus to reassign all standard-cells. Fig. 5 shows an exemple of libraries switching on the whole surface of a circuit.

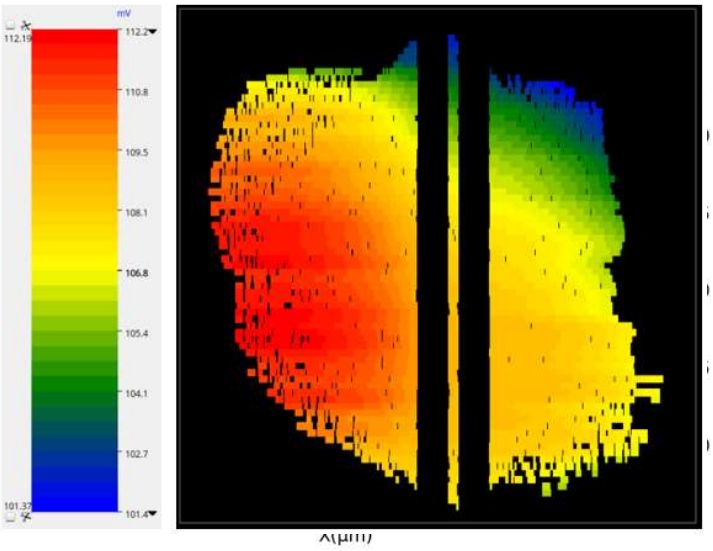

Fig. 3. Result of the IR Drop analysis made by Voltus on a test circuit

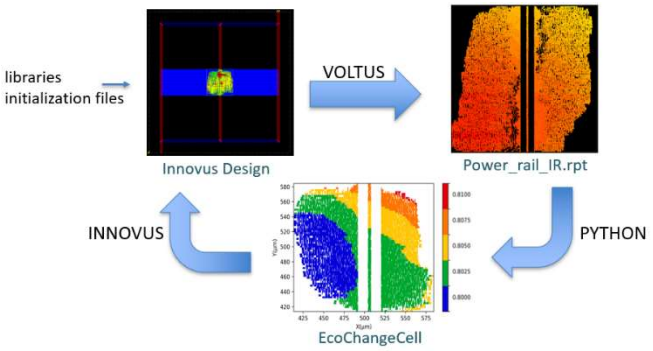

Fig. 4. Explanatory diagram of the iterative method presented in this article

The libraries are now reassigned and the design flow can be followed as if it were a new circuit. The IR drop of the circuit is then re-calculated from the new libraries. For this second cycle, the values of IR Drop decrease significantly. Indeed, the libraries are characterized at the real supply voltages of the circuit, whereas for the first cycle the supply voltages were ideal. During the second cycle the standards will have less activity and will generate less IR Drop. With this second IR Drop result, the library assignment operation can be repeated to start a new cycle. It is then necessary to perform as many cycles as necessary to stabilize the IR Drop value. The work presented in this paper shows that about 3 cycles are needed to stabilize the IR Drop value. However, the exact number of cycles always depends on the context and the desired accuracy.

C. Delays estimations in the method

In the usual design flow, delays are calculated after placement and routing and before taking the IR Drop into account. These delays are inaccurate because they are calculated for an ideal power supply. We can say that these delays are **not IR-aware**. The link between the delays and the IR Drop is made only through the 10% margin, despite the inaccuracies induced. However, with the presented method, the delays are re-calculated after the last assignment of libraries. As the libraries are re-assigned based on the IR Drop, the obtained delays are now **IR-aware**.

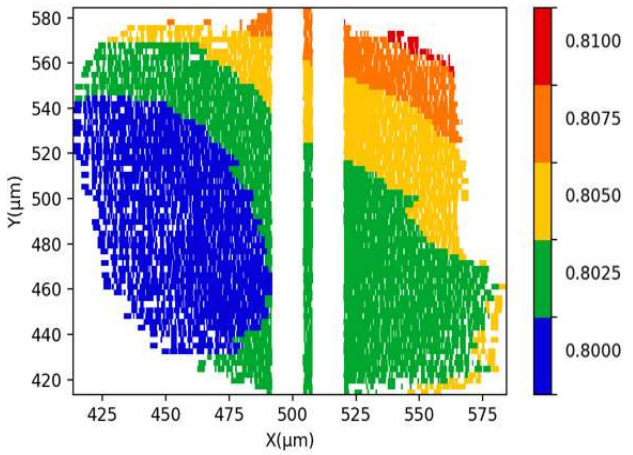

Fig. 5. Supply voltage of the libraries assigned to each standard-cell on the whole circuit for the first iteration

This method allows us to obtain a more precise idea of the values of the delays. Moreover, if these delays are IR-aware, so the 10% IR Drop margin becomes obsolete. The removal of this pessimistic margin could lead to a gain in performance.

In summary, this iterative method (Fig. 4) requires the availability of libraries covering a wider range of supply values. Indeed, it consists in performing several IR Drop analysis by reassigning the library corresponding to the correct power value to each instance of the circuit between each analysis. A priori, 3 IR Drop analysis are necessary. Performing these 3 iterations allows to obtain a stable and more accurate IR Drop value. Knowing the IR Drop of the circuit and being able to integrate it with the use of the libraries allows to calculate the IR-aware delays.

IV. Application and Results

In this section, we apply the iterative method to a simple circuit and compare the results with actual design flow. A 32bit-multiplier is taken as an example (see Fig. 6). This multiplier is made from 65nm technology and composed by 7k logic gates. Its area is 1 mm² and it has a clock period of 3600ps. This multiplier has been designed so that its IR Drop is relatively large and around the 10% margin, in order to be able to correctly illustrate the remarks. The results are specific to this circuit, but it can be extended to any type of circuit.

A. Evolution of IR Drop

The IR Drop is calculated for each standard-cell at each iteration as described in the method. It is therefore possible to plot the Vi seen by a standard-cell as a function of the iterations (see Fig. 7). Iteration 0 is equivalent to the current design flow. The value of Vi at iteration 0 is 992mV. The value of V_{DD} used for IR Drop analysis is 1.1V. It's corresponding to the high voltage for this technology. So, the IR Drop at iteration 0 is 108mV or 9.81% of the external supply voltage. With the classical design flow, the circuit operation seems to be bordeline, but acceptable. It doesn't exceed the limit of 10% IR Drop. On the second cycle, the IR Drop significantly decreased, as expected. With the iterative approach, Vi is stabilized at 997mV, i.e. an IR Drop of 103mV. IR Drop has thus decreased by 4.6% of its value, and it now reaches 9.3% of the external supply value. The value of IR Drop has decreased slightly. It is still quite close to the 10% limit.

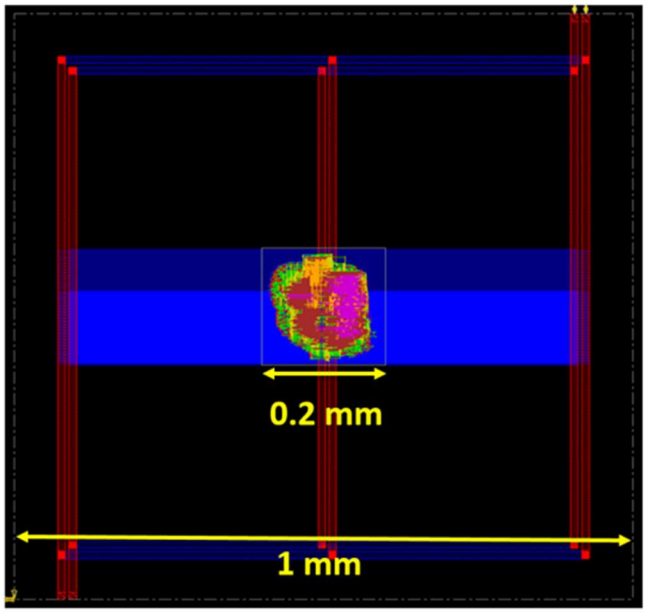

Fig. 6. Evolution of Vi calculated at each iteration seen by a standar-cell placed in the middle of the circuit

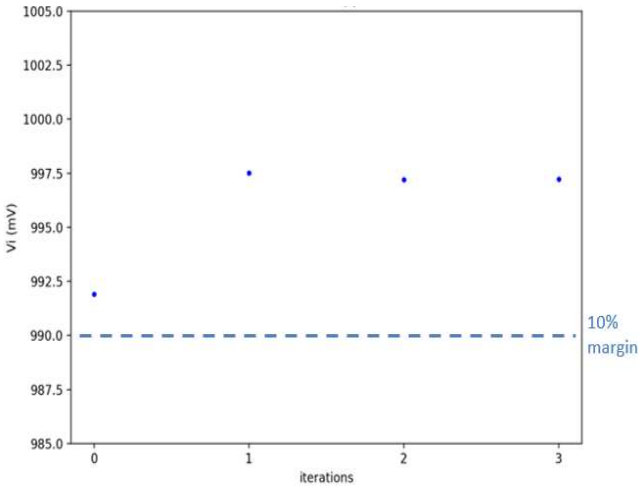

Fig. 7. Evolution of mean Vi calculated at each iteration

B. Evolution of delay estimations

One of the advantages of the iterative method is to be able to calculate IR-aware delays. Thus, the uncertainty about the 10% rule will be eliminated. Indeed, it is very interesting to remove this uncertainty in the case of the multiplier because the value of IR Drop is very close to the limit. As for the IR Drop, the delays at iteration 0 are the same as the delays calculated with the classical design flow. As a reminder, these delays are not IR-aware. With the iterative method, it is possible to recalculate them at each iteration, i.e., at each time we change the libraries. These delays are then calculated according to the IR Drop value of the previous iteration. Finally, as the IR Drop is constant on the last iteration, the delays of the circuit are also stabilized.

Fig. 8 compares the final delays (last iteration) to the initial delays of the logical paths for the multiplier. The setup critical path delay has been slowed down by 16%. The setup critical path delay is used as operating condition of the circuit as it represents the longest path. If this delay is correct, all the

delays are validated. This increase in delays was expected as this delay is IR-aware, unlike to the initial delay. This increase in delay goes hand in hand with a 5% decrease in overall circuit power. However, the clock period being 3.6ns and the critical path delay being 3.9ns the timing slack is negative. The timing slack being the time remaining until the next clock edge, if this one is negative, then the results do not make it possible to validate the correct operation of the circuit.

Moreover, these delays being IR-aware, they become much more accurate and closer to the real values. This induces news reflections. In case of positive critical slack time, it would be possible to use the critical path and its slack time to accurately determine the delay margin of the circuit and to use it to reduce the power consumption or the size of the circuit. As a reminder, the slack time of a logical path is the time remaining between its arrival time and the clock edge. By precisely knowing this time it would be possible to estimate the number of gates that could be reduced in size.

As expected, Fig. 8 also shows that the longer the paths, the greater the impact on delays. We could go further in our thinking. Reducing the size of logic gates means a gain in circuit area but also in power consumption. These gates become slower, but they will generate even less IR Drop. Repeat the iterative analysis of the IR Drop on the circuit with these new gates could be interesting. Obviously, our example of multiplier does not have enough gates for such an optimization to be relevant. However, this reflection leads to interesting optimization perspectives.

In summary, the results of the iterative method show that the performance of this 32bit-multiplier circuit, which didn't seem guaranteed, is actually correct. Moreover, the results on the IR-aware delays open doors for reflection on the optimization of the circuit in terms of area and power consumption.

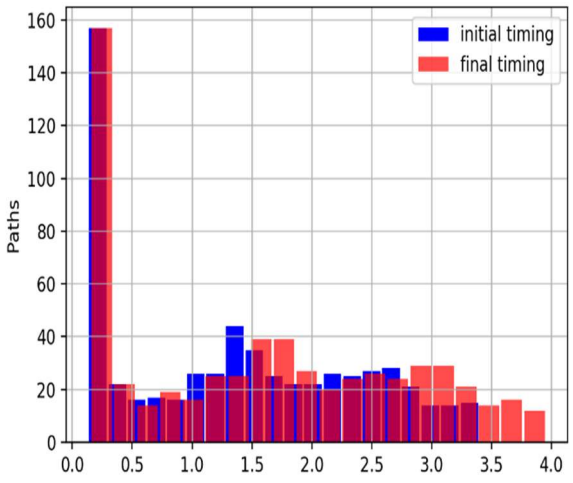

Fig. 8. Final and IR-aware delays obtained by the iterative method, compared to the initial delays

V. Conclusion and Perspectives

The classical design flow has its limits with the miniaturization of the technologies used in the design of integrated circuits, in particular to manage IR Drop issues. Indeed, there is a double pessimism in this flow :

- the fixed margin of 10% of IR Drop which is not necessary and

- the misuse of libraries which leads to an over-estimation of the IR Drop.

In this paper, we have presented a new iterative method to overcome these problems. This method is based on a use of libraries adapted in supply voltage. It consists in conducting several consecutive IR Drop analyses by re-adapting the supply voltage of the libraries used at each iteration and assign a different library to each standard-cell.

By applying this method to the 32bit-multiplier circuit presented, we obtain a better estimation of the IR Drop. The circuit, which had a global IR Drop slightly under 10%, could be considered as operating correctly. However the estimation of real IR Drop leads to IR-aware delays calculation, and IR-aware delays showed that the operation of the circuit was not guaranteed.

Computing the IR-aware delays allows to confirm the good operation of the circuit and open some perspectives. Indeed, having a precise margin on the delays could allow to optimize the circuit in terms of area and power consumption. This is one of the main avenues for future works. This method should also be compared to other tools that are emerging such as Tempus PI [3] from Cadence, released in November 2020.

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