Quadruple and Sextuple Cross-Coupled SRAM Cell Designs With Optimized Overhead for Reliable Applications

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***Abstract*—Aggressive technology scaling makes modern advanced SRAMs more and more vulnerable to soft errors such as single-node upsets (SNUs) and double-node upsets (DNUs). This paper proposes two SRAM cells; the first one is called Quadruple Cross-Coupled SRAM (QCCS) and the second one is called Sextuple Cross-Coupled SRAM (SCCS). The QCCS cell comprises four cross-coupled input-split inverters to keep stored values, and provides self-recoverability from SNUs at low cost. To improve reliability, the SCCS cell uses six cross-coupled input-split inverters to construct a large error-interceptive feedback loop and hence robustly keep stored values. The SCCS cell can self-recover from all possible SNUs and one part of DNUs; for remaining DNUs, a node-separation mechanism is used to avoid their occurrence. Simulation results demonstrate the robustness of the proposed cells. Moreover, compared with the state-of-the-art hardened cells, i.e., NASA13T, RHBD12T, We-Quatro, Zhang14T, QUCCE12T, DNUSRM, QCCM10T, QCCM12T, S4P8N, and S8P4N, the QCCS cell reduces read access time by 17%, write access time by 19%, power dissipation by 4% and silicon area overhead by 10% on average, while the SCCS cell reduces read access time by 44% as well as write access time by 13% on average at the cost of moderate increase in power dissipation and silicon area overhead.**

***Index Terms*—SRAM cell, radiation hardening, circuit reliability, soft error, double-node upset**

I. Introduction

IT is reported by the *International Technology Roadmap for Semiconductors* (*ITRS*) that CMOS technologies will reach approximately 3nm by 2021 [1], significantly improving the integration and performance of circuits and systems. However, with these advanced nano-scale CMOS technologies, the amount of critical charge stored on a node in a circuit decreases due to the decreasing supply voltages and node capacitances. As a result, advanced CMOS circuits and systems are becoming more and more prone to soft errors induced by the striking of particles, such as protons, heavy particles, electrons, muons, and alpha particles [2]. Soft errors may cause the logic value stored inside SRAM cells to be flipped, thus possibly causing serious system failure. Therefore, it is crucial to propose novel SRAM design techniques to solve reliability issues caused by soft errors. The FinFET technology can reduce the soft error rate at transistor or cell level [3], but effective and scalable solutions for soft error tolerance are still highly required.

When a radiation particle hits a storage module, the corresponding single node will collect the generated wrong charge and thus the logical value of the node may be flipped, which is called a *single node upset (SNU)*. Moreover, with the aggressive CMOS technology scaling, circuit integration is becoming much higher and node spacing is becoming much smaller. As a result, one striking-particle may simultaneously affect two OFF-state transistors in a storage element due to multiple-node charge-collection mechanisms [5], causing a *double-node upset* (*DNU*). SNUs and DNUs can cause invalid value-retention in a storage element, which is an important component of modern advanced circuits and systems. Consequently, to improve the robustness of circuits and systems that must be protected against potential value flipping, incorrect value reading, or even serious system failures, both SNUs and DNUs have to be mitigated.

To mitigate SNUs and/or DNUs using a *radiation hardening by design* (*RHBD*) approach, many novel designs of latches [6-8] and flip-flops [9-11] have been proposed. Similarly, several designs have also been proposed for hardening of *static random access memory* (*SRAM*) cells [12-30]. Note that for triple-node upset tolerance, some storage cells have also been proposed as in [31, 32]. However, they are mainly used for aerospace applications in a harsh environment. SRAM hardening for reliable applications is the focus of this paper. The traditional SRAM memory cell, referred to as 6T, consists of six transistors, four of which are used to store values and the two others are used for access operations. Since the 6T cell cannot tolerate SNUs, many IC designers have proposed various types of hardened SRAM cells to enhance reliability. Typical SNU hardened cells include NASA13T [18], RHBD12T [19], We-Quatro [20], Zhang14T [21], QUCCE12T [22], QCCM10T [24] and QCCM12T [24]. Typical DNU

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hardened cells include DNUSRM [23], S4P8N [25] and S8P4N [25]. However, these cells still suffer from some severe problems described below.

(1) To provide complete SNU tolerance, some SRAMs use costly additional techniques, such as enlarging sizes of some transistors [18], increasing spacing between nodes [19], identifying sensitive and insensitive nodes [20].

(2) Many SRAMs are not very effectively hardened against DNUs. For example, neither RHBD11 [17] nor RHBD13 [17] can effectively tolerate DNUs, and they even cannot tolerate SNUs (because they use a reliable component such as C-element and Schmitt trigger to keep values; however, the output of the component is fed to its inputs).

(3) Many SRAMs suffer from large overhead, especially in terms of long read access time [18, 21]. Moreover, some of the cells still suffer from long write access time and high power dissipation [18].

Regarding previous works, the SRAM cell in [23] suffers from large overhead. More than one node in the cell in [24] cannot self-recover from SNUs. The SRAM cell in [25] has only four DNU-recoverable pairs of nodes. These issues motivate us to propose low cost and highly reliable SRAM cells. This paper first presents a reliable *Quadruple Cross-Coupled SRAM (QCCS)* cell with optimized area overhead for reliable applications. The storage module of the cell consists of four interlocked input-split inverters and the cell can self-recover from SNUs. Then, we propose *a Sextuple Cross-Coupled SRAM* (*SCCS*) cell protected against both SNUs and DNUs. The storage module of the cell consists of six interlocked input-split inverters, and the transistors among these inverters are cross-coupled to provide high reliability. Simulation results demonstrate the reliability and optimized overhead for the proposed SRAM cells.

The rest of this paper is organized as follows. Section II describes typical existing SRAM cells. Section III and IV describe the schematic and working principles of the proposed QCCS and SCCS cells, respectively. Section V presents the comparison and evaluation results of alternative cells. Section VI concludes the paper.

II. Typical SRAM Cells

Fig. 1 shows the schematics of typical SRAM cells, including the 6T, NASA13T [18], RHD12T [19], We-Quatro [20], Zhang14T [21], QUCCE12T [22], DNUSRM [23], QCCM10T [24], QCCM12T [24], S4P8N [25], and S8P4N [25]. Fig. 1-(a) shows the schematic of the traditional 6T cell. It can be seen that the 6T cell mainly consists of a couple of cross-coupled inverters. The 6T cell is widely used because of its simple structure and small area. However, the 6T cell is very vulnerable to soft errors. Therefore, in recent years, many researchers have devoted significant efforts to develop effective approaches for radiation hardening of SRAM cells.

The schematic of the NASA13T cell [18] is shown in Fig. 1-(b). The schematic of the cell is divided into three parts. The left-top part is used as a primary storage module with a write block. The left-bottom part acts as a secondary storage module. The right part is a special block for reading values. The read and write blocks ensure its read-ability and write-ability. Compared with 6T, NASA13T provides a higher level of protection against SNUs hence providing soft-error tolerance. However, it still cannot tolerate SNUs that are caused by very high energy particles.

The schematic of the RHBD12T cell [19] is depicted in Fig. 1-(c). It uses twelve transistors, in which NMOS transistors N1 and N2 are used as access transistors. The storage module of the cell consists of ten transistors, in which P1 to P6 are PMOS transistors and N3 to N6 are NMOS transistors. Due to the special structure of feedback loops, the RHBD12T cell is completely SNU-hardened. However, only one pair of nodes (i.e., <S0, S1>) of the cell is DNU-hardened.

Fig. 1-(d) shows the schematic of the We-Quatro cell [20], which has four interlocked storage nodes: A, B, C, and D. It can be seen that, the access transistors N6 and N8 connect B (and C) to BL, and the access transistors N5 and N7 connect A (and D) to BLN. The parallel access transistors make the storage nodes concurrently accessed during read and write operations. Thus, the We-Quatro cell provides a good access performance. However, only some single nodes can tolerate SNUs and only one pair of nodes (i.e., <C, D>) can tolerate DNUs for the cell.

The schematic of the Zhang14T cell [21] is shown in Fig. 1-(e). The cell has six storage nodes: A, B, C, D, E, and F. It can be seen that the gates of transistors P3, P4, N3, and N4 are connected with the ground and/or supply voltage, respectively. Moreover, the gates of transistors P5, P6, N5, and N6 are connected with E, F, C, and/or D, respectively; the assess transistors Na and Nb connect B (and A) to BL (BLN), respectively. Thus, the Zhang14T cell can offer significant improvement in write performance. However, it cannot tolerate DNUs.

Fig. 1-(f) shows the schematic of the QUCCE12T cell [22]. It mainly consists of four cross-coupled input-split inverters, thus forming a large error-interceptive feedback loop to robustly retain stored values. It can be seen that the access transistors N1 and N5 connect Q and B to BL, and the access transistors N2 and N6 connect QN and A to BLN, to make the storage nodes concurrently accessed during read and write operations. However, the QUCCE12T cell still cannot tolerate DNUs.

Note that, the above-mentioned SRAM cells cannot provide enough ability to recover from DNUs. To improve this capability, the DNUSRM cell [23] has been proposed. It can be seen from Fig. 1-(g) that this cell consists of 24 transistors, i.e. PMOS transistors P1 to P8 and NMOS transistors N1 to N16. N9 to N16 are access transistors and their gates are connected to word-line WL. BL and BLN are bit-lines, while Q, QN, and S0 to S5 are internal nodes that are responsible for keeping values. Due to the special structure of feedback loops, the DNUSRM cell is completely DNU-recoverable. However, the cell has very large area and timing overhead.

The schematic of the QCCM10T cell [24] is depicted in Fig. 1-(h). It can be seen that cell is composed of 10 transistors in which P1 to P4 are PMOS transistors and N1 to N6 are NMOS transistors. Transistors N5 and N6 are used for access operations and their gate terminals are connected to word-line WL. Due to parallel and interlock feedback loops of the

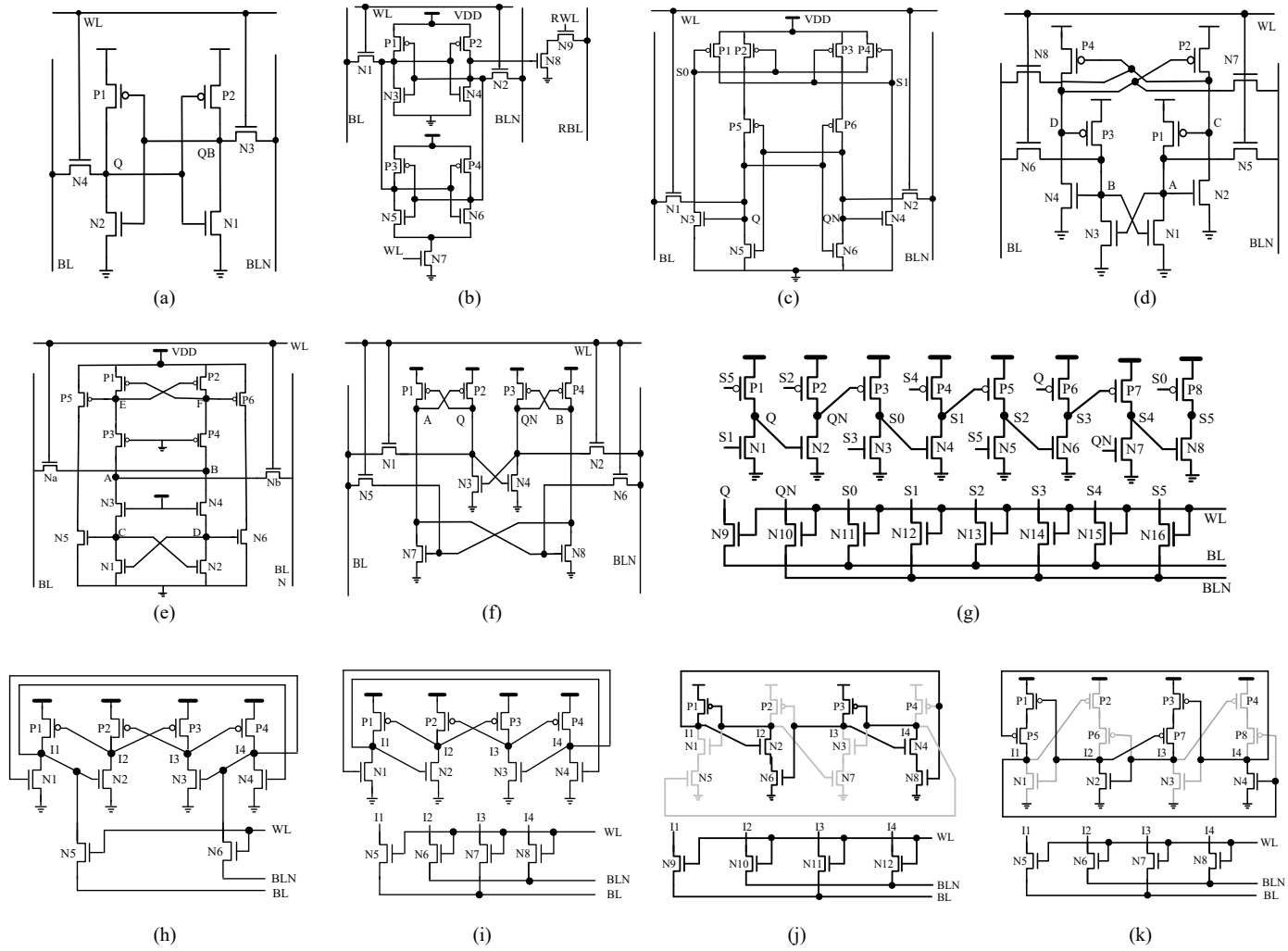

Fig. 1. Schematics of typical existing SRAM cells. (a) 6T. (b) NASA13T [18]. (c) RHD12T [19]. (d) We-Quatro [20]. (e) Zhang14T [21]. (f) QUCCE12T [22]. (g) DNUSRM [23]. (h) QCCM10T [24]. (i) QCCM12T [24]. (j) S4P8N [25]. (k) S8P4N [25].

structure, the QCCM10T cell can provide a high level of protection against SNUs. However, the reading and writing speed of the cell is slow. To improve the access-operation performance, the schematic of the QCCM12T cell [24] has been proposed. It can be seen from Fig. 1-(i) that the storage module of this cell is the same as that of QCCM10T. Therefore, the QCCM12T cell has the same soft-error tolerance ability when compared to the QCCM10T cell. However, only some single nodes can tolerate SNUs and only one pair of nodes can tolerate DNUs for the cells.

To trade-off between reliability and overhead of SRAM cell, the S4P8N cell [25] has been proposed. It can be seen from Fig. 1-(j) that this cell consists of 16 transistors, i.e., PMOS transistors P1 to P4 and NMOS transistors N1 to N12. The storage part of the cell has 4 PMOS transistors and 8 NMOS transistors, i.e., transistors P1 to P4 and N1 to N8. Transistors N9 to N12 are access transistors that are controlled by word line WL. Owing to the elaborately-constructed error-interceptive feedback loops, the S4P8N cell can self-recover from all possible SNUs and a part of DNUs. Moreover, it has low power dissipation since there is no current competition inside (and between) the feedback loops. To reduce read and write access time, the schematic of the S8P4N cell [25] has been proposed. It can be seen from Fig. 1-(k) that the storage part of the S8P4N cell consists of 4 PMOS transistors and 8 NMOS transistors, i.e., transistors P1 to P4 and N1 to N8. The S8P4N cell has the same soft error tolerance capability than the S4P8N cell. However, only four pairs of nodes of the cell are DNU-recoverable.

III. Proposed QCCS SRAM Cell

A. Cell Structure and Behavior

The schematic and layout of the proposed QCCS cell are shown in Fig. 2 and Fig. 3, respectively. The cell has four storage nodes, i.e., I1, I2, I3 and I4. These nodes are connected to the bit lines BL and BLB through pass gates N5 to N8, respectively. These pass gates are controlled by word line WL and will be ON when WL = 1. The stored-1 state for the proposed QCCS cell is taken into consideration for an illustration as shown in Fig. 2. This means that the logic states of nodes I1, I2, I3 and I4 are 1, 0, 1 and 0, respectively. The normal operations of the cell are described as follows.

(1) For the operation of writing 1 to the cell, BL is set to be 1 while BLB is set to be 0 firstly. When WL = 1, the operation of

writing 1 to the cell is executed. At this time, transistors N2, N4, P1 and P3 are ON, and transistors N1, N3, P2 and P4 are OFF. A large feedback loop is constructed (I1 → N2 → I2 → P3 → I3 → N4 → I4 → P1 → I1) at this time. Clearly, the operation of writing 1 is completed and the cell keeps the written value through the feedback loop.

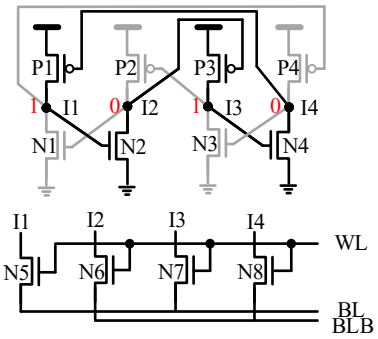

Fig. 2. Schematic of the proposed QCCS cell.

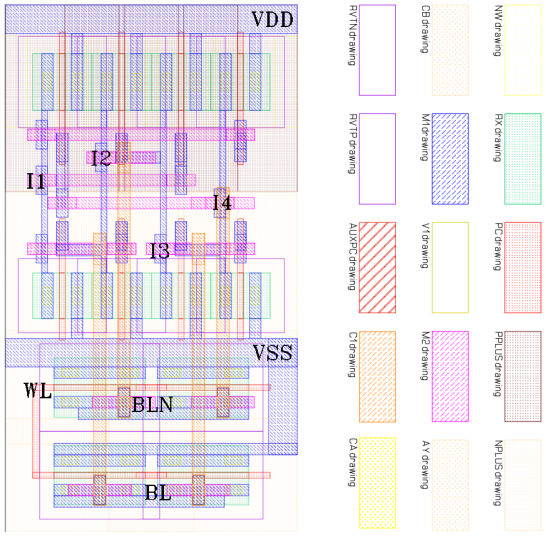

Fig. 3. Layout of the proposed QCCS cell.

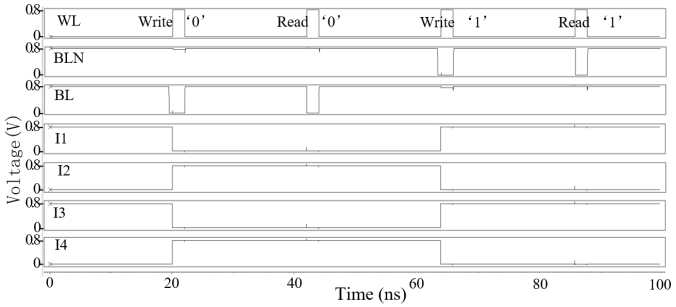

Fig. 4. Simulation results for normal operations of the proposed QCCS cell.

(2) For the operation of reading 1 from the cell, the voltage of both BL and BLB is set to be 1 firstly. The operation of reading 1 from the cell is executed when WL = 1. At this time, the voltage of BL does not change while the voltage of BLB is changed to be 0 because of the discharge operation through N6 and N8. Then, the differential sense amplifier will detect the voltage difference between BL and BLB. For the case of writing/reading 0, the principle is similar as that of writing/reading 1.

(3) For the hold operation, WL is set to be 0. Therefore, the cell keeps holding the stored value at this time through the large feedback loop.

Fig. 4 shows the simulation results of the proposed cell under normal error-free conditions. It can be seen from Fig. 4 that a series of writing/reading 1/0 operations was completed in the cell, and the value was stored in the cell when WL = 0.

B. SNU Recovery Analysis

Assuming that 1 is stored in the cell, i.e., I1 = I3 = 1 and I2 = I4 = 0. First, we describe the case where I1 is affected by an SNU, i.e., I1 is temporarily flipped to 0 from 1. In this case, the SNU is intercepted by N2 since N2 becomes OFF, and thus I2 is not affected (I2=0) and P3 remains ON. Since I3 is not affected (I3=1), N4 remains ON and I4 is 0 (strong 0). Then, P1 remains ON, and I1 can self-recover to 1 from 0. Note that, when I3 is affected by an SNU, i.e., I3 is temporarily flipped to 0 from 1, the similar principle of self-recovery can be observed.

Next, we describe the case where I2 is affected by an SNU. In this case, I2 is temporarily changed to 1 from 0, and hence N1 and P3 are changed to ON and OFF, respectively. I1 has the value 0 (weak 0) since N1 is temporarily changed from OFF to ON. Since I4 is not affected (i.e. I4 = 0), P1 is still ON and I1 has the value 1 (strong 1). However, the strong 1 can neutralize the weak 0 and hence I1 is still correct (I1 = 1). Thus, N2 is ON since I1 has the value 1. Note that P2 is still OFF since I3 is not affected. Therefore, I2 can self-recover from the SNU. When I4 is affected by an SNU, the similar principle of self-recovery can be observed.

Fig. 5 shows the simulation results for SNU self-recovery on nodes I1 to I4 of the proposed QCCS cell. An SNU was respectively injected to nodes I1 and I3 between 0 and 100 ns. Between 300 and 450 ns, an SNU was respectively injected to nodes I2 and I4. It can be seen from Fig. 5 that the proposed cell can self-recover from SNUs. Note that the QCCS cell is not DNU hardened, so that we propose the DNU hardened SCCS cell in the next section.

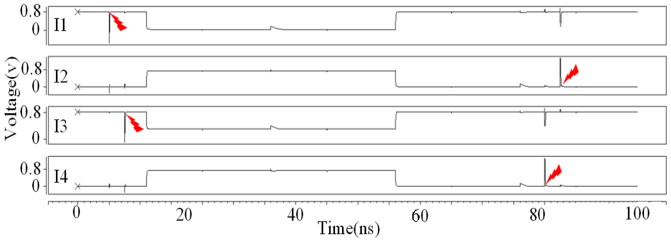

Fig. 5. Simulation results for SNU self-recovery of the proposed QCCS cell

IV. Proposed SCCS SRAM Cell

A. Schematic and Normal Operations

Fig. 6 and 7 show the schematic and layout of the proposed SCCS cell, respectively. The SCCS cell consists of 18 transistors, including PMOS transistors P1 to P6 and NMOS transistors N1 to N12. Transistors P1 to P6 and N1 to N6 are used for value-retention. Transistors N7 to N12 are used for access operations and their gates are connected to word-line

WL. BL and BLN are bit-lines, and they are connected to the internal nodes I1 to I6. When WL = 1, the access transistors are ON, allowing write/read access operations to be executed. When WL = 0, the cell keeps the stored value.

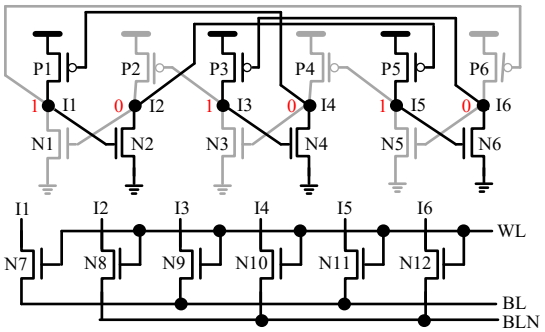

Fig. 6. Schematic of the proposed SCCS cell.

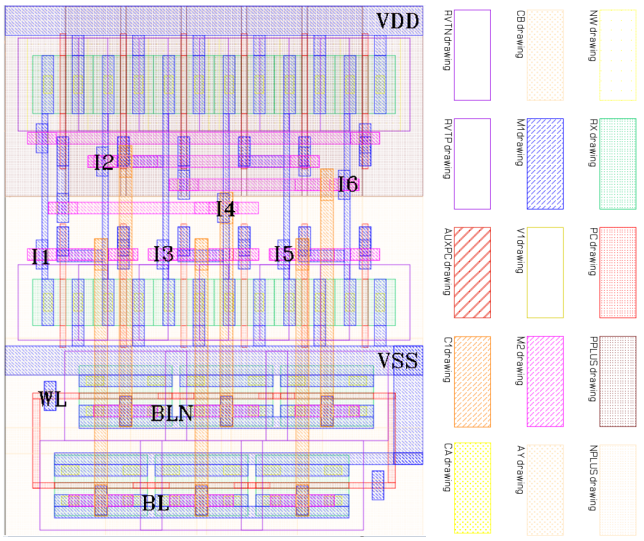

Fig. 7. Layout of the proposed SCCS cell.

Let us describe the normal operations of the proposed SCCS cell. Fig. 6 shows the scenario when the cell stores 1, i.e., I1 = I3 = I5 = 1 and I2 = I4 = I6 = 0. First, we consider the case of writing 1. Before the write operation, BL = 1 and BLN = 0 are set. When WL = 1, the operation of writing 1 to the cell is executed. At this time, transistors N1, N3, N5, P2, P4, and P6 are OFF and transistors P1, P3, P5, N2, N4, and N6 are ON. Thus, a large feedback loop (I1 → I2 → I5 → I6 → I3 → I4 → I1) is constructed in the cell. Clearly, the operation of writing 1 is completed and the cell keeps the writing value through the feedback loop. Next, we consider the case of reading the stored 1. Before the read operation, the voltages of BL and BLN are set to logic 1. When WL = 1, the operation of reading 1 from the cell is executed. At this time, the voltage of BL does not change. However, the voltage of BLN decreases because of its discharge operation through N8, N10, and N12. Once the differential sense amplifier detects that the voltage difference between BL and BLN is a specified constant value, the read operation is finished and the cell outputs the stored value. For the operation of writing/reading 0, the similar principle can be observed.

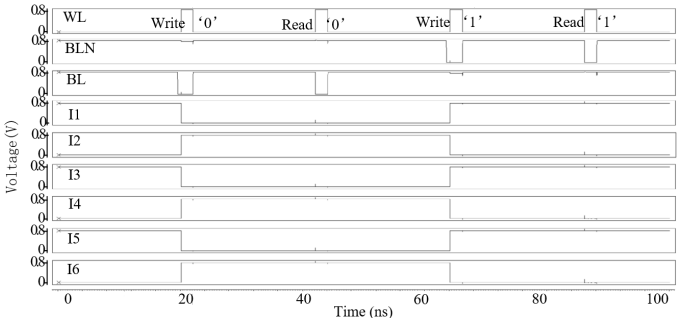

Fig. 8. Simulation results for normal operations of the proposed SCCS cell.

Fig. 8 shows the simulation results for normal operations of the proposed SCCS cell. From Fig. 8 we can see that a series of "write 0, read 0, write 1, and read 1" operations were correctly executed and these written values were correctly kept in the proposed cell.

Regarding fault-tolerance of the proposed SCCS cell, here we use the case of 1 being stored (i.e., I1 = I3 = I5 = 1 and I2 = I4 = I6 = 0) for illustrative purpose. First, we discuss the SNU self-recovery principles of the SCCS cell. The key single nodes are only I1 and I2 due to the symmetric structure of the proposed cell.

B. SNU Self-Recovery Principles

We first describe the case where I1 is affected by an SNU, i.e., I1 is temporarily flipped to 0 from 1. In this case, the SNU is intercepted by N2 since N2 becomes OFF. Thus, I2 is not affected (I2 = 0) and P5 remains ON. Since I5 is also not affected (I5 = 1), N6 remains ON and I6 holds a 0 (strong 0). Meanwhile, the fact that I1 temporarily flips to 0 from 1 can cause P6 to be ON temporarily and I6 holds a 1 (weak 1). However, the strong 0 of I6 can neutralize this weak 1, and hence I6 remains correct (I6 = 0). Thus, P3 remains ON (I3 = 1) and N4 remains ON (I4 = 0), allowing P1 to be still ON (I1 = 1). Clearly, I1 can self-recover from the SNU.

Next, we describe the case where I2 is affected by an SNU, i.e., I2 is temporarily flipped to 1 from 0. In this case, the SNU is intercepted by P5 since P5 becomes OFF. Thus, I5 is not affected (I5 = 1) and N6 remains ON (I6 = 0). Meanwhile, the fact that I2 temporarily flips to 1 from 0 can cause N1 to become ON temporarily. In this case, I1 holds a temporary undetermined value, especially when the striking-particle has a large energy, since the unaffected I4 can allow P1 to be ON. However, at this time, since P6 cannot be ON, I6 still has its correct value (I6 = 0). Thus, P3 remains ON and I3 is also not affected (I3 = 1). Then, N4 remains ON and I4 is also not affected (I4 = 0). Thus, P1 remains ON and I1 outputs 1 (strong 1). However, the strong 1 of I1 can neutralize the weak 0 of I1 induced by the temporary ON of N1. In other words, I1 can self-recover to its previous value (I1 = 1). Thus, N2 can be still ON, and clearly, I2 can self-recover from the SNU. As for any other single-node, the similar SNU self-recovery principles can be observed. In summary, the proposed cell can self-recover from SNUs.

Fig. 9 shows the simulation results for SNU self-recovery on nodes I1 to I6 of the proposed SCCS cell. Between 0 and 100 ns, an SNU was respectively injected to nodes I1, I3, and I5.

Between 300 and 450 ns, an SNU was respectively injected to nodes I2, I4, and I6. It can be seen from Fig. 9 that the proposed cell can self-recover from SNUs.

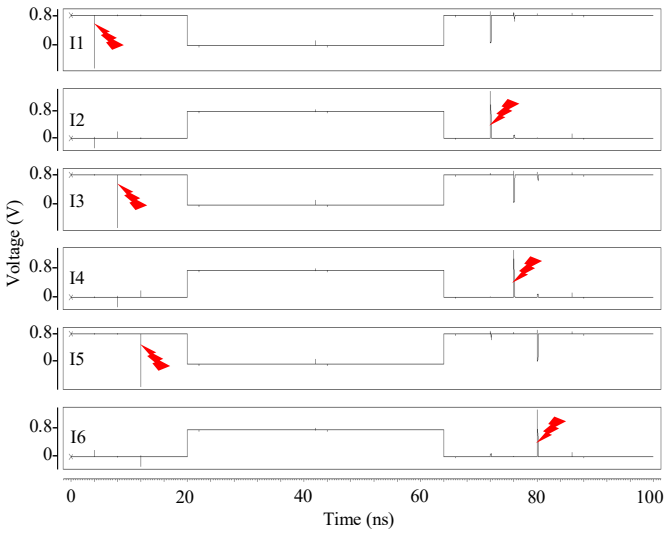

Fig. 9. Simulation results for SNU self-recovery of the proposed SCCS cell.

C. DNU Tolerance Principles

Let us now describe the various cases of DNU tolerance. Due to the symmetric structure of the cell, the node-pairs in any following group are identical.

Group 1: {<I1, I2>, <I3, I4>, and <I5, I6>};
Group 2: {<I2, I3>, <I4, I5>, and <I6, I1>};
Group 3: {<I1, I3>, <I3, I5>, and <I5, I1>};
Group 4: {<I2, I4>, <I4, I6>, and <I6, I2>};
Group 5: {<I1, I4>, <I3, I6>, and <I5, I2>};
Group 6: {<I2, I5>, <I4, I1>, and <I6, I3>}.

In fact, group 6 is identical to group 5, so group 6 is omitted.

Note that, <I1, I5>, <I1, I6> and their identical node-pairs are also considered in the above pair groups. Thus, the key node-pairs are only <I1, I2 >, <I2, I3>, <I1, I3>, <I2, I4>, and <I1, I4>. The DNU tolerance principles of the proposed cell are described in the following.

Case 1**:** <I1, I2> suffers from a DNU.

In this case, I1 is temporarily flipped to 0 from 1 and I2 is temporarily flipped to 1 from 0. Thus, P5 becomes temporarily OFF and P6 becomes temporarily ON. However, I5 is not directly affected (I5 = 1). Thus, I6 holds a 0. Meanwhile, the fact that I1 is temporarily flipped to 0 can allow P6 to be temporarily ON and I6 outputs 1. As a result, I6 becomes temporarily undetermined and N5 cannot become ON. At this time, I5 = 1 cannot affect P4, I4 = 0 cannot affect N3, and I3 = 1 cannot affect P2. Meanwhile, I4 = 0 can allow P1 to remain ON and I1 outputs 1 (strong 1). As a result, the strong 1 of I1 can neutralize the DNU-induced weak 0 of I1. Thus, I1 remains correct (I1 = 1), P6 becomes OFF, and I6 self-recovers to 0. Meanwhile, N2 can be still ON to output 0 (strong 0). As a result, the strong 0 of I2 can neutralize the DNU-induced weak 1 of I2. Thus, I2 = 0, N1 becomes OFF, and P5 becomes ON. Finally, all nodes and transistors can self-recover to their original states. In other words, <I1, I2> of the proposed cell can self-recover from the DNU.

Case 2**:** <I2, I3> suffers from a DNU.

In this case, I2 is temporarily flipped to 1 from 0 and I3 is temporarily flipped to 0 from 1. Thus, P2 becomes temporarily ON. Since I1 = 1 is not directly affected, N2 remains ON. As a result, I2 cannot be determined. However, I2 is temporarily flipped to 1 due to the DNU. Thus, N1 becomes temporarily ON. Meanwhile, I4 is not directly affected (I4 = 1). Thus, P1 remains ON. As a result, I1 cannot be determined and P6 cannot become ON. At this time, I6 = 0 cannot affect N5, I5 = 1 cannot affect P4, and I4 = 0 cannot affect N3. However, I6 = 0 can allow P3 to be still ON and I3 outputs 1 (strong 1). As a result, the strong 1 of I3 can neutralize the DNU-induced weak 0 of I3. Thus, I3 remains correct (I3 = 1) and P2 becomes OFF. Meanwhile, I4 = 0 can allow P1 to remain ON, and I1 outputs 1 (strong 1). As a result, the strong 1 of I1 can neutralize the DNU-induced weak 0 of I1. Thus, I1 remains correct (I1 = 1) and N2 remains ON to output 0 (strong 0). As a result, the strong 0 of I2 can neutralize the DNU-induced weak 1 of I2. Thus, I2 = 0, N1 becomes OFF, and P5 becomes ON. Finally, all nodes and transistors can self-recover to their original states. In other words, <I2, I3> of the proposed cell can self-recover from the DNU.

Case 3**:** <I1, I3> suffers from a DNU.

In this case, both I1 and I3 are temporarily flipped to 0 from 1. Thus, P2 becomes temporarily ON and N2 becomes temporarily OFF. Then, I2 temporarily holds a 1 and N1 becomes temporarily ON. Since I4 = 0 is not directly affected, P1 is ON. As a result, I1 cannot be determined and P6 cannot become ON. At this time, I6 = 0 cannot affect N5, I5 = 1 cannot affect P4, and I4 = 0 cannot affect N3. However, I6 = 0 can allow P3 to be still ON and I3 outputs 1 (strong 1). As a result, the strong 1 of I3 can neutralize the DNU-induced weak 0 of I3. Thus, I3 remains correct (I3 = 1) and P2 becomes OFF. Meanwhile, I4 = 0 can allow P1 to remain ON and I1 outputs 1 (strong 1). As a result, the strong 1 of I1 can neutralize the DNU-induced weak 0 of I1. Thus, I1 remains correct (I1 = 1) and N2 remains ON to output 0 (I2 = 0). Finally, all nodes and transistors can self-recover to their original states. In other words, <I1, I3> of the proposed cell can self-recover from the DNU.

Case 4**:** <I2, I4> suffers from a DNU.

In this case, both I2 and I4 are flipped to 1 from 0. Thus, N1 and N3 become ON and P1 and P5 become OFF. Thus, I1 will get an invalid value (I1 = 0) and P6 becomes ON. Since I5 = 1 is not directly affected, N6 remains ON. As a result, I6 cannot be determined, making both P3 and N5 to become OFF. The fact that both P5 and N5 are OFF can lead to an undetermined value on I5 as time passes. Thus, N6 cannot become ON. Since P6 is ON as mentioned above, I6 will get an invalid value (I6 = 1) and N5 becomes ON. Meanwhile, since P5 is OFF as mentioned above, I5 will get an invalid value (I5 = 0). Since N3 is ON and P3 is OFF as mentioned above, I3 will get an invalid value (I3 = 0). Finally, all nodes and transistors cannot self-recover to their original states. In other words, the proposed cell cannot tolerate the DNU on <I2, I4>. However, the nodes in the pair are not adjacent. Hence, the occurrence of

this DNU is less likely to happen when considering the layout of the cell.

***Case 5*:** <I1, I4> suffers from a DNU.

This case is similar to Case 4, so finally, all nodes and transistors cannot self-recover to their original states. In other words, the proposed cell cannot tolerate the DNU on <I1, I4>. However, the nodes in the pair are not adjacent. Hence the proposed cell can avoid the occurrence of this DNU owing to layout consideration.

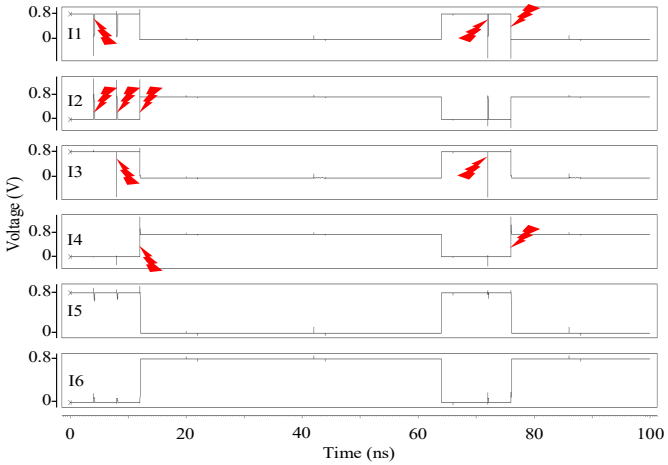

Fig. 10. Simulation results for DNUs of the proposed SCCS cell.

Fig. 10 shows the simulation results for DNUs of the proposed SCCS cell. At 20 ns, 40 ns, and 60 ns, a DNU was respectively injected to node-pairs <I1, I2>, <I2, I3>, and <I2, I4>. At 360 ns and 380 ns, a DNU was respectively injected to node-pairs <I1, I3> and <I1, I4>. It can be seen from Fig. 10 that node pairs <I1, I2>, <I2, I3>, and <I1, I3> of the proposed cell can self-recover from DNUs. Node pairs <I2, I4> and <I1, I4> of the proposed cell cannot self-recover from DNUs. However, the nodes in any of the not-self-recoverable DNU-pairs are not adjacent. Hence, the proposed cell can avoid the occurrence of this kind of DNUs owing to layout consideration. In summary, the proposed cell can tolerate DNUs.

In the above-mentioned fault-injection scenarios, a popular and flexible double-exponential current-source model was used [31]. The time constant of the rise and fall of the current pulse was set to be 0.1 and 3.0 ps, respectively. In all simulations, the Synopsys HSPICE tool was used with a 22 nm CMOS library from GlobalFoundries under room temperature and a supply voltage of 0.8V.

V. Comparison and Evaluation Results

In order to quantify the various overhead of the proposed SCCS and QCCS cell and make a fair comparison with the state-of-the-art SRAM cells described in Section II, the same simulation conditions described in the above section were used for all simulations. The reliability and overhead comparison results among the unhardened/hardened SRAM cells in terms of SNU recoverability (*SNUR*), number of DNU Hardened node-Pairs (*#DHP*), read access time (*RAT*), write access time (*WAT*), average power dissipation (dynamic and static), silicon area measured as in [31] and sensitive cross-section area measured as in [35] are shown in Table I.

Let us describe the reliability comparison. It can be seen from Table I that the DNUSRM, S4P8N, S8P4N, QCCS and SCCS cells can provide complete SNU self-recoverability from all possible SNUs, while the other cells cannot provide complete SNU self-recoverability since any of them has at least one node that cannot self-recover from an SNU. Regarding DHP, the 6T, NASA13T, Zhang14T, and QUCCE12T cells have no DHP, the RHD12T, We-Quatro, QCCM10T, and QCCM12T cells have one DHP, and the S4P8N and S8P4N cells have 4 DHPs. However, the DNUSRM cell has 16 DHPs because it has many redundant nodes. It is clear that, except the DNUSRM cell, only the proposed SCCS cell has the maximum number of DHPs, which is 9. In summary, the proposed SCCS cell can provide much better reliability than the other cells except DNUSRM that has very large power and area.

Let us now describe the qualitative overhead comparison. Regarding WATs and RATs, it can be seen from Table I that the 6T cell has the smallest WAT. This is mainly because the cell has less current competition when writing a value. Similarly, the WAT of the QCCS is also small. Conversely, the QCCM10T has the largest WAT due to more current competition when writing a value. It can be seen from Table I that the proposed cells have a comparable WAT compared with most of the other hardened cells. However, the proposed SCCS cell has the smallest RAT except the DNUSRM cell due to the use of 6 parallel access transistors for reading a value. The NASA13T has the largest RAT due to its special read operation (it has specific extra read transistors). The intrinsic charge/discharge of cell nodes through access transistors can affect WATs and RATs.

Regarding power and area, it can be seen from Table I that the 6T cell has the smallest power and area due to the use of a total of only 6 transistors. Generally, a cell having few transistors requires a smaller area and consumes less power; a cell having a larger area consumes more power. The proposed SCCS cell has to use extra transistors/area to provide the self-recoverability from all possible SNUs and one part of DNUs as well as optimized RAT and WAT. Thus, the cell has large power dissipation as well. However, the DNUSRM has the largest power consumption, mainly due to the large current competition in its feedback loops and the use of extra access transistors. The RHD12T, We-Quatro, QUCCE12T, and QCCM12T have a similar area and power dissipation mainly due to their identical amount of used transistors and similar cell constructions. Therefore, the high reliability and optimized access operations of the proposed SCCS cell are mainly achieved at the cost of indispensable silicon area and power dissipation compared with the other hardened SRAM cells. However, the proposed QCCS cell consumes less WAT, power and area due to less current competition and fewer used transistors compared with the proposed SCCS cell. Note that the sensitive cross-section area of a cell is large if the silicon area of the cell is large.

$$PRC_{WAT}(i) = \frac{WAT_{\text{compared}}(i) - WAT_{\text{proposed}}}{WAT_{\text{compared}}(i)} \times 100\% \quad (1)$$

$$PRC_{WAT}^{\text{average}} = \frac{1}{n}\sum_{i=1}^{n} PRC_{WAT}(i) \quad (2)$$

Let us describe the quantitative overhead comparison. The percentages of reduced costs (PRCs) of the proposed QCCS and SCCS cells compared with the other cells were calculated. The PRC of the WAT was calculated with Eq. (1), where $WAT_{compared}(i)$ means the WAT of the *i*-th compared SRAM cell and $WAT_{proposed}$ means the WAT of the proposed SCCS or QCCS SRAM cell, respectively. Similarly, the PRCs of the RAT, power dissipation, and silicon area can be calculated. The average PRCs were calculated with Eq. (2), where *n* is the count of compared SRAM cells. However, for brevity, only the average PRCs are discussed. Compared with the SNU/DNU hardened cells, the proposed QCCS cell can achieve 17% RAT and 19% WAT reduction, at a cost of 4% power dissipation and 10% silicon area overhead on average; the proposed SCCS cell achieves an approximate 44% RAT as well as 13% WAT reduction at the cost of indispensable power dissipation as well as silicon area.

The *process, voltage and temperature* (*PVT*) variation can significantly impact the performance of IC designs, especially for storage cells, such as latches and SRAMs [8, 31, 33]. The estimation results of PVT variation impacts on RAT, WAT, and power are shown in Fig. 11. In our simulations, the normal temperature was set to 25℃ and the temperature ranged from -25℃ to 125℃. The normal supply voltage was set to 0.8V and the supply voltage variation ranged from 0.65V to 0.95V. The threshold-voltage increment ranged from 0.01V to 0.06V.

It can be seen from Fig. 11-(a), (b), and (c) that the SRAM cells generally need to consume more RAT, WAT, and power when the temperature rises. This is mainly due to the decrease of carrier mobility when the temperature rises [8]. It can be seen from Fig. 11-(a) that the temperature variation has the largest impact on the RAT of the NASA13T cell, mainly due to its more decreased carrier mobility when the temperature rises. However, the temperature variation has a low impact on the RAT of the other SRAM cells, such as the DNUSRM, the proposed QCCS, the proposed SCCS, and the S8P4N. It can be seen from Fig. 11-(b) that the temperature variation has the largest impact on the WAT of the Zhang14T cell, mainly due to the increment of WAT when the temperature rises. However, the temperature variation has a low impact on the WAT of the cells, such as the NASA13T and the QUCCE12T. It can be seen from Fig. 11-(c) that the temperature variation has a low impact on the power of the cells, such as the 6T, the S4P8N, the Zhang14T, and the NASA13T, but has a large impact on the DNUSRM cell mainly due to the extra employed area to provide high reliability.

It can be seen from Fig. 11-(d), (e) and (f) that the SRAM cells need to consume decreasing RAT, WAT, and increasing power in general when the supply voltage rises. Indeed, large supply voltage can reduce access time of transistors but can increase power dissipation in general [8]. It can be seen from Fig. 11-(d) that the supply voltage variation has the largest impact on the RAT of the Zhang14T cell, mainly since it employs many devices from its storage nodes to its output. However, the supply voltage variation has a low impact on the RAT of the other SRAM cells, such as the DNUSRM, the proposed QCCS, the proposed SCCS and the S8P4N since any of them uses more access transistors. It can be seen from Fig. 11-(e) that the supply voltage variation has the largest impact on the WAT of the QCCM10T, mainly since it employs many devices from its storage node to its output. However, the supply voltage variation has a low impact on the WAT of the other SRAM cells, such as the proposed QCCS, the proposed SCCS,

TABLE I
RELIABILITY AND OVERHEAD COMPARISON RESULTS AMONG THE UNHARDENED AND HARDENED SRAMS.

	Ref.	SNUR	#DHP	RAT (ps)	WAT (ps)	Power (nW)	$10^{-3}\times$ Area (nm^2)	$10^{-4}\times$ Sensitive Area (nm^2)	PRC (%)			
									RAT	WAT	Power	Area
6T	-	×	0	25.88	3.65	5.24	4.35	-	-	-	-	-
NASA13T	[18]	×	0	128.67	16.39	18.92	9.70	3.77	93.19	72.54	17.44	-34.74
RHBD12T	[19]	×	1	25.72	5.06	10.38	8.27	3.11	65.98	11.07	-50.48	-58.04
We-Quatro	[20]	×	1	12.99	4.38	10.43	8.71	3.67	32.64	-2.74	-49.76	-50.06
Zhang14T	[21]	×	0	50.66	3.80	7.78	10.25	3.99	82.73	-18.42	-52.39	-27.51
QUCCE12T	[22]	×	0	13.02	4.31	10.43	8.71	3.68	32.80	-4.41	-49.76	-50.06
DNUSRM	[23]	√	16	6.63	4.71	20.86	17.42	8.20	-31.98	4.46	25.12	24.97
QCCM10T	[24]	×	1	18.20	23.21	11.45	7.79	3.39	51.92	80.61	-36.42	-67.78
QCCM12T	[24]	×	1	12.99	4.22	10.43	8.71	3.78	32.64	-6.64	-49.76	-50.06
S4P8N	[25]	√	4	17.93	5.19	8.55	12.67	5.08	51.20	13.29	-82.69	-3.16
S8P4N	[25]	√	4	12.94	3.67	9.26	10.65	4.27	32.38	-22.62	-68.68	-22.72
SCCS	Proposed	√	9	8.75	4.50	15.62	13.07	5.09	44.35	12.71	-39.74	-33.92
QCCS	Proposed	√	0	13.04	4.17	10.43	8.71	3.28	16.66	19.12	3.56	10.23

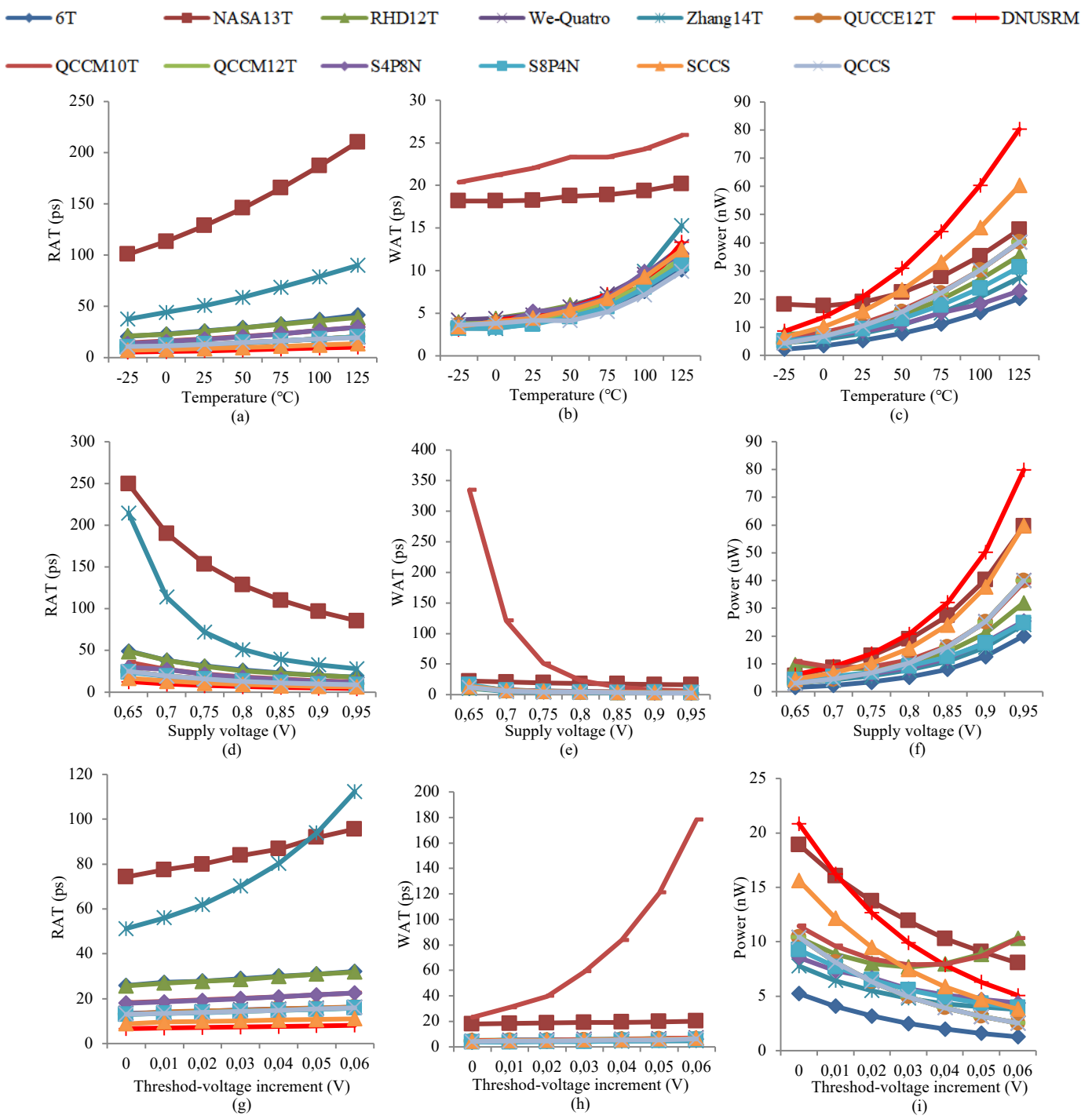

Fig. 11. Estimation results of PVT variation impacts on RAT, WAT, and power for the SRAM designs. (a) Impacts of temperature variations on RAT. (b) Impacts of temperature variations on WAT. (c) Impacts of temperature variations on power. (d) Impacts of supply voltage variations on RAT. (e) Impacts of supply voltage variations on WAT. (f) Impacts of supply voltage variations on power. (g) Impacts of threshold-voltage variations on RAT. (h) Impacts of threshold-voltage variations on WAT. (i) Impacts of threshold-voltage variations on power.

the NASA13T, and the 6T. It can be seen from Fig. 11-(f) that the supply voltage variation has a low impact on the power of the SRAM cells, such as the 6T, the S8P4N, and the S8P4N, but has a large impact on the DNUSRM cell, mainly due to the indispensable employed area to provide high reliability.

It can be seen from Fig. 11-(g), (h) and (i) that the SRAM cells need to consume increasing access time and decreasing power in general when the threshold voltage rises. Indeed, a large threshold voltage can increase the access time of transistors but can decrease power dissipation in general [8]. It can be seen from Fig. 11-(g) that the threshold voltage variation has the largest impact on the RAT of the Zhang14T, mainly since it employs many devices from its storage nodes to its output. However, the threshold voltage variation has a low impact on the RAT of the other SRAM cells, such as the DNUSRM, the proposed QCCS, the proposed SCCS and the S8P4N since any of them uses more access transistors. It can be seen from Fig. 11-(h) that the threshold voltage variation has a

large impact on the WAT of the QCCM10T. It can be seen from Fig. 11-(h) that the threshold voltage variation has a large impact on the WAT of the QCCM10T, mainly since they employ many devices from their storage nodes to their outputs. However, the threshold voltage variation has a low impact on the WAT of the other SRAM cells, such as the S4P8N, the S8P4N, the proposed QCCS and the proposed SCCS. It can be seen from Fig. 11-(i) that the threshold voltage variation has a low impact on the power of the SRAM cells, such as the 6T, S8P4N, and the Zhang14T, but has a large impact on the DNUSRM cell mainly due to the indispensable employed area to provide high reliability.

As the channel length, oxide thickness, and channel width are variable parameters of the transistor, and they may change during fabrication. The MC Simulation result gives the mean (μ) and standard deviation (σ) of output parameters. Based on the variation in output, the designer can decide to change the design. Foundry companies provide a model file for MC Simulation to know the fluctuation in output [35-36]. The μ and σ comparison of power loss and stability for SRAM cells are reported in Table II. Also, to check the process, voltage, and temperature (PVT) variations on SNU and DNU of bit-cells, the MC simulation has been performed. Truncated Gaussian variation is applied to the widths, lengths, and threshold voltages of all-transistor with $\pm 3\sigma$ variation to perform 5000 MC simulations [35]. Meanwhile, the probability of SNU occurrence (P_S) of the cells is calculated as the ratio of the sensitive area of a cell to the total area of the cell [36]. The smaller is P_S, the lesser is the probability of an SRAM being affected by an SNU. P_S of all the considered cells is presented in Table III. Furthermore, the robustness of SNU/DNU recovery is assessed by evaluating the probability of logical flipping (P_{LF}). It is calculated as the ratio of simulations fail to recover to the total number of simulations (5000) [35]. The P_{LF} comparison of considered cells is reported in Table III. Table III shows that PVT fluctuations do not affect the DNUSRM cell's SNU/DNU recovery, while similar variations cause failure in other cells. To evaluate the impact of gate length and threshold voltage V_{th} change on Q_c, a simple empirical model from Ref. [35] is used. The time effectiveness of the model makes it suitable for circuit-level design exploration and tool implementation. We analyze the impact of variation on Q_c variability caused by different 3σ gate length and threshold voltage variations. For 4%, 8%, and 12% of 3σ variation of V_{th}, the 3σ variation of Q_c are 5.1%, 3.7%, and 2.1%, respectively. Similarly, for 5%, 10%, and 15% of 3σ variation of L_{gate}, the 3σ variation of Q_c are 7.1%, 5.2%, and 4.4% respectively.

Moreover, in the circuit simulation-based model, the expected SER (FIT/Mbit) for CMOS SRAM circuits are calculated in (4) combined with (3), as in [35-36]. The empirical equation (not physically-based) to estimate SER by terrestrial neutrons is expressed in (4), where *F, K,* and *A* are neutron flux in the terrestrial region (0.00565 particles/cm^2-s), proportionality constant value (0.1952 FIT-s/b-n), and total drain area are connected to sensitive node (cm^2), respectively [35]. The *Qc* and *Qs* are critical charge and charge collection efficiency [36]. The estimated SER comparison in FIT/Mbit of SRAM cells using (4) and technology parameters [36] is shown in Table III. As for SER, the proposed SCCS SRAM cell is 2.9×, 1.4×, 2.4×, 1.4×, 2.6×, 2.8×, 2.8×, 1.1×, and 1.1× better than NASA13T, RHBD12T, We-Quatro, Zhang14T, QUCCE12T, QCCM10T, QCCM12T, S4P8N, and S8P4N SRAM cells respectively based on circuit-level simulations. The proposed SRAM cells have a better SER than most of the other SRAM cells due to higher critical charge.

$$Q_c = C_{node} \times VDD + I_{P,ON} \times W_{pulse} \quad (3)$$

$$SER = F \times K \times A \times exp^{(-Qc/Qs)} \quad (4)$$

It is reported in [27] that *static noise margin* (*SNM*) is an

TABLE II
PARAMETERS DISTRIBUTION USING 5000 MC SIMULATION OF THE CELLS

SRAMs	HSNM			RSNM			WSNM			Total Power		
	μ (mV)	σ (mV)	σ/μ	μ (mV)	σ (mV)	σ/μ	μ (mV)	σ (mV)	σ/μ	μ (nW)	σ (nW)	σ/μ
6T	198	32.6	0.16	167	24.3	0.15	303	27.9	0.09	6.13	0.93	0.15
NASA13T [18]	205	30.5	0.15	185	29.6	0.16	267	30.9	0.12	17.45	2.08	0.12
RHBD12T [19]	242	40.2	0.17	198	33.1	0.17	368	59.9	0.16	9.94	1.47	0.15
We-Quatro [20]	230	37.5	0.16	176	29.6	0.17	279	45.8	0.16	11.04	1.85	0.17
Zhang14T [21]	145	29.4	0.20	173	25.4	0.15	376	39.4	0.10	7.44	1.64	0.22
QUCCE12T [22]	195	32.2	0.17	188	31.8	0.17	306	49.5	0.16	10.57	1.81	0.17
DNUSRM [23]	238	39.8	0.17	155	25.1	0.16	423	69.2	0.16	19.03	1.71	0.09
QCCM10T [24]	184	27.3	0.15	175	28.2	0.16	275	39.6	0.14	10.98	1.45	0.13
QCCM12T [24]	193	29.5	0.15	177	26.6	0.15	279	33.7	0.12	9.56	1.33	0.14
S4P8N [25]	219	31.8	0.15	180	29.6	0.16	412	40.1	0.10	8.55	1.29	0.15
S8P4N [25]	206	32.5	0.16	179	28.3	0.16	368	38.6	0.10	9.50	1.46	0.15
SCCS-Proposed	244	35.6	0.15	184	30.1	0.16	389	55.9	0.14	14.84	1.81	0.12
QCCS-Proposed	240	39.1	0.16	187	29.8	0.16	354	50.3	0.14	10.66	1.62	0.15

important metric to analyze the stability of SRAM cells for normal operations. Fig. 12 shows the comparison results of SNMs for different SRAM cells under the supply voltage of 0.8V. Note that, the normal temperature was set to 25℃. It can be seen from Fig. 12 that the *hold SNM* (*HSNM*) value of the proposed QCCS and SCCS cells are the highest except for that of the QCCM10T and QCCM12T cell. It can be seen that the *read SNM* (*RSNM*) value of the proposed QCCS and SCCS cells are higher than those of the hardened RHBD12T, Zhang14T, QUCCE12T, QCCM10T, S8P4N and S4P8N cells, but lower than those of the QCCM12T and We-Quatro cells. It can also be seen that the *write SNM* (*WSNM*) value of the proposed QCCS and SCCS cells are higher than those of most hardened cells, but lower than those of the DNUCCE12T and S8P4N cells. In summary, the comparison results of the SNMs show that the proposed QCCS and SCCS cells have moderate SNMs compared with the state-of-the-art hardened SRAM cells.

TABLE III
DETAILED RELIABILITY AND STABILITY COMPARISONS AMONG THE HARDENED SRAMS.

SRAM	SNU *Qc* (fC)	SER (FIT/Mbit)	DM (mV)	WM (mV)	P_S	P_{LF}
NASA13T [18]	13.9	411.7	125	134	0.042	98.4
RHBD12T [19]	41.6	259.5	144	163	0.037	51.6
We-Quatro [20]	14.9	364.7	134	161	0.041	91.7
Zhang14T [21]	40.1	256.3	113	190	0.044	47.8
QUCCE12T [22]	15.0	383.7	145	151	0.039	93.2
DNUSRM [23]	63.8	101.9	105	149	0.057	0.0
QCCM10T [24]	14.3	401.8	131	164	0.039	95.9
QCCM12T [24]	14.3	401.8	135	184	0.041	95.9
S4P8N [25]	38.9	219.5	138	172	0.044	44.3
S8P4N [25]	38.2	220.8	129	177	0.041	45.9
SCCS-Proposed	54.1	106.4	143	178	0.044	22.5
QCCS-Proposed	44.6	195.7	147	182	0.038	30.6

Fig. 13 shows the comparison results of SNMs under different supply voltages. Note that, the normal supply voltage was set to 0.8V and the supply voltage variation was ranged from 0.6V to 1.3V. The normal temperature was still set to 25℃. Fig. 13-(a), (b), and (c) show the impact of supply voltage variations on HSNM, RSNM, and WSNM. It can be seen that, as the supply voltage increases, the value of HSNM generally increases, the value of RSNM generally decreases, and the value of WSNM keeps on increasing. It can be seen from Fig. 13-(a) that, as the supply voltage increases, the proposed QCCS and SCCS cells have a similar HSNM sensitivity compared to the RHBD12T and QUCCE12T cells, and they have a comparatively low HSNM sensitivity. It can be seen from Fig. 13-(b) that, as the supply voltage increases, the proposed QCCS and SCCS cell have a similar RSNM sensitivity compared to the QUCCE12T cell, and the proposed QCCS and SCCS cells have a lower RSNM sensitivity than the DNUSRM, QCCM10T and S8P4N cells. It can be seen from Fig. 13-(c) that, as the supply voltage increases, the proposed SCCS cell has a similar WSNM sensitivity compared to the S4P8N, RHD12T and QCCM10T cells, and the proposed SCCS cell has a lower RSNM sensitivity than the QCCM12T and S8P4N cells.

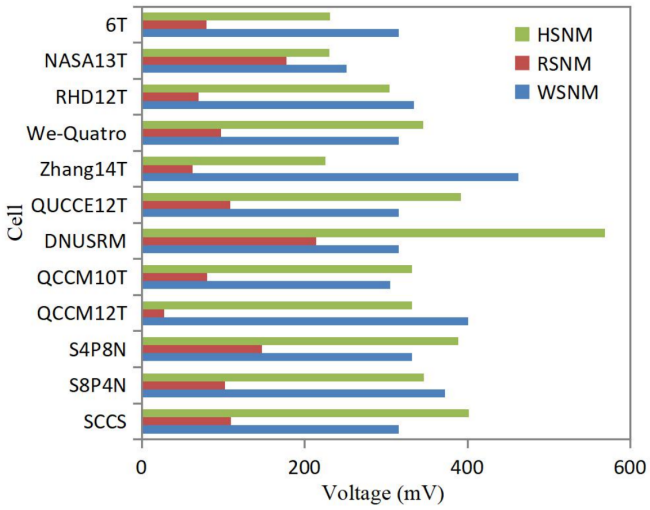

Fig. 12. SNM comparison under the supply voltage of 0.8V.

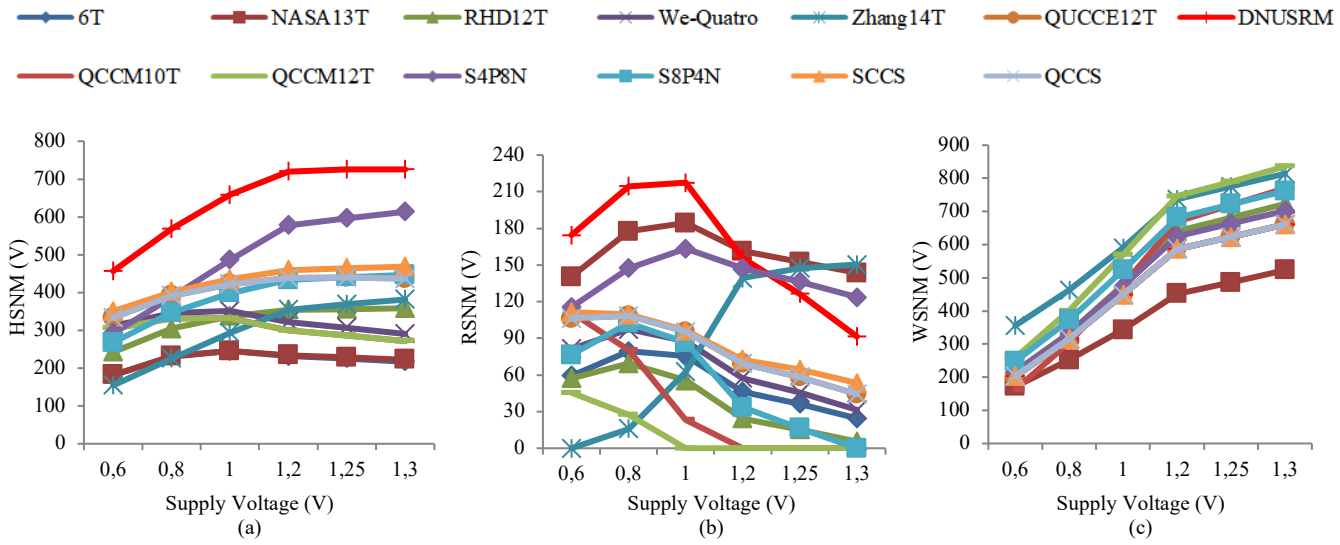

Fig. 13. SNM comparisons under different supply voltage. (a) HSNM. (b) RSNM. (c) WSNM.

Moreover, using the method in [35], the normalized power performance area (PPA) comparison for 4×4 bit cells array and for macro operation (width of WL 0.4ns) is calculated and Fig. 14 shows the comparison results. It can be seen that the proposed SRAMs have moderate PPAs. We also considered connection for WL/BL/BLN in a bitcell array for the proposed SRAMs. We use the tree structure to ensure data drive and consistence.

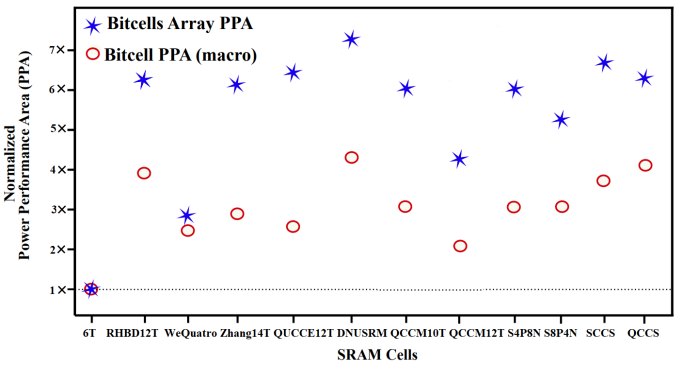

Fig. 14. PPA comparison of alternative SRAMs.

VI. Conclusion and Further Work

The aggressive CMOS technology scaling increases the sensitivity of SRAMs to soft errors, such as SNUs and DNUs. Based on the RHBD approach, two novel SRAM cells with optimized overhead and reliability have been proposed in this paper. The cells can self-recover from all possible SNUs and the SCCS cell can additionally self-recover from one part of DNUs. For those node-pairs that cannot self-recover from a DNU, the position of the nodes in the SCCS cell-layout may prevent their occurrence. The proposed cells can be effectively used in fields, such as highly reliable terrestrial applications, where higher reliability is indispensable.

In our further work, we will tapeout a test chip based on the proposed SRAMs, prepare the fabrication data, and analyze the results.

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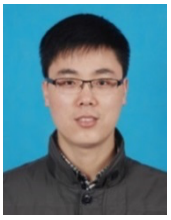

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