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Abstract—With the aggressive reduction of CMOS transistor feature sizes, the soft error rate of nano-scale integrated circuits increases exponentially. In this paper, we propose a novel cost-optimized and robust latch, namely CRLHQ, hardened against quadruple-node-upsets (QNUs) for nanoscale CMOS technology. The latch mainly comprises a 5×5 matrix based on interlocked source-drain cross-coupled inverters to robustly store logic values. Owing to the redundant constructed feedback loops, the latch can recover from all possible QNUs. Simulation results demonstrate all key QNUs' recovery of the proposed CRLHQ latch. Simulation results also show that the latch can approximately reduce 44.3% D-Q delay, 7.3% silicon area and 14.2% delay-area-power product (DAPP), compared with the state-of-the-art same-type reference latch that can recover from any QNU.

I. Introduction

As *complementary-metal-oxide-semiconductor* (*CMOS*) technologies scaling down, integrated circuits are becoming severely susceptible to soft errors caused by the impact of high-energy particles/rays, such as neutrons, X rays, protons, muons and alpha particles [1]. Typical soft errors include *single-node upset* (*SNU*), *double-node upset* (*DNU*), *triple-node upset* (*TNU*), and even *quadruple-node upset* (*QNU*) [2]. In the harsh radiation environment (e.g., space), cases of catastrophic accidents and economic losses caused by the failures of integrated circuits due to soft errors abound. Clearly, the reliability of integrated circuits and systems in safety-critical applications cannot be neglected. Therefore, highly robust circuit designs based on effective approaches, e.g., *radiation-hardening-by-design* (*RHBD*), for soft error tolerance are urgently needed.

In previous studies of hardening for storage circuits, SNUs and DNUs were paid more attention by researchers. Some studies have shown that *multiple-node-upset* (*MNU*) occurs more frequently in latches manufactured by CMOS process below 250nm. At present, MNUs has become an important cause of circuit failures. TNUs and QNUs are typical MNUs. Under the mechanism of charge sharing, the logic states of adjacent circuit nodes become more susceptible to the interference of high-energy particles hitting silicon [3]. As shown in Fig. 1, multi-cell upsets of circuits are much more common in newer technology nodes [4]. Therefore, MNUs must be considered for hardening in advanced CMOS circuits.

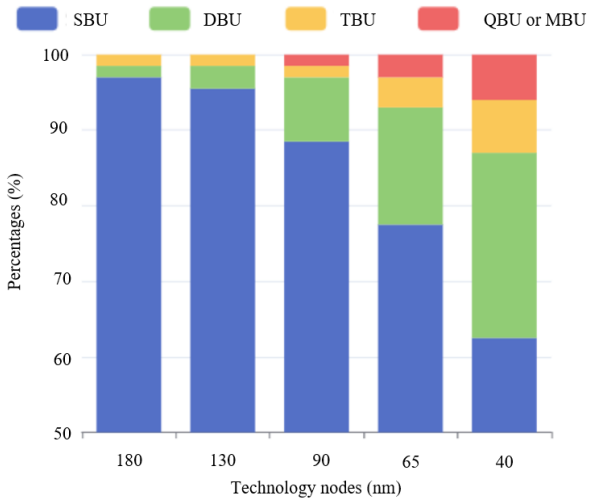

Fig.1. Multi-cell error percentages in different technology nodes.

According to [3], it is very difficult to accurately calculate the possibility of QNU occurrence, because at least six parameters should be known. This paper mainly discusses the design of latches. On the one hand, for an SNU-resilient latch fabricated with a very small technology node such as 7nm, the impact of a high-energy particle can cause a QNU due to the charge sharing mechanism. On the other hand, when the latch is hit by two high-energy particles in succession during its hold mode, it can cause two DNUs, which can form a QNU. Similarly, an SNU and a TNU can also form a QNU, if a latch cannot provide recovery from soft errors during its hold mode.

In recent decades, many robust latches [2-3, 5-15] have been proposed, to tolerate SNUs, DNUs, TNUs and even QNUs. Typical SNUs, DNUs, TNUs and/or QNUs tolerant latches include the ST [5], TILL [6], 5-MR extended from traditional *triple-modular-redundancy* (*TMR*), DNCSST [7], DeltaDICE [8], TNUTL [9], TNUHL [10], TNURL [11], QNUTL [3] and QRHIL [13]. In these latches, *C-elements* (*CEs*) are widely used. Fig. 2 shows the schematics of CEs, such as 2-input three-terminals CEs, and normal 2-input and 3-input CEs.

When the inputs of a CE have the same value, the CE only behaves as an inverter; however, when its inputs change to have different values, it intercepts the error on its input and temporarily retaining the previous correct value on its output. The clock-gating based CEs can also be controlled by the *system clock* (*CLK*) and *negative system clock* (*NCK*) signals.

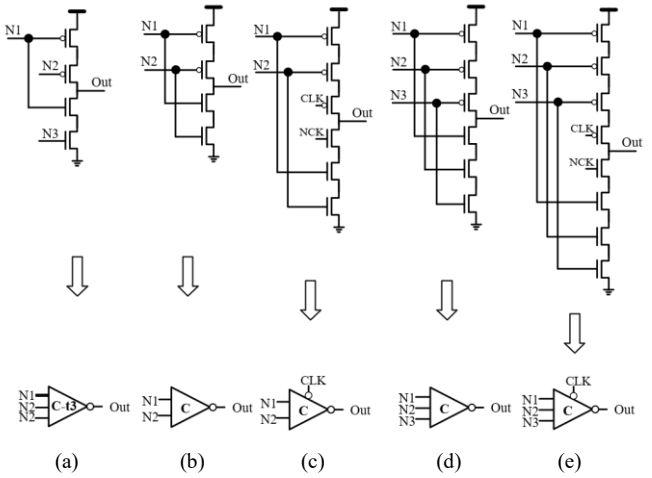

Fig. 2. Schematics of widely used C-elements. (a) 2-input three-terminals, (b) 2-input, (c) Clock-gating based 2-input, (d) 3-input, and (e) Clock-gating based 3-input.

Fig. 3 presents the circuit schematics of these typical TNU and QNU hardened latches. The TNUTL latch [9] in Fig. 3-(a) mainly comprises five 2-input three-terminals CEs, and a 2-input CE to build three-level of nodes to intercept errors. The latch can provide TNU-tolerance, but it cannot recover from TNUs.

The TNUHL latch [10] in Fig. 3-(b) employs four 4-input CEs to construct many feedback loops to retain values. Meanwhile, using *multiple-level error-interception* (*MLEI*) in the right part four CEs, the latch can provide TNU-tolerance, but it cannot recover from TNUs.

The QNUTL latch [3] in Fig. 3-(c) mainly comprises three *dual-interlocked-storage-cells (DICEs)* [14] and a triple-level *soft-error interception module* (*SIM*) that consists of six 2-input CEs. Due to the SNU self-recoverability of DICEs and the soft-error interception of the SIM, the latch can provide QNU-tolerance. However, the latch has high power dissipation.

The TNURL latch [11] in Fig. 3-(d) is mainly composed of seven mutual feedback SIMs, and any one of them is composed of two 3-input CEs and one 2-input CE. Due to the dual-level soft-error interception of each SIM and mutual feedback mechanism of SIMs, the latch can recover from TNUs. However, the latch cannot tolerate QNUs.

The QRHIL latch [13] in Fig. 3-(e) is mainly constructed from a 5×5 looped CE matrix and can recover from QNUs. However, the latch has large area overhead.

From the above discussion, it can be seen that these latches still have serious limitations. First, very few latches can provide complete self-recovery from MNUs, especially QNUs, which means that errors will be retained and accumulated. Although the TNURL can provide complete TNU recovery, it cannot tolerate QNUs and cannot recover from QNUs. Although the QRHIL can provide complete QNU recovery, its delay, area and DAPP are not small.

In this paper, we propose a novel *source-drain cross-coupled inverters* (*SCIs*) based *Cost-optimized and Robust Latch Hardened against QNUs* (*CRLHQ*). The CRLHQ latch mainly comprises two parts (i.e., the left to pre-charge the latch and the right to store the pre-charged values). The storage part of the

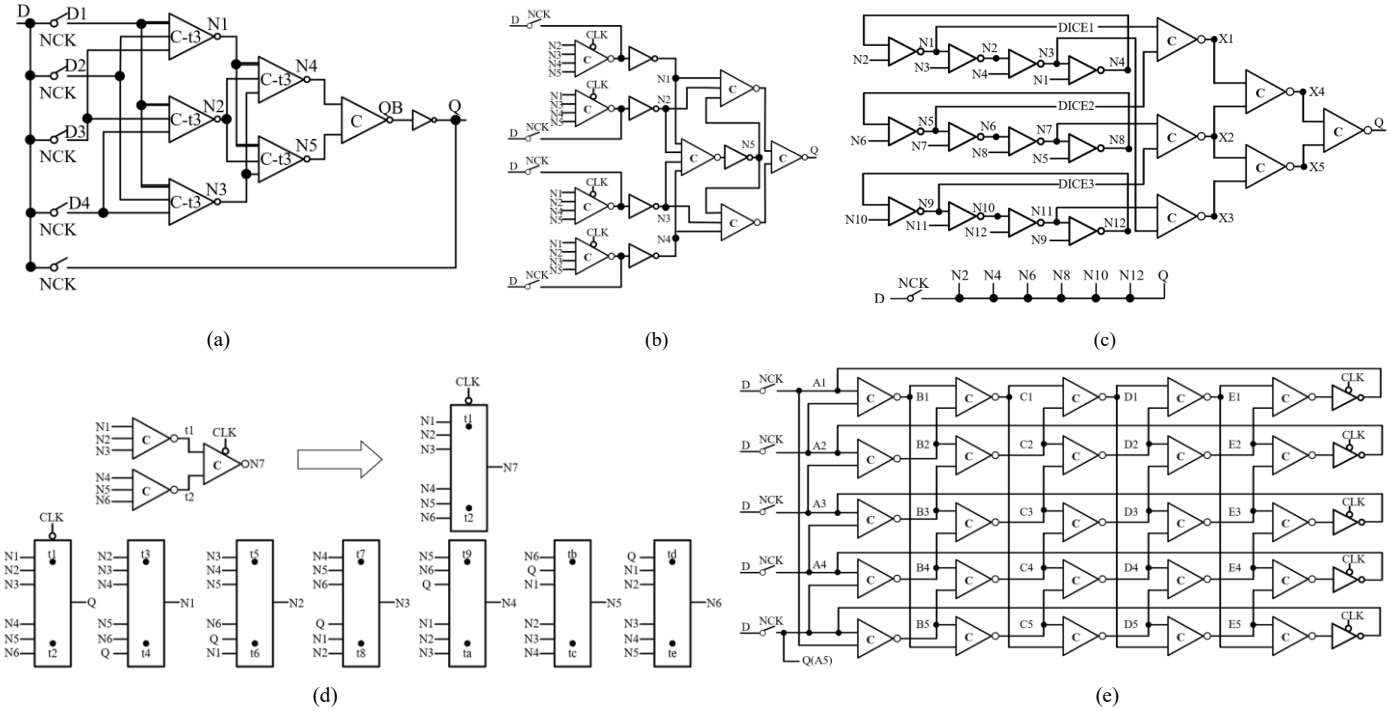

Fig. 3. Schematics of typical MNU-hardened latch designs. (a) TNUTL [9], (b) TNUHL [10], (c) QNUTL [3], (d) TNURL [11], and (e) QRHIL [13].

latch mainly comprises a 5×5 matrix based on interlocked SCIs to robustly store the pre-charged values. Simulation results demonstrate the QNU-recovery (so that SNU/DNU/TNU recovery) and low delay, silicon area and DAPP compared with the state-of-the-art same-type latch that is completely QNU recoverable.

The rest of this paper is organized as follows. Section II presents the schematic diagram, working principles, and verifications of the proposed latch. Section III provides comparison results and Section IV concludes this paper.

II. Proposed Hardened Latch Design

A. Circuit Schematic and Behavior

Fig. 4 shows the circuit schematic of the proposed CRLHQ latch design. It can be seen that the latch consists of two parts, i.e., the left-bottom part constructed from thirteen transmission gates (TGs) and the right part constructed from a 5×5 interlocked SCIs based matrix. Note that the left-top part is only used to indicate the transistor-level structures of SCIs, and the right-side SCI can also be controlled by CLK. The right part of the latch also includes a TG whose output is Q. In the CRLHQ latch, D, Q, CLK and NCK are the input, output, system clock, and negative system clock, respectively. Obviously, the right part of the latch includes five rows and five columns of SCIs so that we name the SCIs as a matrix. We define N1→ N2 → N3 → N4 → N5 as the first row and N1 → N6 → N11 → N16 → N21 as the first column. It can be seen that, in columns 2, 3 and 4, eight clock-gating based SCIs are used to reduce current competition on storage nodes, thereby saving power. In this way, the silicon area and power dissipation of the latch are balanced.

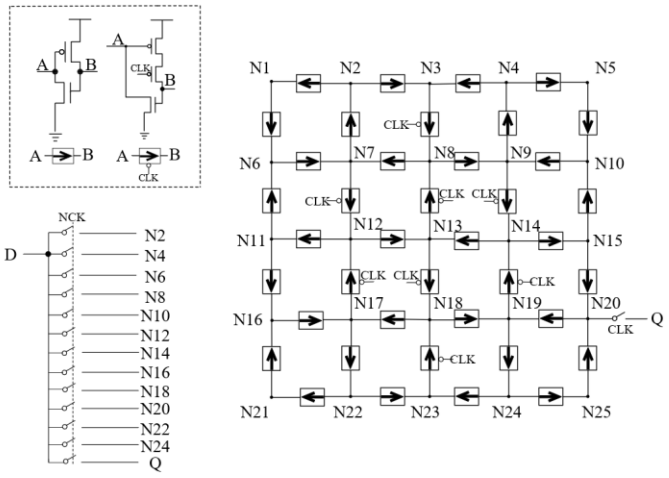

Fig. 4. Schematic of the proposed CRLHQ latch.

In the following, we take D = 0 as an example to introduce all the operations of the latch. Note that when D = 1, we can easily get the similar scenarios/conclusions.

When the TGs in the left part of the latch are ON, i.e., CLK is high and NCK is low, the latch works in transparent mode. At this time, the TG in the right part of the latch is OFF, but the left-bottom TGs are ON, thus D can be transferred directly to Q, thereby reducing the transmission delay from D to Q in transparent mode. Note that nodes Ni = Q = 0 (i = 2, 4, 8, …, 24). Because N2 = N4 = 0, the SCIs in the first row of the latch can output 1, so that N1 = N3 = N5 =1; Because N6 = N8 = N10 = 0, N7 = N9 = 1; Because N12 = N14 = 0, N11 = N13 = N15 =1; Because N16 = N18 = N20 =0, N17 = N19 = 1; Because N22 = N24 = 0, N21 = N23 = N25 = 1. In this way, the values of all nodes in the latch can be pre-charged.

When the TGs in the left part of the latch are OFF, i.e., CLK is low and NCK is high, the latch works in hold mode. At this time, the values of all nodes of the latch are still correct, and the TG with output Q is turned on, so Q = N20 = 0 in this mode. Note that the eight clock-gating based SCIs can work normally because CLK is low. Obviously, large feedback loops, such as N1 → N6 → N7 → N2 → N1 and N8 → N9 → N14 → N13 → N8, can be formed in the latch, so that the node values in the latch can be retained. In summary, the proposed latch can be operated correctly in both transparent and hold mode.

The proposed CRLHQ latch was implemented by advanced 22 nm CMOS technology and the relevant simulations are carried out by Synopsys HSPICE. The simulation parameters were introduced here. The supply voltage was set to 0.8V, the working temperature was set to the room temperature, and the PMOS and NMOS transistors had the W/L ratio of 100nm/22nm and 28nm/22nm, respectively.

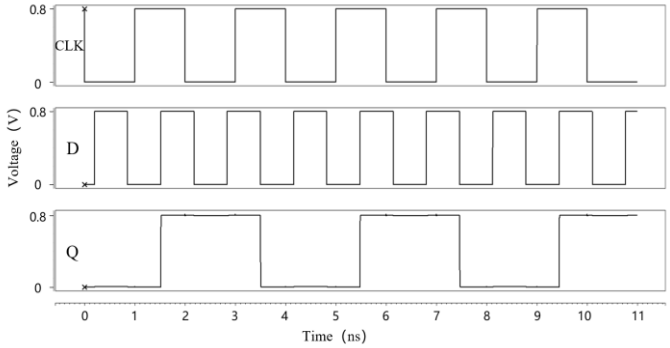

Fig. 5. Simulation results of the error-free case for the CRLHQ latch.

Fig. 5 illustrates the error-free operations for the proposed CRLHQ latch. It can be seen that when the latch works in transparent mode (CLK = 1), the output Q of the latch can change correctly with D, and when the latch works in hold mode (CLK = 0), the latch can store the sampled D value.

B. QNU-Recovery Principles and Simulations

The principles of QNU-recovery are discussed below. Because of the symmetric structure of the latch, we only need to consider two cases. ***Case T1***: Four nodes from each row of SCIs are affected by a QNU. ***Case T2***: Four nodes from different rows of SCIs in the latch are affected by a QNU. Note that, we can easily obtain similar scenarios/conclusions when we discuss the QNU nodes from the same/different columns. ***Case T1-1***: The first row of SCIs is affected by a QNU so that the representative QNU node lists include <N1,N2,N3,N4>, <N1,N2,N3,N5> and <N1,N2,N4,N5>. When <N1,N2,N3,N4> is affected by a QNU, the correct

values 1, 0, 1 and 0 of N1, N2, N3 and N4 will be changed to wrong values 0, 1, 0 and 1, respectively. At this time, N1 = 0 so that this error can pass to N6 changing N6 = 1. Then, N6 will pass the error to N11, N16 and N21, changing their logic values to 0, 1 and 0, respectively; Similarly, N2 = 1 so that this error can pass to N7, N12, N17 and N22, changing their logic values to 0, 1, 0 and 1, respectively; N3 = 0 so that this error can pass to N8, N13, N18 and N23 changing their logic values to 1, 0, 1 and 0, respectively. Meanwhile, N4 = 1 so that the logic values of N9, N14, N19 and N24 will be changed to 0, 1, 0 and 1, respectively. Note that although the logic values of N4, N9, N14, N19 and N24 are wrong, N5, N10, N15, N20 and N25 in the fifth column will not be affected and they still keep their correct values due to the special transistor structure of SCIs. At the same time, N5 with the correct value of 1 will restore N4, N3, N2 and N1 to their original correct logic values. Similarly, N10, N15, N20 and N25 will respectively restore the nodes in rows second, third, fourth and fifth to their original correct logic values. Moreover, when <N1,N2,N3,N5> is affected by a QNU, the impacted nodes in the first, second, third and fifth columns can recover from the non-impacted nodes in the fourth column; when <N1,N2,N4,N5> is affected by a QNU, the impacted nodes in the first, second, fourth and fifth columns can recover from the non-impacted nodes in the third column. In other words, the proposed latch can self-recover from QNUs for ***Case T1-1***.

Case T1-2: The second row of SCIs is affected by a QNU so that the representative QNU node lists include <N6,N7,N8,N9>, <N6,N7,N8,10> and <N6,N7,N9,N10>. When <N6,N7,N8,N9> is affected by a QNU, the correct values 0, 1, 0 and 1 of N6, N7, N8 and N9 will be changed to wrong values 1, 0, 1 and 0, respectively. At this time, N6 =1 so that this error can pass to N1 and N11 changing N1 and N11 to 0 (N11 = 0 so that N16 = 1 and thus N21 = 0); N7 = 0 so that this error can pass to N2 and N12 changing N2 and N12 to 1 (N12 = 1 so that N17 = 0 and thus N22 = 1); Similarly, N8 and N9 will finally flip all nodes in the third and fourth columns, respectively. However, the nodes in the fifth column are still unaffected. As mentioned in ***Case T1-1***, the latch can recover through correct states of nodes in the fifth column. Moreover, when <N6,N7,N8,N10> or <N6,N7,N9,N10> is affected by a QNU, the impacted nodes can recover from the non-impacted nodes. Therefore, the proposed latch can self-recover from QNUs for ***Case T1-2.***

Case T1-3: The third row of SCIs is affected by a QNU so that the representative QNU node lists include <N11,N12, N13,N14>, <N11,N12,N13, N15> and <N11,N12,N14,N15>. When <N11,N12,N13,14> is affected by a QNU, the correct values 1, 0, 1 and 0 of N11, N12, N13 and N14 will be changed to wrong values 0, 1, 0 and 1, respectively. At this time, N11= 0 so that this error can pass to N6 and N16 changing them to 1. Then, N6 = 1 so that N1 = 0 and N16 = 1 so that N21 = 0. Meanwhile, the nodes in the second, third and fourth columns will be flipped. As mentioned in ***Case T1-1***, the latch can recover through the correct states of nodes in the fifth column. Moreover, when <N11,N12,N13,N15> or <N11,N12,N14,N15> is affected by a QNU, the impacted nodes can also recover from the non-impacted nodes. Therefore, the latch can self-recover from QNUs for ***Case T1-***

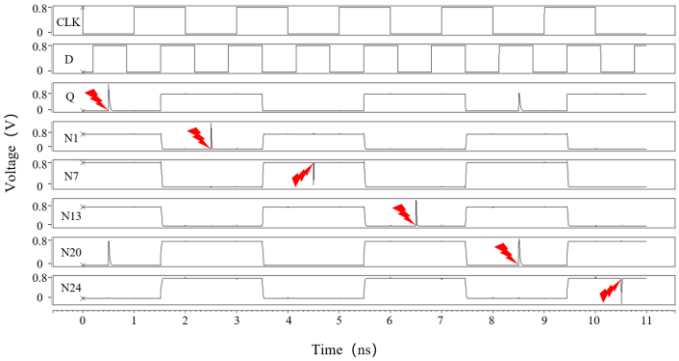

Fig. 6. Simulation results of SNU-injections for the CRLHQ latch.

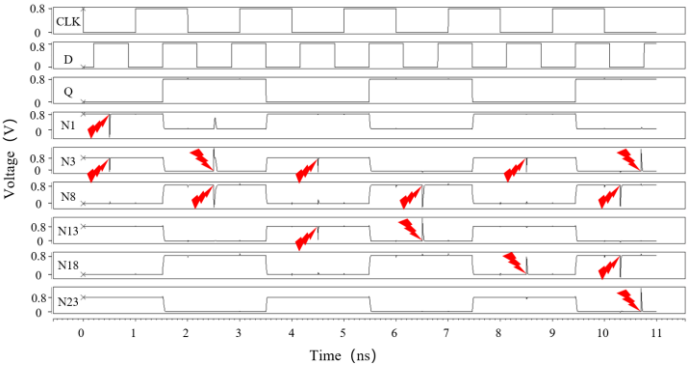

Fig. 7. Simulation results of DNU-injections for the CRLHQ latch.

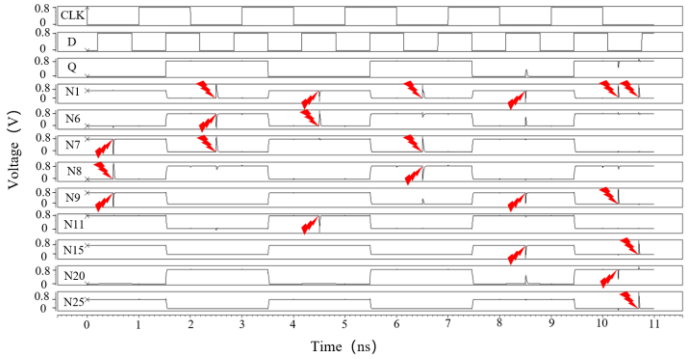

Fig. 8. Simulation results of TNU-injections for the CRLHQ latch.

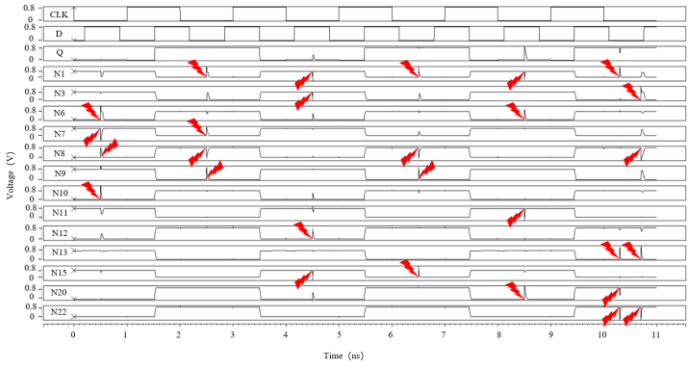

Fig. 9. Simulation results of QNU-injections for the CRLHQ latch.

3. From the above discussions, we can see that the proposed latch can recover from any possible QNU in ***Case T1***.

In ***Case T2***, there are six sub-cases. ***Case T2-1***: The QNU nodes from the first and second rows are impacted and the representative QNU node list is <N1,N7,N8,N9>. ***Case T2-2***: The QNU nodes from the first and third rows are impacted and the representative QNU node list is <N1,N3,N12,N15>. ***Case T2-3***: The QNU nodes from the first, second and third rows are impacted and the representative QNU node list is <N1,N8,N9,N15>. ***Case T2-4***: The QNU nodes from the first, second, third and fourth rows are impacted and the representative QNU node list is <N1,N6,N11,N20>. ***Case T2-5***: The QNU nodes from the first, third, fourth and fifth rows are impacted and the representative QNU node list is <N1,N13,N20,N22>. ***Case T2-6***: The QNU nodes from the first, second, fourth and fifth rows are impacted and the representative QNU node list is <N3,N8,N13,N22>. After investigation, we can see that, for all the above cases, any possible QNU cannot affect five columns of nodes at the same time. In other words, at least one column of nodes in the latch cannot be impacted so that the impacted nodes can recover through the non-impacted nodes.

From the above discussions, we can see that, the proposed latch can provide complete recovery from all key QNUs (and thus TNUs/DNUs/SNUs), so that providing very high reliability for reliable computing of safety-critical applications, especially in harsh radiation environments. Figures 6 to 9 show the simulation results for the key SNU, DNU, TNU and QNU injections of the CRLHQ latch. In the injection simulations, a controllable double-exponential-current-source model was used and the rise and fall time constant of current pulses was set to be 0.1ps and 3ps, respectively [15]. The injected charge is large enough to mimic real node upsets. It can be seen from these figures that the latch can self-recover from all injected key SNUs, DNUs, TNUs and QNUs. In summary, the latch can provide high reliability protected against SNUs, DNUs, TNUs and QNUs.

III. Comparisons

For a fair comparison, the ST [5], TILL [6], 5-MR, DNCSST [7], DeltaDICE [8], TNUTL [9], TNUHL [10], TNURL [11], QNUTL [3] and QRHIL [13] were designed using the same conditions in the same technology as the proposed CRLHQ latch (i.e., an advanced 22 nm CMOS technology, 0.8V supply voltage and room temperature).

Table I shows the reliability comparisons for alternative latches. We can see from Table 1 that the ST latch cannot provide node upset tolerance although its critical charge is effectively increased. The TILL latch can tolerate SNUs, but cannot provide SNU recovery. Although the 5-MR latch is DNU-tolerant, it cannot provide SNU/DNU recovery. The DNCSST latch is SNU/DNU-tolerant and can provide SNU recovery, but it cannot recover from DNUs. The DeltaDICE can provide DNU recovery, but it cannot tolerate TNUs. The TNUTL and TNUHL latches can provide TNU-tolerance but they cannot recover from TNUs, and the TNUTL latch even cannot provide SNU recovery. The TNURL and QRHIL latches can recover from TNUs or QNUs, but their overhead is not small. The proposed CRLHQ latch can provide SNU/DNU/TNU/QNU recovery but with low cost (especially in terms of delay, area and DAPP) that will be discussed below.

Table II shows the overhead comparisons for these latch designs in terms of delay, area, power and DAPP. Note that delay expresses D to Q transmission delay (i.e., the average of rise and fall delays from D to Q), area expresses the silicon area calculated as in [15], power expresses the average power dissipation (dynamic and static) and the DAPP means a comprehensive metric that is calculated by multiplying delay, area and power. As can be seen from Table II, the 5-MR's delay is very large because redundant transistors from D to Q are used. The delay of the TNUHL latch is also large, which is mainly due to the multilevel fault interception mechanism of the latch. However, the TNURL, QNUTL, QRHIL, as well as the proposed latch have a low delay since they use high-speed transmission paths from D to Q. Due to their intrinsic property,

TABLE I
RELIABILITY COMPARISONS AMONG THE SNU, DNU, TNU AND/OR QNU HARDENED LATCH DESIGNS.

Latch	Ref.	SNU Tolerant	SNU Resilient	DNU Tolerant	DNU Resilient	TNU Tolerant	TNU Resilient	QNU Tolerant	QNU Resilient
ST	[5]	×	×	×	×	×	×	×	×
TILL	[6]	√	×	×	×	×	×	×	×
5-MR	-	√	×	√	×	×	×	×	×
DNCSST	[7]	√	√	√	×	×	×	×	×
DeltaDICE	[8]	√	√	√	√	×	×	×	×
TNUTL	[9]	√	×	√	×	√	×	×	×
TNUHL	[10]	√	√	√	×	√	×	×	×
TNURL	[11]	√	√	√	√	√	√	×	×
QNUTL	[12]	√	√	√	√	√	×	√	×
QRHIL	[13]	√	√	√	√	√	√	√	√
CRLHQ	Proposed	√	√	√	√	√	√	√	√

the delay of the proposed latch and the QNUTL latch are the smallest.

TABLE II
OVERHEAD COMPARISON RESULTS FOR ALTERNATIVE LATCH DESIGNS.

Latch	Delay (ps)	10^{-4}×Area (nm^2)	Power (μW)	10^{-6}× DAPP
ST	14.11	1.41	0.28	0.06
TILL	14.92	3.10	0.52	0.24
5-MR	155.72	24.01	4.26	159.27
DNCSST	23.17	4.51	0.90	0.94
DeltaDICE	14.28	5.63	2.13	1.71
TNUTL	26.24	6.48	0.61	1.04
TNUHL	62.28	11.54	1.78	12.79
TNURL	6.11	18.02	1.92	2.11
QNUTL	1.85	12.39	4.23	0.97
QRHIL	3.32	18.30	1.98	1.20
CRLHQ	1.85	16.97	3.28	1.03

The area of latches is compared. Obviously, The DNCSST and DeltaDICE latches consume small area because they only consider DNU hardening with a few transistors. Similarly, because only SNU tolerance is considered, the silicon area of the TILL is very small. Although the TNUTL latch has a small area and provides TNU tolerance, it cannot recover from SNUs/DNUs/TNUs. In the RHBD approach, higher reliability is achieved at the cost of larger silicon area. The 5-MR, TNURL and QRHIL latches consume large silicon area because redundant transistors are used to provide DNU tolerance, TNU recovery and QNU recovery, respectively. It can be seen that the proposed latch's overhead is smaller than that of the same-type QRHIL latch in terms of silicon area.

The power dissipation of latches is compared. The latches only considering SNU hardening consume low power because their area is small. The 5-MR latch consumes the largest power mainly because of its largest employed area. It can be seen from Table II that the power dissipation of the QNUTL latch is very large, mainly due to much current competition in the latch. Note that, if in transparent mode, there are many feedback loops in a latch, it will lead to large power consumption. Although the silicon area of the TNURL latch is large, the power dissipation of the TNURL latch is small due to the use of clock-gating to avoid current competition. Anyway, the proposed CRLHQ latch consumes moderate power to provide QNU recovery.

In terms of DAPP, because the 5-MR and TNUHL latches have very large delay or area, their DAPP values are high. Conversely, the ST, TILL, DNCSST, TNUTL and QNUTL latches as well as the proposed latch have low DAPP values since their area, delay, and/or power are not large. The other latches have moderate DAPP values. Clearly, the proposed latch has lower overhead than that of the same-type QRHIL latch in terms of DAPP value. In summary, the proposed CRLHQ latch can provide QNU recovery (and thus TNU, DNU and SNU recovery) with low cost in terms of delay, area, and DAPP. Although its power is not small, it is not the largest.

IV. CONCLUSION

In safety-critical applications, such as aerospace and nuclear, circuits and systems need very high reliability. Existing latches suffer from severe limitations such as non-recovery from QNUs and/or large overhead. In order to solve this problem, this paper has proposed a novel cost-optimized and robust latch, namely CRLHQ, hardened against QNUs for safety-critical applications in 22nm CMOS technology. Simulation results have clearly demonstrated the QNU self-recovery as well as its low overhead especially in terms of D-Q delay, silicon area and DAPP for the proposed latch.

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