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***Abstract*— In space, the impact of radiative particles, such as neutrons and heavy ions, can change the node states of a flip-flop, thus resulting in loss of data. In this paper, a Highly reliable and Low power Radiation-hardened-by-design (RHBD) Flip-Flop cell, namely HLRFF, completely hardened against double-node-upsets (DNUs), is proposed for aerospace applications. The HLRFF is a master-slave structure. The master latch is mainly constructed from two 2-input C-elements (CEs) and one 2-input clock-gating based CE, while the slave latch has an additional keeper at the output stage. The verification results demonstrate that the proposed HLRFF is completely DNU-tolerant. Furthermore, compared to the state-of-the-art radiation-hardened FF cells, the proposed HLRFF can reduce power consumption by approximately 69%. However, only the proposed HLRFF is not only completely DNU-tolerant but also insensitive to high-impedance-state.**

***Index Terms*—radiation hardness, circuit reliability, flip-flop cell, soft error, double-node-upset**

I. Introduction

Due to aggressive shrinking of transistor feature sizes in nano-scale integrated-circuit manufacturing technologies, the amount of critical charge required to change the state of a node is constantly decreasing, easily causing soft errors [1]. Consequently, for storage circuits working in harsh radiation environments, soft errors caused by the strike of high-energy particles (e.g., heavy ions, protons, and neutrons) have become one of the main reliability challenges to their operations [2]. *Single-node-upset* (*SNU*) is one of the most common soft errors. When the charge generated by a particle through hitting silicon is collected by the source/gate diffusion of a CMOS transistor, an SNU can occur. To mitigate SNUs, RHBD for reliable circuits is an effective method, and based on which many radiation-hardened SRAMs, latches and *flip-flops* (*FFs*) have been proposed, such as those in [3-6]. This paper mainly focuses on FF cells.

In the RHBD approach, traditional inverters as well as CEs are critical components for radiation-hardness of FF cells. Figure 1 shows the transistor level implementation of a 2-input CE and the *clock-gating* (*CG*)-based 2-input CE. The working principle of a CE is that it behaves as an inverter, when its inputs, including the *system clock* (*CLK*) and the *negative system clock* (*NCK*) signals, have an identical value. However, if its input values become different, its output will enter into *high impedance state* (*HIS*) [7], thus having the previous value for a period of time. Note that a CE differs from a XOR gate which can output a high value if its two inputs are different; if its two inputs have the same value, it can output a low value.

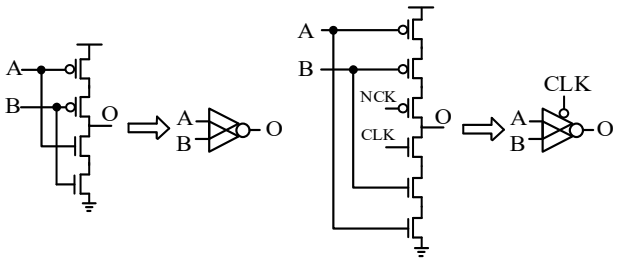

Fig. 1. Transistor level implementation of two types of C-elements. (a) 2-input. (b) Clock-gating-based 2-input.

Nowadays, with the aggressive advancement of circuit integration and the rapid reduction of transistor feature sizes, a single radiative particle has high probability to impact multiple nodes simultaneously due to charge-sharing [8-9], causing a *multiple-node-upset* (*MNU*). DNU is one of the most concerned MNUs. Moreover, compared with latches, FF cells generally have extra transistors and thus larger area, making FF cells to be more likely to be impacted by a particle causing a DNU. Therefore, DNU-hardness for FF cells is highly required, especially for aerospace applications.

Few techniques have been proposed to address the DNU issue for FF cells. Figure 2 shows the schematics of existing hardened FF cells. They are reviewed as follows.

Figure 2-(a) presents the *triple-modular-redundancy FF* (*TMR-FF*). The TMR-FF comprises three *traditional unhardened master-slave FFs* (*TUFFs*) and a 3-input voter. When two or more TUFFs are affected by soft errors simultaneously, the voter will fail to output the correct values. Thus, the TMR-FF is not DNU-tolerant. Moreover, the TMR-FF consumes large area and high power.

Figure 2-(b) shows the *dual-redundancy radiation-hardened FF* (*DRRH-FF*) [10]. The master latch comprises two independent unhardened traditional latches, while the slave latch is mainly made up of three 2-input CEs and two inverters. Obviously, when the slave latch suffers from a DNU (e.g., the outputs of two CEs are affected), the output-level CE cannot block error values. Thus, the DRRH-FF is not DNU-tolerant. Moreover, the FF is sensitive to the HIS because node Q can change to an uncertain value especially when the inputs of the output-level CE change to have different values caused by a DNU.

This work was supported in part by the NSFC under Grants 61974001 and 61874156, the NSFC-JSPS Exchange Program under Grant 62111540164, and the JSPS Grant-in-Aid for Scientific Research (B) 21H03411.

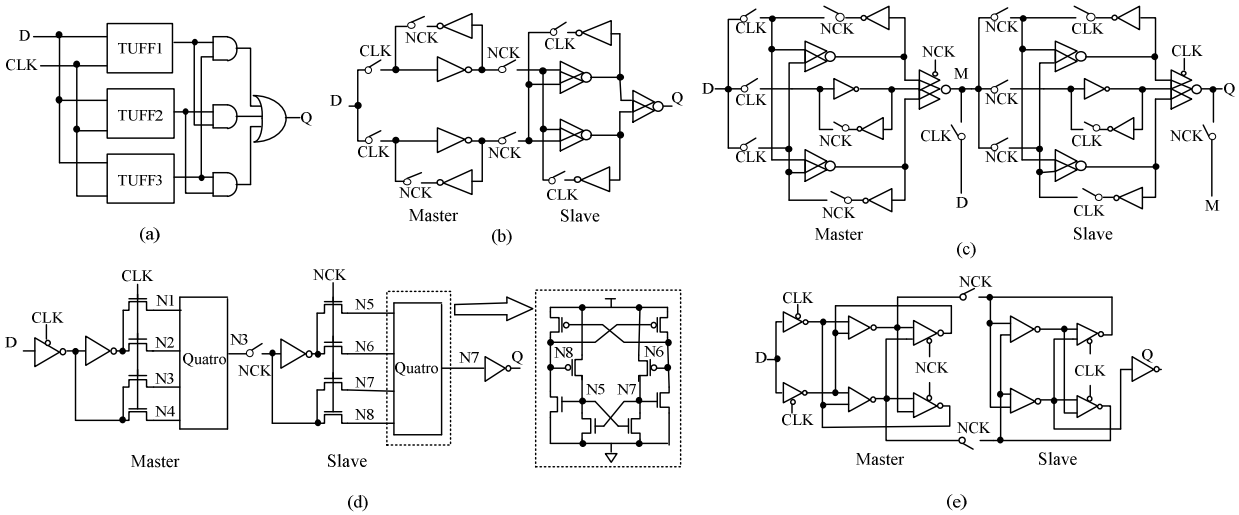

Fig. 2. Schematics of reviewed FF cells. (a) TMR-FF, (b) DRRH-FF [10], (c) DNUR-FF [11], (d) Quatro-FF [12], (e) DICE-FF [14].

Figure 2-(c) shows the *DNU-resilient FF* (*DNUR-FF*) [11]. In the DNUR-FF, multiple CEs and inverters are connected to each other to form redundant feedback loops to robustly retain values. However, the DNUR-FF is not DNU-tolerant, because the middle input and the output of any CE in the FF can be flipped by a DNU causing invalid value retention. Moreover, similarly to the DRRH-FF, the DNUR-FF cell is also HIS-sensitive.

Figure 2-(d) shows the Quatro-FF [12], which consists of several transmission transistors and two Quatro cells [13]. By constructing multiple feedback loops, the Quatro cell can keep its previous output value even if one of its four input nodes (i.e., M1, M2, M3 and M4) is flipped. Note that, if a particle affects double nodes in each Quatro cell through charge sharing, the output of the FF can be upset. Thus, the FF cannot provide DNU-tolerance. Moreover, the Quatro-FF consumes large delay and high power.

Figure 2-(e) shows the *dual-interlocked-storage-cell FF* (*DICE-FF*) [14], which employs a DICE cell as its master latch and slave latch, respectively. The input connects two non-adjacent nodes of the DICE in the master latch through CG-based inverters. Note that, a DICE can self-recover from any SNU, but it is not DNU-tolerant. In the worst case, if a node-pair inside a DICE is upset by a DNU, the output of the DICE-FF can flip. Thus, the DICE-FF cannot provide complete DNU-tolerance.

In this paper, we present a novel and robust FF cell, namely HLRFF, providing complete protection against DNUs with extremely low power. The proposed HLRFF cell is a master-slave structure. The master latch of the FF cell comprises of five *transmission gates* (*TGs*) and three 2-input CEs, two of which feed the inputs of the third CE; the slave latch has the same structure as the master but has an additional keeper. Using high-speed transmission paths, CG technologies and few transistors, the proposed FF cell features small transmission delay, low power and small area.

The rest of this paper is organized as follows. In Section II, we present the circuit structure, working principles, and verification results of the proposed HLRFF cell. Section III describes comparison results among different FF cells. Section IV concludes the paper.

II. Proposed Flip-Flop Cell

Figure 3 shows the structure of the proposed HLRFF cell. All the switches in the figure are TGs. The clock-connections of a TG are explained. If it is labeled with CLK, the CLK signal is connected to the gate-terminal of the NMOS transistor and the NCK signal is connected to the gate-terminal of the PMOS transistor. As shown in Fig. 3, the HLRFF is a master-slave structure. For the master latch, the input D is connected to the inputs (i.e., N1, N2, N3 and N4) of two independent 2-input CEs (i.e., CE1 and CE2) through four TGs. The outputs of the above CEs are connected to the inputs of CE3. The output node of CE3 (i.e., M) is also the output node of the master latch, feeding the input of the slave latch. Note that, the input D is directly connected to node M through a TG to create a high-speed path to reduce delay. For the slave latch, it is quite similar to the master one except that an additional keeper is used at the output. Nodes M and Q are the input and output of the slave latch, respectively.

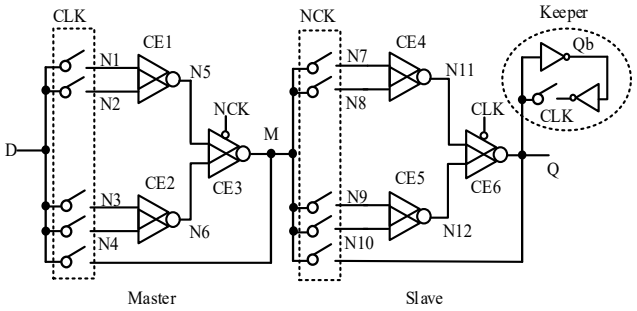

Fig. 3. Proposed HLRFF cell.

Figure 4 presents the error-free verification waveform for the HLRFF under the voltages of 0.6V, 0.7V, 0.8V, 0.9V and 1.0V. It can be seen that the Q-value changes to the D-value only at the falling edge of CLK. In any other time period, Q keeps its previous value. The waveform demonstrates that the HLRFF can work correctly in 500MHz so that it can also work correctly in 500+ MHz. Note that, the proposed HLRFF was implemented in a 22nm CMOS technology from GlobalFoundries. The PMOS transistors had the ratio W/L = 90/22nm, and the NMOS transistors had the ratio W/L =

45/22nm. The standard supply voltage was set to 0.8V, and the working temperature was set to room temperature. The simulations were performed with Synopsys HSPICE tool.

According to Fig. 4, the detailed working principle of the proposed FF is introduced here.

(1) Initially (i.e., 0ns in Fig. 4), when CLK is high and NCK is low, the input D-value can propagate to the master latch (works in transparent mode) through five TGs. In other words, the input D-value can initialize the devices in the master latch. However, in the slave latch, because the data paths are OFF through five TGs between M and N7~Q, the slave latch cannot receive any value from the master latch.

(2) When CLK changes to low (i.e., during 0ns to 1ns in Fig. 4), the input D-value can no longer propagate to the master latch (works in hold mode) through TGs but the master latch is pre-charged in Step (1). Meanwhile, the slave latch (works in transparent mode) can receive the D-value stored in the master latch and can output the value through Q. Note that, when the slave latch works in transparent mode, the feedback loop of the keeper is not formed so that there is no current competition at Q.

(3) When CLK returns to high (i.e., during 1ns to 2ns in Fig. 4), the master latch can receive a new D-value from D and can output the value to M through the left-bottom TG. Meanwhile, the slave latch enters into hold mode, and stores and outputs the value it received in step (2). Moreover, Qb is connected to Q through an inverter and a TG, and thus a feedback loop is formed in the keeper. Note that, the HLRFF is HIS-insensitive. This is because, if the inputs of CE6 become different, Q can still keep its previous value through the feedback loop in the keeper.

(4) When CLK changes to low again (i.e., during 2ns to 3ns in Fig. 4), the master latch keeps the D-value received in step (3) and the slave latch receives the value and outputs to Q. Therefore, the Q-value can be changed to the D-value only at the falling edge of CLK.

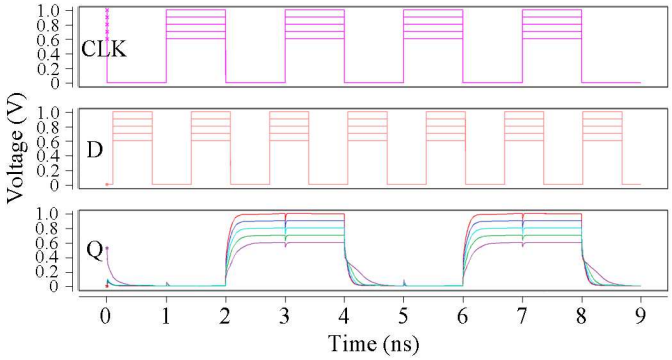

Fig. 4. Error-free verification result for the proposed HLRFF under the voltage of 0.6V, 0.7V, 0.8V, 0.9V and 1.0V.

Now, let us discuss the fault-tolerance of the proposed HLRFF. Considering the structural similarity between the master and the slave latches, we discuss the fault-tolerance of the slave latch only in this paper. In the presence of an SNU, all situations can be divided into three categories: **(a)** A single input node of CE4/CE5 is affected by an SNU. Obviously, the CE can intercept the SNU; **(b)** A single input node of CE6 is affected by an SNU. Obviously, the CE can intercept the SNU; **(c)** Q is affected by an SNU. In this situation, Q-value can self-recover through CE6 since the inputs of CE6 are correct. Thus, the indicative single nodes for SNUs are N7, N11 and Q only. Note that, if Qb is affected by an SNU in hold mode, this means that Q is affected by this SNU. Therefore, the proposed HLRFF is SNU-tolerant.

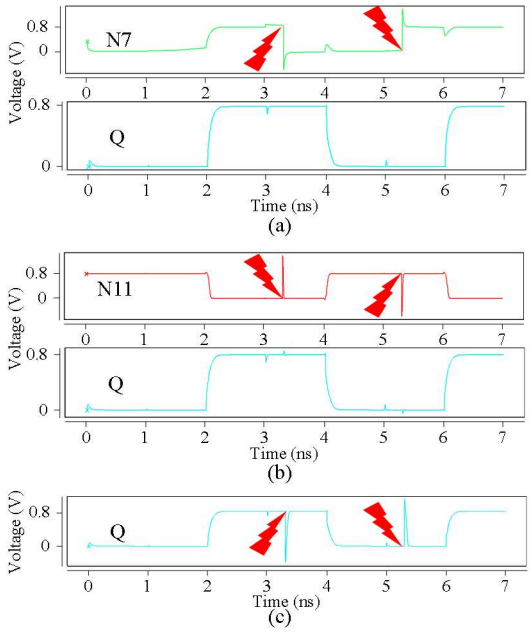

Fig. 5. Verification results for the indicative SNU injections in the HLRFF. (a) SNU on N7, (b) SNU on N11, and (c) SNU on Q.

Figure 5 shows the verification results for the indicative SNU injections on the indicative single-nodes in the proposed HLRFF cell. In Fig. 5, the lightning marks denote the inject errors. Note that we used a controllable double exponential current-source model to mimic node upsets as in [3, 5, 7] and we used injection statements in HSPICE to finish the error injections. It can be seen that, after injecting an SNU on N7, the waveform of Q is still correct; after injecting an SNU on N11 or Q, the affected single nodes can self-recover.

Next, let us consider the impact of a DNU. If one of the affected nodes belongs to the master latch while the other belongs to the slave latch, the DNU is equivalent to two SNUs. Therefore, the HLRFF can tolerate this type of DNUs. When both nodes belong to one latch (we only need to consider the slave one), there are two possible cases (Case A and Case B) that need to be discussed. Note that, if node-pair <Q, Qb> is affected by a DNU in hold mode, this means that Q/Qb is affected by an SNU, so that this node-pair can be omitted for DNU-tolerance discussion.

Case A: A DNU affects double nodes that do not belong to the same CE. The DNU node-pairs are <N7, Q>, <N7, N12>, <N7, N9>, <N7, N10>, <N8, Q>, <N8, N12>, <N8, N9>, <N8, N10>, <N9, Q>, <N9, N11>, <N10, Q> and <N10, N11>.

Note that, we can make further DNU-case divisions based on locations of the flipped node-pairs: **(A1)** When the node-pair contains Q and an input of CE4/CE5, the DNU node-pairs are <N7, Q>, <N8, Q>, <N9, Q> and <N10, Q>. Obviously, CE4/CE5 can intercept the error at its single inputs, so that the value of N11 and N12 cannot be changed. Thus, node Q can self-recover through CE6; **(A2)** When the node-pair contains the output of CE4/CE5 and an input of

CE5/CE4, the DNU node-pairs are <N7, N12>, <N8, N12>, <N9, N11> and <N10, N11>. Obviously, N11 (N12) can self-recover since the inputs of CE4 (CE5) are correct, and thus Q is still correct; **(A3)** When the node-pair contains an input of CE4 and an input of CE5, the DNU node-pairs are <N7, N9>, <N7, N10>, <N8, N9> and <N8, N10>. Obviously, CE4 and CE5 can intercept the errors at their single inputs, so that N11 and N12 cannot be changed. Thus, Q is still correct. Therefore, the proposed HLRFF can tolerate all DNUs in Case A. Note that, we select one node-pair from each above sub-case, so that the indicative DNU node-pairs in Case A are <N7, Q>, <N7, N9> and <N9, N11> only.

Figure 6 shows the verification results for the indicative DNU injections on the indicative Case-A node-pairs, respectively. Note that we use too simultaneously injected SNUs to mimic a DNU. It can be seen that, when <N7, Q> is affected, node Q can self-recover; when other node-pairs are respectively affected by a DNU, node Q can still keep its previous value.

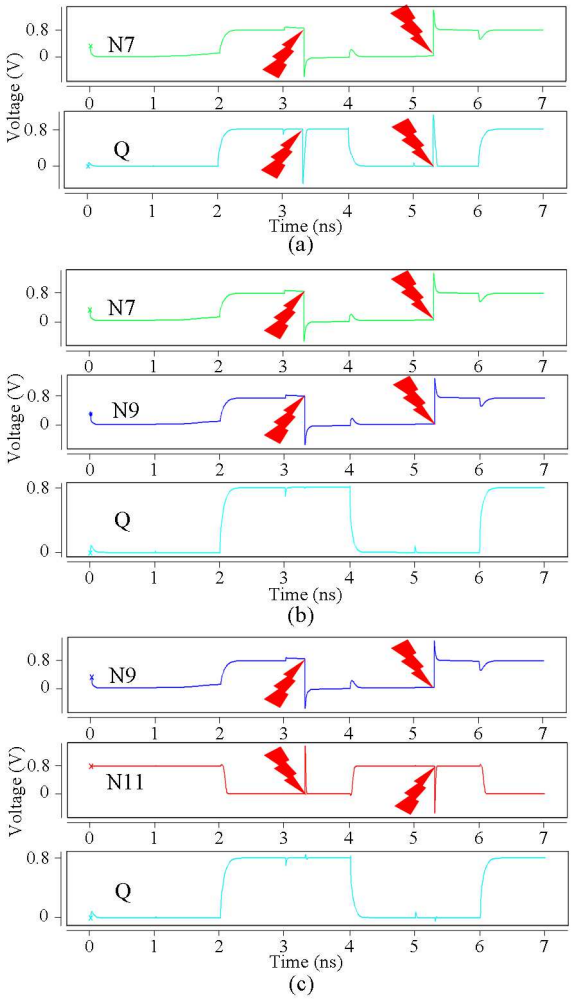

Fig. 6 Verification results for the indicative DNU (Case-A) injections in the HLRFF. (a) DNU on <N7, Q>, (b) DNU on <N7, N9>, and (c) DNU on <N9, N11>.

Case B: A DNU affects double nodes of a CE. The DNU node-pairs are <N7, N8>, <N7, N11>, <N8, N11>, <N9, N10>, <N9, N12>, <N10, N12>, <N11, N12>, <N11, Q> and <N12, Q>.

In this case, we can make further DNU-case divisions based on the locations of the flipped node-pairs: **(B1)** When the node-pair contains two nodes of CE4/CE5, the DNU node-pairs are <N7, N8>, <N7, N11>, <N8, N11>, <N9, N10>, <N9, N12> and <N10, N12>. In this case, either CE4 or CE5 cannot intercept errors at its inputs. However, the outputs of CE4 and CE5 cannot simultaneously have an error in this case. Thus, the error at N11 or N12 can be blocked by CE6 so that Q is still correct; **(B2)** When the node-pair contains two nodes of CE6, the DNU node-pairs are <N11,

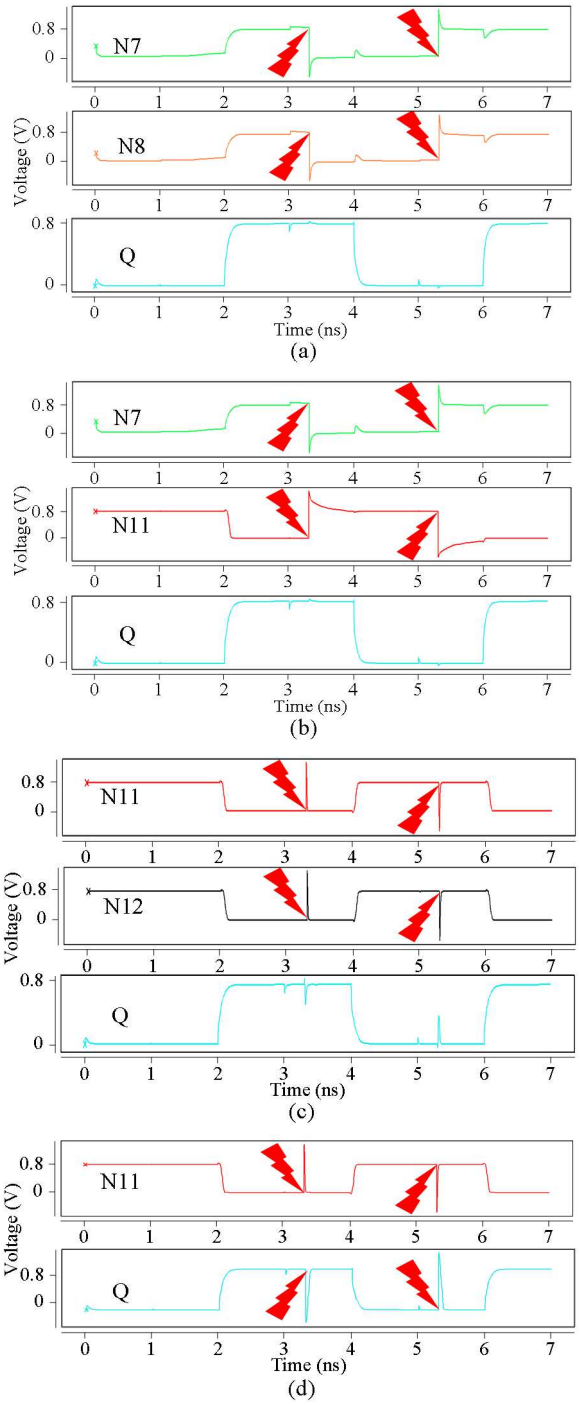

Fig. 7 Verification results for the indicative DNU (Case-B) injections in the HLRFF. (a) DNU on <N7, N8>, (b) DNU on <N7, N11>, (c) DNU on <N11, N12> and (d) DNU on <N11, Q>.

N12>, <N11, Q> and <N12, Q>. In this case, N11 and N12 can self-recover through CE4 and CE5 because the inputs of CE4 and CE5 are correct. Thus, Q can self-recover through CE6 because the inputs of CE6 are correct. Therefore, the proposed HLRFF can tolerate this type of DNUs. Note that, we select one node-pair from each above sub-case, so that the indicative DNU node-pairs in Case B are <N7, N8>, <N7, N11>, <N11, N12> and <N11, Q> only. In summary, the proposed HLRFF is completely DNU-tolerant.

Figure 7 shows the verification results for the indicative DNU injections of the above-mentioned Case B. It can be seen that, when a DNU impacts <N7, N8>, <N7, N11>, or <N11, N12>, node Q can still keep its previous value; when a DNU impacts <N11, Q>, this node-pair can self-recover. Note that, for <N11, N12> suffering from a DNU, the node pair can also self-recover. In summary, the above verifications demonstrate that the proposed HLRFF is completely SNU- and DNU-tolerant.

III. Evaluation Results

To make a fair comparison, the TUFF and all the reviewed FF cells in Fig. 2 have been implemented using the same conditions as mentioned in the previous section (22nm CMOS technology from GlobalFoundries, 0.8V standard supply voltage, and room temperature). Table I shows the reliability comparison results among those FF cells. It can be seen from Table I that, the TUFF cell is not SNU/DNU tolerant, but it is insensitive to the HIS. The DRRH-FF and DNUR-FF cells are SNU tolerant, but they are sensitive to the HIS. The TMR-FF, Quatro-FF and DICE-FF cells are SNU tolerant, and they are insensitive to the HIS. Note that, the proposed HLRFF is not only SNU/DNU tolerant but also insensitive to the HIS; therefore, it is the most reliable among these FF cells.

TABLE I
Reliability Comparison Results among the Unhardened and Hardened Flip-Flop Cells

Flip-Flops	Ref.	SNU Tolerant?	DNU Tolerant?	HIS Insensitive?
TUFF	-	No	No	Yes
DRRH-FF	[10]	Yes	No	No
DNUR-FF	[11]	Yes	No	No
TMR-FF	-	Yes	No	Yes
Quatro-FF	[12]	Yes	No	Yes
DICE-FF	[14]	Yes	No	Yes
HLRFF	Proposed	Yes	Yes	Yes

TABLE II
Overhead Comparison Results among the Unhardened and Hardened Flip-Flop Cells

Flip-Flops	Power (μW)	Delay (ps)	10^{-4}×Area (μm^2)	10^{-2}× PDAP
TUFF	1.06	17.23	2.97	0.54
DRRH-FF	1.58	43.16	5.94	4.05
DNUR-FF	2.26	42.70	11.29	10.89
TMR-FF	2.97	45.38	9.66	13.02
Quatro-FF	4.95	38.99	6.14	11.85
DICE-FF	1.79	17.13	5.64	1.73
HLRFF	0.71	29.24	8.02	1.66

Table II presents the overhead comparison results, in terms of CLK-Q delay, power dissipation, silicon area and *power-delay-area product* (*PDAP*), among the unhardened and hardened FF cells. Note that, we define the average of CLK-Q rise delay and CLK-Q fall delay as the CLK-Q delay (see Fig. 8 and Eq. (1)); we define the average power (dynamic and static) as the power dissipation; we use the approach in [7] to effectively measure silicon area; we define the product of delay, power, and area as the PDAP (see Eq. (2)). The PDAP is used to compare all aspects of overhead of FF cells in a comprehensive manner (Obviously, a small PDAP is better).

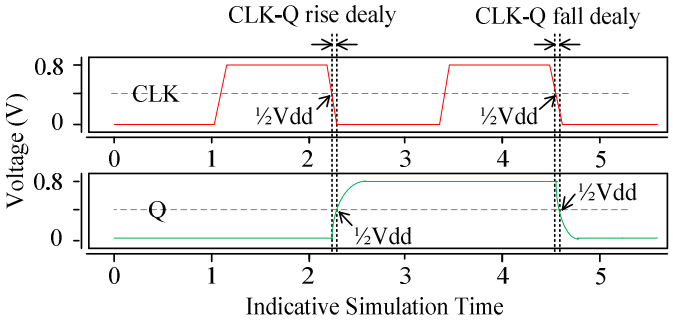

Fig. 8. CLK-Q rise delay and CLK-Q fall delay.

$$\text{CLK-Q delay} = (\text{CLK-Q fall delay} + \text{CLK-Q rise delay}) / 2 \quad (1)$$

$$\text{PDAP} = \text{CLK-Q delay} \times \text{Power} \times \text{Area} \quad (2)$$

Among all the compared FFs, the TUFF has lower power, smaller delay, and the smallest area and PDAP. This is because the FF is not SNU/DNU hardened. To tolerate SNUs and/or DNUs, by means of the RHBD approach, extra overhead has to be introduced.

Among all the compared FF cells including the proposed HLRFF, the Quatro-FF has the highest power consumption since there is significant current competition in the Quatro cell of the FF. However, the proposed HLRFF has the lowest power consumption. This is because, each node can be determined by the output of only one device, leading to no current competition in the FF. Note that there is only one feedback in the FF.

In terms of delay, among all the compared FF cells, the TMR-FF has the largest delay, mainly because there are many devices from input D to output Q. Note that, as shown in Fig. 4, Q is changed to D only at the falling edge of CLK. Thus, the devices between D and Q can determine the delay. The DICE-FF has the smallest delay since there are only a few inverters between D and Q. The proposed HLRFF consumes moderate delay since there are only a few C-elements between D and Q (note that the delay of a C-element is little larger than that of an inverter).

In terms of area, the DNUR-FF consumes the largest area, since it uses a large amount of transistors to provide partial DNU-tolerance. Moreover, among all the hardened FF cells including the proposed HLRFF, the DICE-FF consumes the smallest area since it mainly uses some inverters for hardening leading to a small amount of transistors; however, the DICE-FF cannot completely provide DNU-tolerance. The proposed HLRFF consumes moderate area since a few

C-elements is used for hardening leading to a small amount of transistors.

In terms of PDAP, the TMR-FF consumes the largest PDAP since its delay is the largest and its power and area is not small. Moreover, the TUFF consumes the smallest PDAP since its area is the smallest and its power and delay is not large. However, the proposed HLRFF consumes moderate PDAP since its power is the smallest while its delay and area is moderate.

$$\triangle\text{Power} = ((\text{Power}_{\text{comparedFF}} - \text{Power}_{\text{proposedFF}}) / \text{Power}_{\text{comparedFF}}) \times 100\% \quad (3)$$

TABLE III
QUANTITATIVE COMPARISON RESULTS OF OVERHEAD AMONG THE HARDENED FLIP-FLOP CELLS

Flip-Flops	△Power (%)	△Delay (%)	△Area (%)	△PDAP (%)
DRRH-FF	55.06	32.25	-35.02	4.05
DNUR-FF	65.58	31.52	28.96	84.76
TMR-FF	76.09	35.57	16.98	87.25
Quatro-FF	85.66	25.01	-30.62	85.99
DICE-FF	60.34	-70.69	-42.20	4.05
Average	69.15	10.73	-12.38	64.21

Table III shows the quantitative comparison results of overhead among the hardened FF cells. In Table III, △Power means the percentage of power reduction of the proposed HLRFF compared with the alternative hardened FF cells, and it is calculated through Eq. (3). Thus, the meaning of △Delay, △Area and △PDAP can be known and the calculation for them can be done. The average percentages of overhead reduction of the proposed HLRFF compared with the alternative hardened FF cells are discussed here. That is, the HLRFF can reduce power dissipation by approximately 69.2%, the CLK-Q delay by 10.7% and PDAP by 64.2%, respectively, but at the cost of increasing 12.4% silicon area on average. However, none of the state-of-the-art FF cells are completely DNU-tolerant. Moreover, the proposed HLRFF is insensitive to the HIS (so that Q is reliable). In summary, compared to all the hardened FFs, our proposed HLRFF can not only provide the highest robustness but also the lowest power consumption and a moderate overhead in terms of delay and area.

Moreover, readers may concern that there is no feedback loop in the master latch of the proposed FF (although intrinsic capacitances of CEs are temporarily holding the value once D is cut off when the master latch works in hold mode). However, even though there is a risk with the master latch in hold mode (clock low), its data has already transferred to the slave latch. Whatever changes in N1-N6 will not impact node M at all (due to CEs). If M has a direct hit and is discharged, the error may propagate to the slave latch, but will have to fight with Q. If Q is big enough (it has to be bigger as it has to drive all loads downstream), it won't overturn Q. In the other words, the combined capacitance of M and Q and all those distributed capacitances in the TG, CE4 and CE5 make it much less likely to flip so that the risk is low. For the other (clock high) phase, any upset in the master latch is irrelevant, as the upstream D will correct it when clock resumes. Therefore, if the clock stopping logic is a little smarter, this problem should be minimal.

IV. CONCLUSION AND FURTHER WORK

Due to the aggressive shrinking of transistor feature sizes, DNU is becoming more severe among soft errors yet less existing FF cells are completely DNU-tolerant. To ensure high reliability with cost-effectiveness, we have proposed an FF cell with complete SNU/DNU-tolerance, using connected CEs in a multi-level manner to intercept DNUs, using a keeper at the output to avoid HIS-sensitivity, and using fewer devices from the input to the output to reduce CLK-Q delay. The verifications demonstrate that the proposed FF can provide the highest robustness with the smallest power.

Reference [15] has reported a scan FF which is very interesting. Our further work will focus on the hardened scan FF designs.

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