A Highly Robust, Low Delay and DNU-Recovery Latch Design for Nanoscale CMOS Technology

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Abstract

With the advancement of semiconductor technologies, nano-scale CMOS circuits have become more vulnerable to soft errors, such as single-node-upsets (SNUs) and double-node-upsets (DNUs). In order to effectively tolerate DNUs caused by radiation and reduce the delay and area consumption of latches, this paper proposes a DNU resilient latch in the nanoscale CMOS technology. The latch mainly comprises four input-split inverters and four 2-input C-elements. Since all internal nodes are interlocked, the latch can recover from all possible DNUs. Simulation results show that, compared with the state-of-the-art DNU self-recovery latch designs, the proposed latch can save 64.51% transmission delay and 56.88% delay-area-power-product (DAPP) on average, respectively.

CCS CONCEPTS

• **Hardware → Circuit hardening; Latch design; Transient errors and upsets; Fault tolerance.**

Keywords: Radiation hardening; latch reliability; soft error; double-node upset; recovery

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1 Introduction

As the feature sizes of semiconductor devices shrink, the supply voltage and node capacitance decline continuously, which lessens the amount of charge stored on a node [1, 2]. Therefore, nano-scale CMOS circuits are becoming more and more vulnerable to soft errors, and the reliability of circuits has become a severe problem to which circuit designers pay more and more attention. Researchers point out that single-node-upset (SNU), double-node-upset (DNU) and single-event transient (SET) are the major types of soft errors [1, 3]. With the aggressive scaling of CMOS technologies, these effects govern the radiative response of the circuits [4]. With regard to a storage unit, particle impact can cause the state change to just one node within the cell, known as an SNU. Nevertheless, in advanced nano-scale CMOS technologies, particle impact can lead to the state changes of two nodes in a cell, which is called a DNU. In combinational logic, particle impact can cause transient pulse at a gate's output, known as an SET.

Radiation effects account for about 45% of the abnormal factors of spacecrafts, and among them, SNU is the major factor, accounting for about 80% [5]. Therefore, SNU is considered as a severe circuit reliability problem. In order to mitigate this issue, some structures have been studied as a solution to the problem [6-9]. These researches have focused on the effective tolerance of SNUs. Nevertheless, as transistors shrink, the occurrence of DNUs

becomes more likely due to the charge sharing between the near-by transistors [10] and thus also leads to a more frequent occurrence of SETs due to the reduction of critical charge. This paper mainly focuses on SNUs/DNUs.

In order to effectually alleviate the DNU issue, many attempts have been made by researchers to find efficient solutions. As a result, some proposals of DNU-tolerant latches have appeared in recently published papers [11-21]. The DNCSEIL latch [11] is DNU tolerant but cannot restore from DNUs. The DeltaDICE latch [13] employs three Dual Interlocked Cells (DICEs) to tolerate DNUs. For this design, due to the existence of the strong current competition within the DICEs, the latch causes large power consumption and extra delay. The DONUT latch [14] can tolerate DNUs through using many interlocked DICEs. However, the latch design still has higher power consumption because it constructs many feedback loops even in the transparent mode. The NTHLTCH latch [15] is designed to tolerate DNUs. Nevertheless, it uses many transistors, which can lead to extra overhead, such as high-power consumption and large area.

As mentioned above, the existing latches mainly suffer from the following problems.

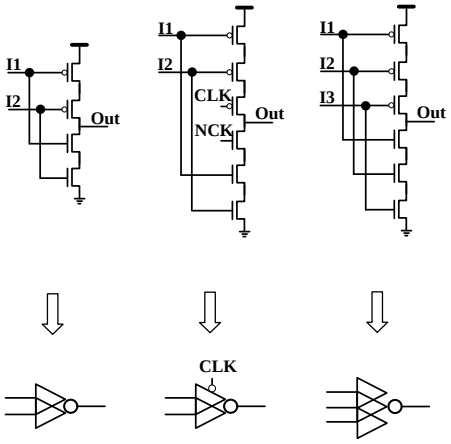

Figure 1: Different types of C-elements. (a) 2-input. (b) Clock-gating based 2-input. (c) 3-input.

(1) They cannot effectively tolerate DNUs because there exists at least one counter-example that they will output an invalid value if they suffer from a DNU.
(2) They cannot effectively self-recover from DNUs because there exists at least one counter-example that some node errors will be kept in the latches although they can output correct values if they suffer from a DNU. Note that the kept errors can be accumulated so that the reliability of the latches will be compromised.
(3) They have large overhead, especially in terms of delay and power dissipation.

In this paper, we propose a DNU self-recoverable latch with a small transmission delay and low power consumption. The latch is mainly constructed from four interlocked C-elements and four interlocked input-split inverters. The latch benefits from soft error tolerance of C-elements and low overhead of input-split inverters. The high-speed path between the input and the output of the latch can effectively reduce the delay and the small amount of used transistors can efficiently reduce the area of the latch. Simulation results show that the proposed latch design can provide complete DNU tolerance and cost effectiveness (especially in terms of delay and area) compared with the state-of-the-art DNU hardened latch designs, demonstrating that the latch can be effectively used for applications with higher reliability and lower cost requirements.

The rest of the paper is as follows. Section 2 reviews previous hardened latch designs. Section 3 introduces the proposed latch, and shows the normal operation and DNU resilience of the latch. The area, delay and power consumption of the proposed latch are compared with the previously proposed SNU/DNU hardened latches in Section 4. Section 5 summarizes this paper.

2 Previous Radiation Hardened Latch Designs

A C-element (CE) is one of the widely used components of hardened latch design as shown in Fig. 1. For a CE, if the values of its inputs are the same, it behaves as an inverter. It temporarily holds the previous value when its input values become different. Regarding the clock gating (CG)-based CE, its behavior can be also controlled by the clock CLK signal and negative clock (NCK) signal. This section reviews typical hardened latch designs, such as high performance SNU tolerant (HPST) [8], self-recoverable, frequency-aware and cost-effective (RFC) [9], double node charge sharing (DNCS) [11], DeltaDICE [13], double node upset tolerance (DONUT) [14], non-temporally hardened latch (NTHLTCH) [15], double-node upset resilient latch (DNURL) designs [16] and double node upset self-healing (DNUSH) [17].

2.1 HPST Latch

The HPST latch is designed for tolerating SNUs, mainly using three CEs and two inverters to form feedback loops to store value robustly. However, the latch cannot provide SNU resilience since the error can be kept if any input of the output-level CE is wrong.

2.2 RFC Latch

In order to realize SNU recoverability, the RFC latch mainly uses three interconnected and reciprocally feeding back CEs. Nevertheless, if the values of the outputs of two CEs are flipped because of a DNU, the latch will retain invalid data.

2.3 DNCS Latch

The DNCS latch uses six 2-input CEs to create a feedback loop to store data stably and uses a 3-input CE to intercept errors. The latch can provide not only SNU resilience but also DNU tolerance. Nevertheless, the latch cannot completely self-recover from a DNU when two nodes inside the feedback loop are flipped.

2.4 DeltaDICE Latch

The DeltaDICE latch applies three united DICE cells. It can provide DNU tolerance and recoverability through three interlocking DICE cells. However, due to the existence of the strong current competition within the DICEs, the latch suffers from large power consumption.

2.5 DONUT Latch

The DONUT latch comprises four interlocked DICEs. Due to the formed feedback loops, the latch can provide redundant nodes to

recover itself from DNUs. Nevertheless, the latch suffers from high power consumption similarly to the DeltaDICE latch.

2.6 NTHLTCH Latch

The NTHLTCH latch can provide DNU resilience. In the latch, nine CEs and three inverters can form many feedback loops to provide complete DNU recovery. However, the latch requires a significant area overhead since it uses many CEs.

2.7 DNURL Latch

The DNURL latch uses three RFC cells to make it capable of recovering from SNUs and DNUs. The latch utilizes a D-Q high-speed path and clock gating to achieve low delay and power consumption. Nevertheless, the DNURL latch is not cost-effective due to the large area.

2.8 DNUSH Latch

In the DNUSH latch, eight CEs can create many feedback loops that allow the latch to self-recover from all possible SNUs and DNUs. Note that the four inverters in the latch are used for ensuring correct logic. Nevertheless, the latch suffers from large area and delay similarly to the NTHLTCH latch.

3 Proposed Hardened Latch Design

3.1 Circuit Structure and Behavior

The circuit structure of the proposed Highly Robust and Low Delay DNU-recovery latch design (referred to as HRLD.) is presented in Fig. 2. It can be seen that the latch design consists of four transmission gates (TG1 to TG4), four input split inverters (INV1 to INV4) and four 2-input CEs (CE1 to CE4). Note that the CE4 is CG based. There is a CE between two neighboring inverters, and there is an inverter between two neighboring CEs. D and Q are the input and output of the latch, respectively. CLK and NCK are the system clock and negative system clock signals, respectively, and I1 to I7 are the internal nodes.

When CLK=1 and NCK=0, the transmission gates are ON and the latch works in transparent mode. Therefore, nodes I2, I4, I6 and Q are driven by D through the transmission gate. When D=1, D=I2=I4=I6=Q=1 and at the same time, the NMOS transistors in INV1, INV2, INV3 and INV4 can be ON, hence I1=I3=I5=I7=0. It can be seen that Q is only driven by the transmission gate TG2 between D and Q. Note that the CG based CE whose output is Q cannot output a value in this mode. Therefore, the latch can avoid current competition at the output (Q) of the CG based CE to reduce power consumption and D-Q transmission delay. In summary, the latch can work correctly in transparent mode of operation.

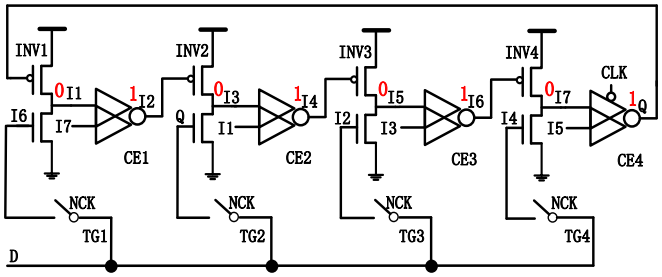

Figure 2: Schematic of the proposed HRLD latch.

When CLK = 0 and NCK = 1, the latch works in hold mode. In this mode, the transistors in transmission gates connected to D are OFF and the clock-controlled transistors in the CG based CE are ON. As a result, nodes I2, I4, I6 and Q are no longer driven by D through the transmission gates but instead are driven by the CEs and the CG based CE, respectively. At this time, all interlocked feedback loops in the latch can be formed to retain values reliably. It can be seen from Fig. 2 that, the feedback rules of the inverters and CEs are as follows: the output of any inverter (or CE) in the ordered and circulated list < INV1, CE1, INV2, CE2, INV3, CE3, INV4 and CE4> is fed to one input of the next CE (or inverter) and one input of the triply posterior CE (or inverter). For example, the output (I1) of INV1 is fed to one input (the first input) of the next/adjacent CE (CE1) and one input (the second input) of the triply posterior CE (CE2). Therefore, many feedback loops in the latch can be formed to robustly retain values for the latch in hold mode and the stored value can output through Q.

When the latch operates in hold mode, there are totally 28 DNU cases. If we denote the node distance between two adjacent nodes as λ, since the storage nodes of the latch are circularly linked, the maximum node distance is only 4λ. Considering the node distance between nodes of a node pair, these DNU cases can be divided into four disjoint parts. As shown in Fig. 2, two nodes are segregated by one to four device(s). The cases where two nodes are segregated by one device compose part 1: <I1, I2>, <I2, I3>, <I3, I4>, <I4, I5>, <I5, I6>, <I6, I7>, <I7, Q>, and <Q, I1>. The cases where two nodes are segregated by two devices compose part 2: <I1, I3>, <I2, I4>, <I3, I5>, <I4, I6>, <I5, I7>, <I6, Q>, <I7, I1>, and <Q, I2>. The cases where two nodes are segregated by three devices compose part 3: <I1, I4>, <I2, I5>, <I3, I6>, <I4, I7>, <I5, Q>, <I6, I1>, <I7, I2>, and <Q, I3>. The cases where two nodes are segregated by four devices compose part 4: <I1, I5>, <I2, I6>, <I3, I7>, <I4, Q>, <I5, I1>, <I6, I2>, <I7, I3>, and <Q, I4>. Therefore, we only need to choose one representative node-pair from each of the four parts to discuss the DNU self-recoverability.

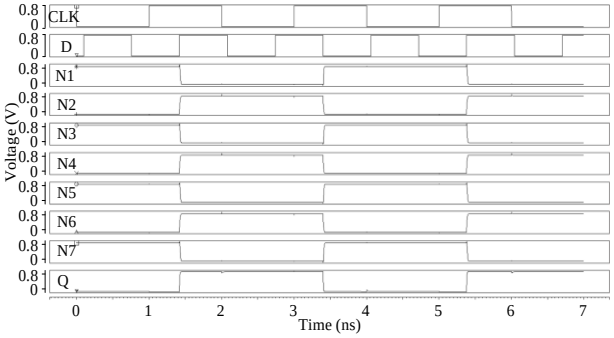

Figure 3: Simulation results without any error injection of the proposed HRLD latch.

First, let us consider the DNU affecting the node pair <I1, I2> from part 1. We assume that the previous correct value of I1 is 0 (see Fig. 3) for discussing all DNU recovery principles, so that the current value of the impacted I1 is 1 and the current value of the impacted I2 is 0. I5 and I7 are not directly affected, so that CE4 still outputs the correct value 1 at Q. Meanwhile, the PMOS in INV1 is still OFF (the error value of I1 cannot be retained) and the NMOS in INV2 is still ON (I3 still has a strong value 0). The value of I2

temporarily changes to 0, causing the PMOS in INV2 to temporarily ON, thus I3 produces a weak value 1. However, the strong 0 of I3 can neutralize the weak 1 of I3 so that I3 still has the correct value 0. The value of I1 temporarily changes to 1, but the value of I3 is correct. Therefore, CE2 can intercept the error and output the correct value 1 at I4. The value of I2 temporarily changes to 0, thus the NMOS in INV3 is temporarily OFF. However, the value of I4 is still 1. As a result, the output I5 of INV3 cannot change and still retain its correct value 0. The values of I3 and I5 mentioned above are still correct, so that CE3 outputs the correct value 1 at I6. Obviously, INV4 outputs the correct value at I7 since its inputs I4 and I6 are correct. Meanwhile, the NMOS in INV1 is still ON (I1 still has a strong value 0). Since Q=1, the PMOS in INV1 is still OFF, so that the strong value 0 of I1 can neutralize the weak value 1 generated by the particle strike at I1. Therefore, the value of I1 still has the correct value 0. The value of I7 mentioned above is still correct so that CE1 can output the correct value at I2 (since all inputs of CE1 are still correct). In summary, the node pair <I1, I2> can recover from the DNU.

Second, let us consider the DNU affecting the node pair <I1, I3> from part 2. We still assume that the previous correct value of I1 is 0, so that the current value of the impacted I1 and I3 is 1. I7 is not directly affected, so that CE1 still outputs the correct value 1 at I2. Therefore, the NMOS in INV3 is still ON (I5 still has a strong value 0). The values of I1 and I3 temporarily change to 1, thus CE2 outputs the wrong value 0 at I4, causing that the PMOS in INV3 becomes temporarily ON. As a result, I5 produces a weak value 1. However, the strong 0 of I5 can neutralize the weak 1 of I5 so that I5 still has the correct value 0. The value of I3 temporarily changes to 1, but the value of I5 is still correct. Therefore, CE3 can intercept the error and CE3 can still output the correct value 1 at I6. At this time, the NMOS in INV1 is still ON (I1 still has a strong value 0) and the PMOS in INV4 is still OFF. Meanwhile, the PMOS and the NMOS in INV4 are both OFF since the value of I4 temporarily changes to 1 and I6 is still 1 as mentioned above. As a result, the value of I7 remains at its correct value 0. The values of I5 and I7 as mentioned above are still correct, thus CE4 outputs the correct value 1 at Q. Thus, the PMOS in INV1 is still OFF and the NMOS in INV2 is still ON (I3 still has a strong value 0). Thus, the strong 0 of I1 can neutralize the weak 1 induced by the strike of the particle at I1 so that I1 still has the correct value 0. CE1 can output the correct value 1 at I2 (since all inputs of CE1 are still correct). The PMOS in INV2 is still OFF, so that the strong value 0 of I3 can neutralize the weak value 1 induced by the strike of the particle at I3. Therefore, the value of I3 still has the correct value 0. At this time, CE2 outputs the correct value 1 at I4 (since all inputs of CE2 are still correct). In summary, the node pair <I1, I3> can recover from the DNU.

Third, let us consider the DNU affecting the node pair <I1, I4> from part 3. We still assume that the previous correct value of I1 is 0, so that the current value of the impacted I1 is 1 and the current value of the impacted I4 is 0. I2 and I7 are not directly affected, so that the NMOS in INV3 is still ON (I5 still has a strong value 0). The value of I4 temporarily changes to 0, causing the PMOS in INV3 to temporarily be ON, thus I5 produces a weak value 1. However, the strong 0 of I5 can neutralize the weak 1 of I5 so that I5 still has the correct value 0. As a result, CE3 still outputs the correct value 1 at I6. At this time, the PMOS in INV4 is still OFF, and the NMOS in INV1 is still ON (I1 still has a strong value 0). The value of I4 temporarily changes to 0, so that the NMOS in INV4 is temporarily OFF. The value of I6 as mentioned above is still 1, thus I7 still remains its correct value 0. The values of I5 and I7 as mentioned above are still correct, so that CE4 outputs the correct value 1 at Q. At this time, the PMOS in INV1 is OFF, so that the strong value 0 of I1 can neutralize the weak value 1 generated by the particle strike at I1. Therefore, the value of I1 still has the correct value 0. The values of I1 and I7 as mentioned above are still correct so that CE1 can output the correct value 1 at I2. At this time, Q is still correct so that I3 can output the correct value 0. Therefore, CE1 outputs the correct value 1 at I2 since the inputs of CE1 are correct so that CE2 outputs the correct value 1 at I4. In summary, the node pair <I1, I4> can recover from the DNU.

Finally, let us consider the DNU affecting the node pair <I1, I5> from part 4. We still assume that the previous correct value of I1 is 0, so that the current value of the impacted I1 and I5 is 1. Obviously, the glitch on I1 can feed one input of CE1 and one input of CE2, the glitch on I5 can feed one input of CE3 and one input of CE4. Therefore, the output of CE1, CE2, CE3 and CE4, i.e., I2, I4, I6 and Q, are still correct since a single input error cannot affect the output of a CE. Thus, the inputs of INV1 and INV3 are still correct. As a result, I1 and I5 can recover to their correct values by the correct inputs through INV1 and INV3, respectively. In summary, the node pair <I1, I5> can recover from the DNU.

From the above detailed analysis, we can draw the conclusion that the proposed HRLD latch is completely DNU-self-recoverable because all the DNU affected node pairs can self-recover from all DNUs.

3.2 Simulation Results

The SNU/DNU resilience of the proposed HRLD latch were demonstrated by simulations. The simulations were performed by using an advanced 22 nm CMOS technology with the Synopsys HSPICE tool. The supply voltage was set to 0.8 V, and the working temperature was set to 25° C.

The transistor sizes in the latch design are as follows: (a) With regard to the normal CEs and input-split inverters, the PMOS transistors had W/L = 130nm/22nm and the NMOS transistors had W/L = 40nm/22nm; (b) With regard to the CG based CEs, the PMOS transistors had W/L = 130nm/22nm and the NMOS transistors had W/L = 80nm/22nm.

In order to verify the error-free operations of the HRLD, extensive simulations were carried out without any error injection. Fig. 3 shows the simulation results without any error injection of the proposed HRLD latch. These results demonstrate that the operations of the HRLD latch are the same as that of the conventional latch. This demonstrates the normal operational capability of the HRLD latch.

Fig. 4 shows the simulation results for the SNU injections of the proposed HRLD latch. Aiming at validating the SNU resilience, an SNU with sufficient charge was injected on I1, I2, I3, I4, I5, I6, I7 and Q, respectively. We can clearly see from the figure that any node can recover to the original correct value which confirms that the latch is SNU self-recoverable.

The simulation results for the DNU injections at key node pairs <I1, I2>, <I1, I3>, <I1, I4>, and <I1, I5> of the proposed HRLD latch

are shown in Fig. 5. It can be seen that, at 2.3, 2.7, 4.3, 4.7, 6.3, 6.7, 8.3, and 8.7 ns, two SNUs with sufficient charge were injected at node pairs <I1, I2>, <I1, I3>, <I1, I2>, <I1, I3>, <I1, I4>, <I1, I5>, <I1, I4>, and <I1, I5> to mimic DNU injections, respectively. The results clearly demonstrate that the DNU-injected node pairs can rapidly recover from DNUs.

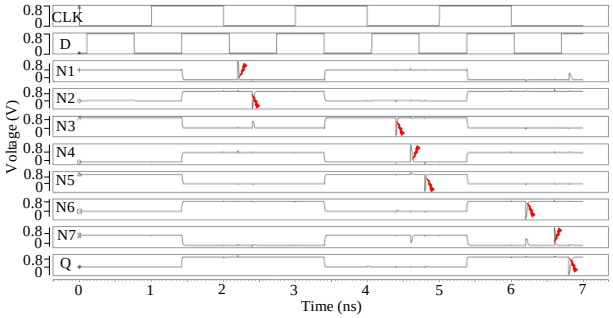

Figure 4: Simulation results for the SNU injections of the proposed HRLD latch.

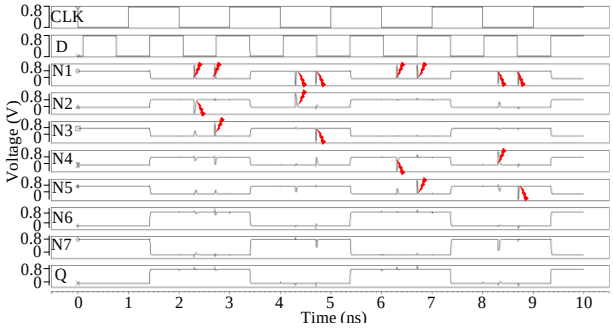

Figure 5: Simulation results for the key DNU injections for <I1, I2>, <I1, I3>, <I1, I4>, and <I1, I5> of the proposed HRLD latch (Note that any single node can be set as the output of the latch so that any node pair comprising Q is also DNU recoverable and this is also true for cases in figure 6).

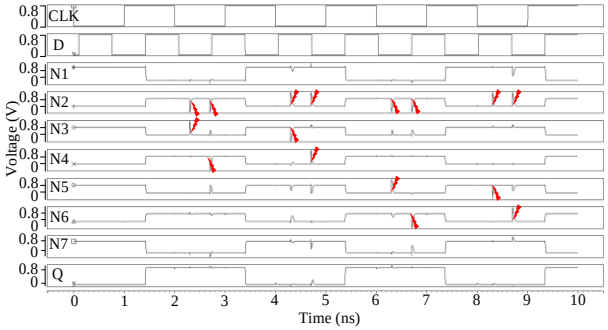

Figure 6: Simulation results for the key DNU injections for <I2, I3>, <I2, I4>, <I2, I5>, and <I2, I6> of the proposed HRLD latch.

The simulation results for the DNU injections at key node pairs <I2, I3>, <I2, I4>, <I2, I5>, and <I2, I6> of the proposed HRLD latch are shown in Fig. 6. It can be seen that, at 2.3, 2.7, 4.3, 4.7, 6.3, 6.7, 8.3, and 8.7 ns, two SNUs with sufficient charge were injected at node pairs <I2, I3>, <I2, I4>, <I2, I3>, <I2, I4>, <I2, I5>, <I2, I6>, <I2, I5> and <I2, I6> to mimic DNU injections, respectively. The results clearly demonstrate that the DNU-injected node pairs can rapidly recover from DNUs.

In summary, the above-mentioned simulation results can strongly verify the self-recoverability from SNUs/DNUs of the proposed HRLD latch. Note that, in all the above simulations, we used a controllable double exponential current source model to perform all the DNU injections [21]. The worst-case injected charge was up to 45fC. The time constants of the rise and fall of the current pulse were set to 0.1 ps and 3.0 ps, respectively.

4 Latch Comparison and Evaluation

In this section, the proposed HRLD latch is compared with the latch designs reviewed in Section 2 to further assess its performance. For fair comparison, the reviewed latches were also designed using the same conditions, i.e., same working temperature, same supply voltage, and same CMOS technology. First, the reliability comparisons among the SNU and/or DNU hardened latch designs are shown in Table 1. We can see that the HSPT latch can tolerate SNUs but cannot recover from them. The RFC latch can provide SNU resilience; however, it cannot tolerate DNUs. The DNCS latch can overcome the disadvantage of being unable to tolerate DNUs, but it cannot provide DNU recovery. The DeltaDICE latch, the DONUT latch, the NTHLTCH latch, the DNURL latch and the DNUSH latch can provide SNU and DNU resilience simultaneously. However, compared to our proposed latch, they all suffer from a large delay and/or extra silicon area, which will be discussed below.

The overhead comparisons among the SNU and/or DNU hardened latch designs are discussed here. These designs are compared in terms of D to Q transmission delay (delay), i.e., the average of rise and fall delays of D to Q, silicon area that is obtained through the model in [29], power dissipation and delay-area-power-product (DAPP). Note that power dissipation is the average power dissipation (dynamic and static) and the DAPP was calculated by multiplying D to Q transmission delay, silicon area and power dissipation. A latch with the smallest DAPP means it has the best comprehensive performance.

TABLE 1: Reliability comparisons among the SNU and/or DNU hardened latch designs

Latch	SNU Tolerant	SNU Recoverable	DNU Tolerant	DNU Recoverable
HPST [8]	Yes	No	No	No
RFC [9]	Yes	Yes	No	No
DNCS [11]	Yes	Yes	Yes	No
DeltaDICE [13]	Yes	Yes	Yes	Yes
DONUT [14]	Yes	Yes	Yes	Yes
NTHLTCH [15]	Yes	Yes	Yes	Yes
DNURL [16]	Yes	Yes	Yes	Yes
RDTL [17]	Yes	Yes	Yes	Yes
HRLD (Proposed)	Yes	Yes	Yes	Yes

The details of the overhead comparison results among these hardened latch designs are shown in Table 2. We can see that although the HPST latch designed for tolerating SNUs and the RFC latch designed for recovering from SNUs have a small delay, small area, low power and small DAPP, they cannot fully tolerate DNUs since that at least one node pair of any of them can retain the wrong values when they are affected by a DNU. Regarding the DNCS latch which cannot recover from DNUs, it has the largest delay among

these latch designs mainly since there are many devices from D to Q.

TABLE 2: Overhead comparison results of the SNU and/or DNU hardened latch designs

Latch	Delay (ps)	10^{-4}×Area (nm^2)	Power (μW)	10^{-2}× DAPP
HPST [8]	2.53	5.50	1.43	0.20
RFC [9]	3.09	4.64	0.44	0.06
DNCS [11]	65.41	8.60	2.35	13.22
DeltaDICE [13]	16.29	7.10	2.18	2.52
DONUT [14]	19.34	6.36	2.30	2.83
NTHLTCH [15]	13.19	11.37	2.27	3.40
DNURL [16]	4.02	13.93	1.18	0.66
DNUSH [17]	4.03	9.35	1.24	0.47
HRLD (Proposed)	2.50	6.62	2.75	0.46

In comparison with several other latches, such as DeltaDICE, DONUT, NTHLTCH, DNURL and DUSH, that can provide complete DNU resilience, we can see that our proposed latch has a small delay, moderate and even small area, as well as a small DAPP. ***(Detailed Delay Comparison)*** Compared with the DNU self-recoverable latches, our proposed latch has the lowest D-Q transmission delay, which can be seen from Table 2. The reason why our proposed latch suffers from the lowest delay is that there is a high-speed transmission path used from D to Q and the clock gating is also used at the CE whose output is Q to reduce the current competition at Q. ***(Detailed Area Comparison)*** The area of the NTHLTCH latch is large primarily because of the large number of employed CEs in it. Besides, the DNURL latch and the DNUSH latch also have large area compared with our proposed latch. ***(Detailed Power Comparison)*** The power consumption of the DeltaDICE latch is large primarily due to the existence of the strong current competition within the DICEs. The DONUT latch also forms many feedback loops in the transparent mode which makes it have higher power consumption. ***(Detailed DAPP Comparison)*** We also can see from Table 2 that our proposed latch has the lowest DAPP among the DNU hardened latches. This is because, the delay of our proposed latch is the smallest, the area of our proposed latch is close to the smallest, although the power dissipation of our proposed latch is the highest. Note that we can use clock gating for devices to significantly reduce the power consumption, but the area will be increased.

For a quantitative comparison, the relative overhead of the reviewed DNU recoverable latches was compared to our proposed latch in terms of delay (ΔDelay), area (ΔArea), power (ΔPower), and DAPP (ΔDAPP) calculated using the following formula and the relative overhead comparison results are shown in Table 3. It can be seen that, our proposed latch can reduce transmission delay by 64.51%, can save 25.23% silicon area as well as 56.88% DAPP on average, but at the cost of 64.33% extra power consumption compared with other DNU recoverable latch designs. In summary, the quantitative comparison results demonstrate the reasonable overhead of the proposed latch to provide high reliability for high performance and aerospace applications.

$$\Delta = (\text{Overhead}_{\text{compared}} - \text{Overhead}_{\text{proposed}}) / \text{Overhead}_{\text{compared}} \times 100\%$$

TABLE 3: Relative overhead comparisons of the DNU self-recoverable latch designs compared with ours

Latch	Δ Delay (%)	Δ Area (%)	Δ Power (%)	Δ DAPP (%)
DeltaDICE [13]	84.65	6.76	-26.15	81.75
DONUT [14]	87.07	-4.09	-19.57	83.75
NTHLTCH [15]	81.05	41.78	-21.15	86.47
DNURL [16]	31.81	52.48	-133.05	30.30
RDTL [17]	37.97	29.20	-121.77	2.13
Average	64.51	25.23	-64.33	56.88

5 Conclusions and Further Work

In this paper, we have proposed a novel high performance and DNU self-recoverable latch design. Compared with other DNU self-recoverable latches, the proposed latch has the smallest delay to improve performance. The proposed latch only uses a small number of transistors than most of the DNU recoverable latches. Simulation results have demonstrated the DNU recovery, low delay and moderate silicon area of the proposed latch so that the latch can be applied to high performance and aerospace applications.

Due to page limitation, some extra work cannot be done and shown in this paper. In our further work, we will consider SET hardening to improve the latch reliability and perform the PVT simulations, etc.

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