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Two 0.8 V, Highly Reliable RHBD 10T and 12T SRAM Cells for Aerospace Applications

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ABSTRACT

Aggressive scaling of CMOS technologies requires to pay attention to the reliability issues of circuits. This paper presents two highly reliable RHBD 10T and 12T SRAM cells, which can protect against single-node upsets (SNUs) and double-node upsets (DNUs). The 10T cell mainly consists of two cross-coupled input-split inverters and the cell can robustly keep stored values through a feedback mechanism among its internal nodes. It also has a low cost in terms of area and power consumption, since it uses only a few transistors. Based on the 10T cell, a 12T cell is proposed that uses four parallel access transistors. The 12T cell has a reduced read/write access time with the same soft error tolerance when compared to the 10T cell. Simulation results demonstrate that the proposed cells can recover from SNUs and a part of DNUs. Moreover, compared with the state-of-the-art hardened SRAM cells, the proposed 10T cell can save 28.59% write access time, 55.83% read access time, and 4.46% power dissipation at the cost of 4.04% silicon area on average.

KEYWORDS

CMOS, SRAM cell, radiation hardening, single node upset, double node upset

1 Introduction

Nowadays, in nanoscale CMOS technologies, SRAM circuit integration and performance have been significantly improved mainly by reducing transistor sizes [1]. However, the dramatic reduction of transistor feature sizes induces that the critical charge of circuit nodes to become small. As a result, modern advanced SRAMs are becoming increasingly prone to soft errors caused by the strike of particles [2]. Soft errors can cause the logic value of a node inside an SRAM to be flipped, and the flipped value can be read, thus causing a serious system failure. Therefore, it is crucial for circuit designers to propose reliable SRAM designs to mitigate reliability issues caused by soft errors. Recently, several radiation-hardening-by-design (RHBD) based reliable SRAMs have been proposed. In terms of FinFET-based SRAMs [3], they can reduce the soft error rate at transistor or cell

level. However, these cells cannot provide high reliability for safety-critical applications in harsh environments. Therefore, effective and scalable solutions for tolerating soft errors are still highly required for other technologies (CMOS, FDSOI), especially for aerospace applications.

In a combinational logic circuit, when a radiation particle directly strikes a sensitive node, it ionizes on the incident path, and the corresponding single sensitive node collects the wrong charge and causes the logical value of the node to be flipped. This is called a single event transient (SET) [4]. On the other hand, an OFF-state transistor in a storage element may be directly struck by a radiation particle, thus charging the node-value, which is called a single node upset (SNU). However, in modern advanced nanoscale CMOS technologies, the sharp reduction of transistor feature sizes can provide high circuit integration. Therefore, due to charge sharing, the impact of one particle can simultaneously change the states of two nodes in a memory cell [5], which is called a double-node upset (DNU).

Many latches, flip-flops, and SRAMs have been proposed by researchers to tolerate/mitigate SNUs and/or DNUs [6-25]. Typical designs about SRAMs include NASA13T [18], RHD12T [19], QCCM12T [20], QUCCE12T [21], DNUSRM [22], we-Quatro [23], Zhang14T [24], and QCCM10T [20]. However, these SRAMs still have the following problems.

(1) Most SRAM cells can achieve self-recovery from SNUs, but they have high power consumption and large silicon area, such as NASA13T [18], RHD12T [19], QCCM12T [20], QUCCE12T [21], DNUSRM [22], and we-Quatro [23]. Moreover, some cells have a large read and write access time, such as NASA13T [18] and QUCCE10T [21].

(2) Many SRAM cells are not effectively hardened against DNUs. For example, neither RHD11 nor RHBD13 can effectively tolerate DNUs.

Based on the radiation hardening by the design (RHBD) approach, a highly reliable RHBD10T cell is firstly proposed in this paper. The proposed 10T cell has four interlocked input-split inverters to self-recover from SNUs because of its internal feedback loops. The read/write access time (R/WAT) and area of the RHBD10T cell are considerably low mainly since it uses a smaller number of transistors. The reliability and optimized access operations of the proposed SRAM cells are demonstrated by simulation results.

The rest of this paper is organized as follows. Section 2 introduces the schematic and working principles of the proposed cells. Section 3 presents the comparison and evaluation results of the proposed cells. Section 4 concludes this paper.

2 Proposed SRAM Cells

2.1 Schematic and Normal Operations

Fig. 1 shows the schematic of the proposed RHBD10T cell. The RHBD10T cell consists 10 transistors. Transistors P1 to P4 and N1 to N4 are used for keeping values. Transistors N5 to N6 are used for access operations that are controlled by word-line WL and connected to bit-lines BL and BLB. The nodes I1 to I4 are used for keeping values. When WL = 1, the access transistors N5 and N6 are ON, allowing write/read access operations to be executed. When WL = 0, the cell keeps the stored value.

Fig. 1 shows the case where the cell stores 1, i.e., I1 = I3 = 0 and I2 = I4 = 1. First, we consider the case of writing 0. Before the write operation, both the bit-lines BL and BLB are charged up to VDD by pre-charge circuitry. One of the bit-lines then discharges to 0 due to write circuitry. In this case, BLB goes to 0. When WL becomes high, the operation of writing 0 to the cell is executed. At this time, transistors N1, N3, P2, and P4 are turned ON and transistors P1, P3, N2 and N4 are turned OFF; as a result, the stored value is rightly changed to 0. The operation of writing 0 is completed.

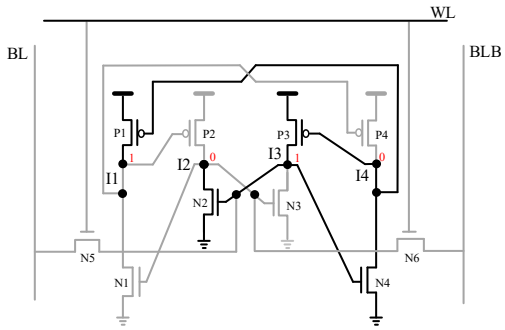

Fig. 1. Schematic of the proposed RHBD10T cell.

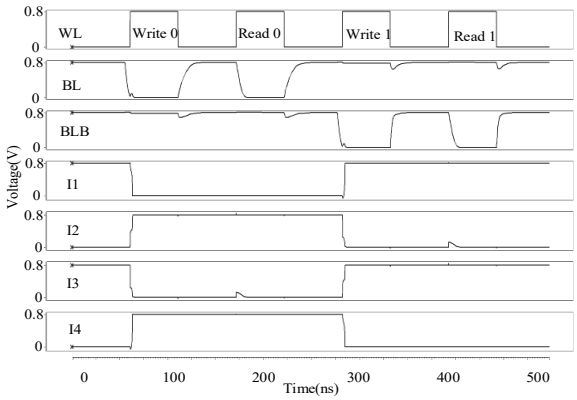

Fig. 2. Simulation results for normal operations of the proposed RHBD10T cell.

Next, we consider the case of reading the stored 0. Before the read operation, both bit-lines BL and BLB are charged up to VDD by pre-charge circuitry. When WL = 1, the operation of reading 0 from the cell is executed. At this time, the voltage of BL does not change. However, the voltage of BLB decreases because of its discharge operation through N5 and N6. Once the differential sense amplifier detects the voltage difference between BL and BLB, the read operation is finished and the cell outputs the stored value. For writing/reading 1, the similar scenario can be observed. Simulation results of the normal operations of the proposed RHBD10T cell are shown in Fig. 2. It can be seen that the write/read operations are all correctly executed.

Next, we describe the SNU and DNU self-recovery principle of the proposed RHBD10T cell. Here, we consider the case where 1 is stored in the cell (i.e., I1 = I3 = 1 and I2 = I4 = 0). In the next

section, we discuss the SNU and DNU self-recovery principle, respectively.

2.2 SNU Self-Recovery Principle

The cell-state shown in Fig. 1 is considered for SNU self-recovery analysis, and we first consider the case where I1 is affected by an SNU. In this case, I1 is temporarily changed to 0 from 1, and hence P2 and P4 are temporarily changed from OFF to ON. Since I3 is not affected (i.e., I3 = 1), N2 and N4 are still ON. Thus, I2 and I4 still have the correct value of 0. Thus, N1 is still OFF and P1 is still ON, so that I1 can self-recover from the SNU. Note that the similar SNU self-recovery principle can be observed when any other single node is affected by an SNU.

When the cell stores the value 0, the analysis and simulation results allow to be concluded that the cell can also self-recover from any SNU. We first consider the case where I1 is affected by an SNU. When I1 is temporarily changed to 1 from the original value of 0 due to the SNU, P4 and P2 become OFF. At this time, I3 is not affected by the SNU, and it still has the original value (i.e., I3 = 0). Hence, N2 and N4 remain OFF. Thus, I2 and I4 keep their original values (i.e., I2 = I4 = 1). Since I2 =1 and I4 = 1, N1 and N3 become ON and P1 and P3 become OFF. Thus, I1 can self-recover from the SNU. Note that, when I3 is affected by an SNU, i.e., I3 is temporarily changed to 1 from 0, the similar SNU self-recovery principle can be observed.

Next, we consider the case where I2 is affected by an SNU. In this case, I2 is temporarily changed to 0 from the original value 1 due to the SNU, and N1 and N3 become OFF. At this time, the SNU is intercepted by N1 and N3. Thus, I1 and I3 are not affected (I1 = I3 = 0) and P4 remains ON. Since I4 is also not affected (I4 = 1), P1 remains OFF, I1 keeps the value of 0 and P2 is ON, so that the value of I2 is still 1. Therefore, I2 can self-recover from the SNU. Note that, when I4 is affected by an SNU, i.e., I4 is temporarily changed to 0 from 1, the similar SNU self-recovery principle can be observed.

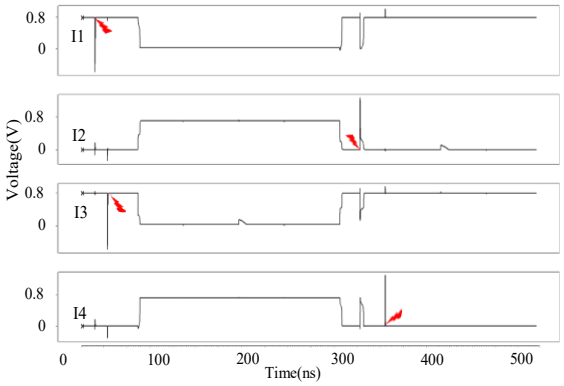

Fig. 3. Simulation results for SNU self-recovery of the proposed RHBD10T cell.

The simulation results for SNU self-recovery on nodes I1 to I4 of the proposed RHBD10T cell are shown in Fig. 3. At 20 ns and 40 ns, an SNU was respectively injected to nodes I1 and I3. At 320 ns and 340 ns, an SNU was respectively injected to nodes I2 and I4. It can be seen from Fig. 3 that the proposed cell can self-recover from all possible SNUs.

2.3 DNU-Tolerance Principle

Let us now consider the DNU tolerance principle of the proposed RHBD10T cell. The key node-pairs are <I1, I4> and <I2, I3>. We first describe the case where the RHBD10T cell stores 1. First, we consider the case where <I1, I4> is affected by a DNU, i.e., I1 is temporarily changed to 0 from the original value of 1 and I4 is temporarily changed to 1 from the original value of 0. Thus, P2 becomes temporarily ON and P3 becomes temporarily OFF, I2 has the value of weak 1. Since I3 is not directly affected (I3 = 1), N4 and N2 remains ON and N1 remains OFF, I2 has the value of strong 0 and I4 = 0. The strong 0 neutralizes the weak 1; as a result, N1 is ON, and I1 = 1. Finally, all nodes and transistors can return to their original states. In other words, <I1, I4> of the proposed RHBD10T cell can self-recover from the DNU.

Let us now describe the case where <I2, I3> is affected by a DNU. In this case, I2 is temporarily changed to 1 from 0 and I3 is temporarily changed to 0 from 1. At this time, N1 and N3 are temporarily changed from OFF to ON, and N2 and N4 are temporarily changed from ON to OFF. Clearly, P1, P2, P3, and P4 are not directly affected, having their original states. Since I1 = 1, P4 and N4 are OFF, I4 has the value 0, so that P3 is ON, and hence I3 still has the value 1. Since I3 = 1, N2 is ON and P2 is OFF, I2 can recover to the value 0. In other words, node pair <I2, I3> of the cell can self-recover from the DNU. In summary, the proposed RHBD10T cell provides DNU tolerance ability.

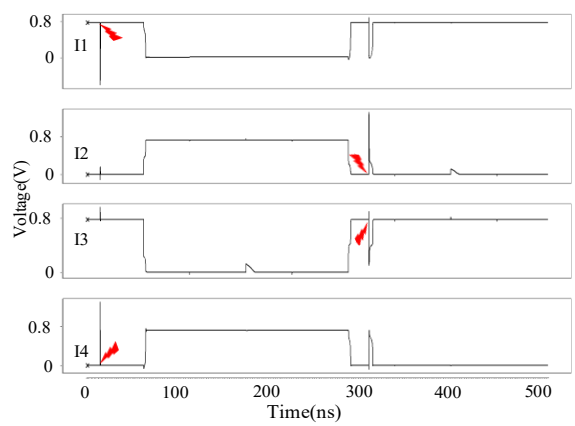

Fig. 4. Simulation results for DNUs of the proposed RHBD10T cell.

Fig. 4 shows the simulation results for DNU self-recovery of node pairs <I1, I4> and <I2, I3> of the proposed RHBD10T cell. In the case of 1 being stored (I1 = 1), DNUs were injected to node pairs <I1, I4> and <I2, I3> between 0 and 100 ns and between 300 and 400 ns, respectively. In the case of 0 being stored (I1 = 0), DNUs were injected to node pairs <I1, I2> and <I3, I4> between 100 and 300 ns, respectively. We can conclude from Fig. 4 that the proposed RHBD10T cell can self-recover from DNUs on node pairs <I1, I4> and <I2, I3> when storing 1 and 0, respectively.

In the above simulations, we use a flexible double-exponential current source model to perform all fault injections. The time constant of the rise and fall of the current pulse was set to 0.1 and 3 ps, respectively. The proposed cells are implemented using an advanced 22 nm CMOS library under the room temperature and a 0.8V supply voltage. All simulations were performed by the Synopsys HSPICE tool.

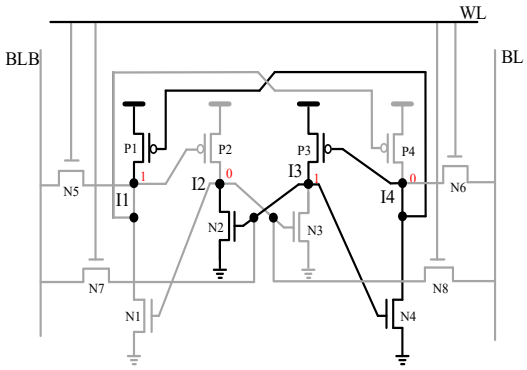

Fig. 5. Schematic of the proposed RHBD12T cell.

In order to reduce the read and write access time, the RHBD12T cell is proposed and the schematic of the cell is shown in Fig. 5. It can be seen that the storage module of RHBD12T is the same as that of RHBD10T. Therefore, the RHBD12T cell has the same soft-error tolerance ability when compared to the RHBD10T cell, i.e., they have the same SNU and DNU tolerance principles. However, the RHBD12T cell uses two extra access transistors compared to the RHBD10T cell to effectively improve the access operation performance. The simulation results for SNUs and DNUs self-recovery on nodes I1 to I4 of the proposed RHBD12T cell are similar to those of the proposed RHBD10T.

3 Comparison and Evaluation

The performance of the proposed designs RHBD10T and RHBD12T are compared to previous radiation hardened cells reviewed in Section II. We have made a comparison of many parameters in the same conditions. These parameters include SNU recoverability (SNUR), number of DNU Hardened node-Pairs (#DHP), read access time (RAT), write access time (WAT), average power dissipation, and silicon area, as shown in Table I. Let us describe the performance comparison. From Table I, we can see that the RHD12T, DNUSRM, RHBD12T and RHBD10T cell can completely self-recover from all possible SNUs, while the other cells have at least one node that cannot self-recover from an SNU. In terms of DHP, the 6T, NASA13T, QUCCE12T, and Zhang14T cells have no DHP, the QCCM12T, and QCCM10T cells have one DHP, the RHD12T and We-Quatro cells have 4 DHPs, and the RHBD12T and RHBD10T cells have 2 DHPs. However, the DNUSRM cell has 16 DHPs because it has many redundant nodes. It is clear that, except the DNUSRM cell, only the proposed RHBD12T and RHBD10T cells have the maximum number of DHPs, which is 4. In summary, except the DNUSRM cell, the proposed RHBD12T and RHBD10T cells can achieve much better performance than the other cells that has large power and area.

Now, we describe the qualitative overhead comparison. For WATs and RATs, it can be seen from Table I that the proposed RHBD12T cell has the smallest WAT except the 6T cell. This is mainly because the cell has less current competition when writing a value. The proposed RHBD10T has a relatively large WAT due to more current competition when writing a value. The proposed cells have a comparable WAT compared with the other hardened cells. However, the proposed RHBD12T cell has the smallest RAT except the DNUSRM cell due to the use of 4 parallel access transistors for reading a value. The proposed RHBD10T cell has a smaller RAT compared with most cells mentioned above. The NASA13T has the largest RAT due to its special read operation (it has specific extra read transistors). The intrinsic charge/discharge of cell nodes through access transistors can affect WATs and RATs.

As for power and area, we believe that a cell will have a large power consumption and large area overhead if it uses many transistors, and it will have a small power consumption and small area overhead when using only a few transistors. It can be seen from Table I that the 6T cell has the smallest power consumption and area overhead because it uses only 6 transistors. From Table I, we can see that the DNUSRM cell has the largest power consumption and area overhead. This is because of using extra transistors and thus there is more current competition inside of the cell. RHD12T, QCCM12T, QUCCE12T, and the proposed RHBD12T cell have similar cell constructions and they have the same amount of transistors, so they have similar power consumption and area overhead. Except the 6T cell, it can be seen that the proposed RHBD10T cell has the smallest power consumption and area overhead, mainly because of the fewer amount of used transistors and less current competition inside of the cell.

In summary, the proposed RHBD10T and RHBD12T cells have been effectively hardened. Compared with the existing hardened cells, the proposed RHBD10T cell has lower overhead especially in terms of silicon area and power dissipation, and the proposed RHBD12T cell has lower overhead in RAT and WAT.

The temperature and voltage (TV) variations can seriously impact the performance of SRAM cells. Fig. 6 shows the simulation results of TV variation impacts on RAT, WAT, and power. In our simulation experiments, the temperature was ranged from -25°C to 125°C and the normal temperature was set to 25°C. The supply voltage variation was ranged from 0.65V to 0.95V and the normal supply voltage was set to 0.8V.

It can be seen from Fig. 6-(a), (b), and (c) that the SRAM cells generally need to consume more RAT, WAT, and power when the temperature rises. This is due to the decrease of carrier mobility when the temperature rises [8]. It can be seen from Fig. 6-(a) that the temperature variation has the large impact on the RAT of the NASA13T cell and Zhang14T cell, due to its more decreased carrier mobility when the temperature rises. However, the temperature variation has a low impact on the RAT of the other SRAM cells, such as the DNUSRM cell, the proposed RHBD10T cell and the proposed RHBD12T cell. It can be seen from Fig. 6-(b) that the temperature variation has the largest impact on the WAT

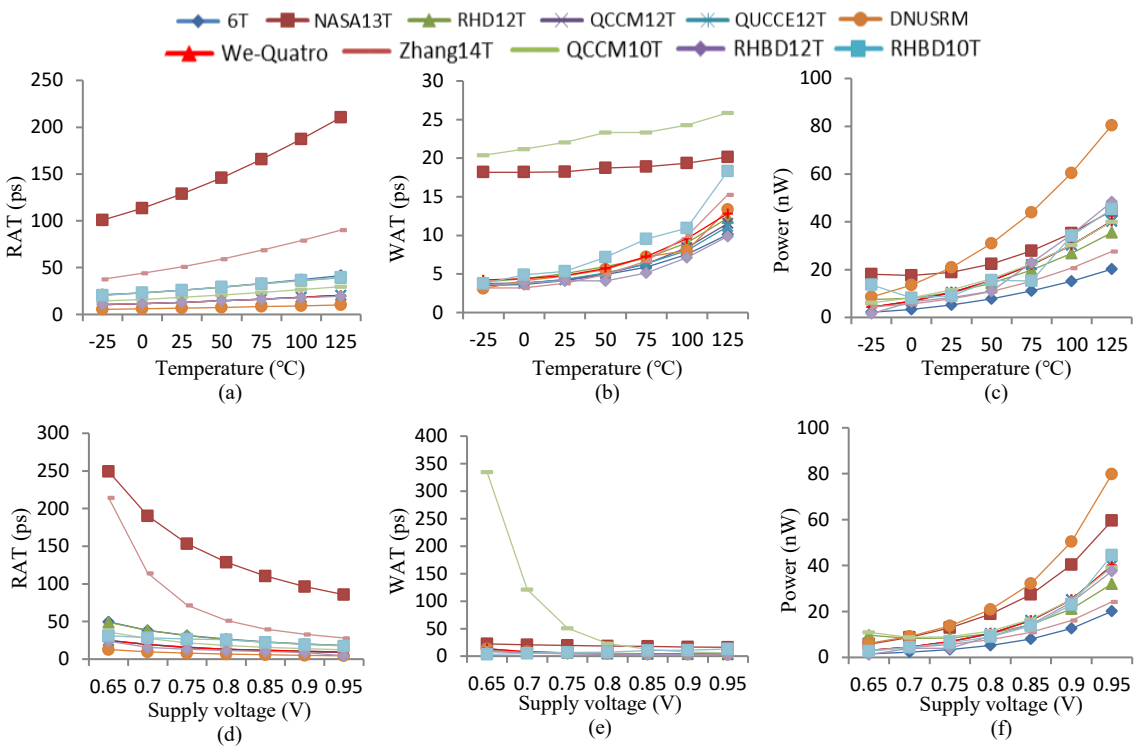

Fig. 6. Simulation results of VT variation impacts on RAT, WAT, and power for the SRAM designs. (a) Impacts of temperature variations on RAT. (b) Impacts of temperature variations on WAT. (c) Impacts of temperature variations on power. (d) Impacts of supply voltage variations on RAT. (e) Impacts of supply voltage variations on WAT. (f) Impacts of supply voltage variations on power.

of the RHBD10T cell, mainly due to the increment of WAT as the temperature rises. However, the temperature variation has a low impact on the WAT of the cells, such as the NASA13T cell and the QUCCE12T cell. It can be seen from Fig. 6-(c) that the temperature variation has a low impact on the power of the cells, such as the 6T cell, the Zhang14T cell, and the NASA13T cell, but has a large impact on the DNUSRM cell mainly due to the extra employed area to provide high reliability. When the temperature becomes very high, the proposed RHBD10T cell and the proposed RHBD12T cell are greatly affected.

It can be seen from Fig. 6-(d), (e), and (f) that the SRAM cells need to consume less RAT, WAT, and more power in general when the supply voltage rises. Indeed, large supply voltage can reduce access time of transistors but can increase power dissipation in general [8]. It can be seen from Fig. 6-(d) that the supply voltage variation has the largest impact on the RAT of the Zhang14T cell. This is because it employs many devices from its storage nodes to its output. However, the supply voltage variation has a low impact on the RAT of the other SRAM cells, such as the DNUSRM, the proposed RHBD10T, the proposed RHBD12T and the We-Quatro, mainly since any of them uses more access transistors. It can be seen from Fig. 6-(e) that the supply voltage variation has the largest impact on the WAT of the QCCM10T, mainly since it employs many devices from its storage node to its output. However, the supply voltage variation has a low impact on the WAT of the other SRAM cells, such as the proposed RHBD12T, the proposed RHBD10T, the NASA13T, and the 6T. It can be seen from Fig. 6-(f) that the supply voltage variation has a low impact on the power of the SRAM cells, such as the 6T, the proposed RHBD12T, and the proposed RHBD10T, but has a large impact on the DNUSRM cell, mainly due to the indispensable employed area to provide high reliability.

In summary, the RHBD10T cell and RHBD12T cell have low TV sensitivities in terms of RAT and WAT, but have high VT sensitivities in terms of power except the DNUSRM cell, compared with the state-of-the-art hardened SRAM cells. Therefore, the proposed cells are suitable for aerospace applications that require both low-cost access operations and high reliability.

4 Conclusions

CMOS technology scaling makes modern memory cells increasingly sensitive to soft errors that include SNUs and DNUs. In this paper, first, a novel and highly reliable RHBD10T cell has been proposed. The cell is effectively hardened against SNUs and DNUs and has a low cost especially in terms of area and power consumption. Next, to reduce the read and write access time, the RHBD12T cell has been proposed. The cell has the same soft error tolerance ability compared to the RHBD10T cell and has low overhead in terms of read and write access time. The proposed cells can be effectively used in aerospace, applications, where high reliability is required.

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