Sextuple Cross-Coupled-DICE Based Double-Node-Upset Recoverable and Low-Delay Flip-Flop for Aerospace Applications

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ABSTRACT

This paper proposes a novel sextuple cross-coupled dual-interlocked-storage-cell (DICE) based double-node-upset (DNU) recoverable and low-delay flip-flop (FF), namely SCDRL-FF, for aerospace applications. The SCDRL-FF mainly consists of sextuple cross-coupled DICEs controlled by clock-gating. The use of clock-gating based DICEs significantly reduces the CLK-Q transmission delay of the SCDRL-FF. Through the redundant and interlocked clock-gating based DICEs, the SCDRL-FF can provide complete DNU recoverability. Simulation results demonstrate the DNU recoverability of the SCDRL-FF and a 65% delay reduction on average compared with the state-of-the-art hardened FFs. The low delay overhead makes the proposed SCDRL-FF effectively applicable to high-performance applications and the DNU recoverability makes the proposed SCDRL-FF also suitable for aerospace applications.

KEYWORDS

Harsh radiation, flip-flop reliability, soft error, recovery

1 Introduction

With the continuous advancement of *complementary metal-oxide semiconductor* (CMOS) technologies, the feature sizes of transistors continuously scale down. Therefore, circuits are becoming more and more susceptible to radioactive particles [1]. In space environments, the strikes of radioactive particles are the main causes of system errors commonly known as soft errors [2-3]. Soft errors are temporal errors that can upset values stored in storage circuits and generate transient voltage pulses in combinational circuits, which are called *single-node upsets* (SNUs) and *single event transients* (SETs), respectively. In particular, with the feature sizes

of transistors continuously scaling down, a radioactive particle can affect multiple storage nodes simultaneously, causing a *multiple-node upset* (MNU) due to charge sharing [4]. Soft errors can cause fatal effects to electronic devices; therefore, protecting the devices against soft errors using *radiation-hardening-by-design* (RHBD) is becoming increasingly important.

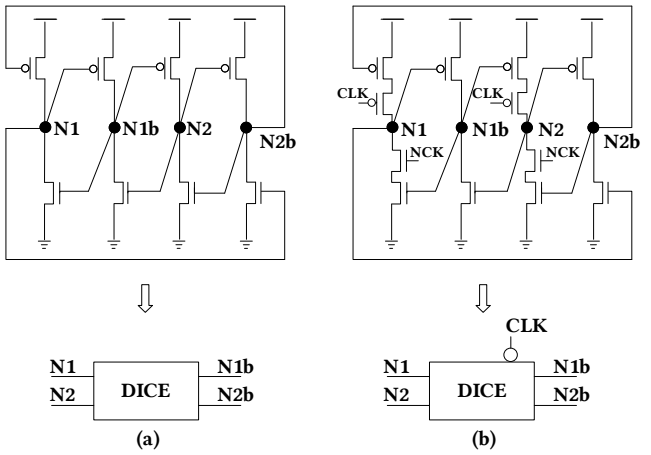

Figure 1: Structure and symbol of dual-interlocked-storage-cell (DICE). (a) Normal DICE, and (b) Clock-gating based DICE.

RHBD of SETs and MNUs, such as *triple-nod-upsets* (TNUs) and *quadruple-node-upsets* (QNUs), can lead to performance degradation and extra overhead. Therefore, this paper mainly focuses on radiation hardening against SNUs and DNUs. To tolerate SNUs and DNUs with the RHBD approach, many novel structures, such as latches [5-9], *static random-access memories* (SRAMs) [10-11] and FFs [12-18], have been proposed. Among them, DICEs are widely used [19]. Fig. 1(a) shows the schematic and the symbol of the DICE cell. A DICE cell is composed of eight transistors. The DICE cell can recover from any SNU and a part of DNUs. In particular, the DICE cell can be controllable by the *system clock* (CLK) and the *negative system clock* (NCK) signals. Fig. 1(b) shows the schematic and the symbol of the clock-gating based DICE. The clock-gating based DICE structure can switch between transparent mode and hold mode. In transparent mode (CLK = 1), N1 and N2 nodes can be used as input ports. In hold mode (CLK = 0), the clock-gating based DICE cell is equivalent to the normal DICE cell.

This paper focuses on the hardening of FFs that are mainly constructed from clock-gating based DICEs. An FF is usually composed of a master latch and a slave latch. Because conventional latches usually can be severely affected by radioactive particles, the conventional FFs composed of these latches are vulnerable to radioactive particles, which can induce SNUs and DNUs. To tolerate SNUs and DNUs with the RHBD approach, a series of FFs, such as those in [12-18], have been proposed. However, these FFs still suffer from some problems in terms of reliability and overhead issues:

(1) None of these FFs only except the DURI-FF [18] can tolerate DNUs, making most of them unsuitable for aerospace applications that require high reliability.

(2) Most of these FFs cannot recover from SNUs or DNUs. Only the DURI-FF [18] is simultaneously SNU and DNU recoverable but suffers from Problem (3).

(3) Some FFs have high power consumption as well as large delay and area overhead in tolerating SNUs and DNUs.

In order to mitigate these problems, this paper proposes a *sextuple cross-coupled-DICE based DNU recoverable and low-delay FF* (SCDRL-FF). The master/slave latch of SCDRL-FF is composed of three interlocked clock-gating based DICEs, and the clock signal connections for these latches are opposite to ensure correct logic for the SCDRL-FF. In the master latch, three common nodes of the interlocked clock-gating based DICEs are connected to the input (D) through three *transmission gates* (TGs). In the slave latch, three common nodes of the interlocked clock-gating based DICEs are connected to new TGs with opposite clock signal connections and one of the nodes is the output (Q). The proposed SCDRL-FF mainly uses the redundant and interlocked clock-gating based DICEs to realize recoverability from SNUs and DNUs. Moreover, we reduce the delay through the use of a high-speed transmission path. Simulation results show that the proposed SCDRL-FF can provide correct operations and is recoverable from any SNU and DNU. Compared with the state-of-the-art hardened FFs, the delay of the proposed SCDRL-FF structure is the smallest.

The rest of this paper is organized as follows. Section 2 introduces the schematic, working principle and recoverability verification of the proposed SCDRL-FF. Section 3 presents the comparison results. Section 4 concludes the paper.

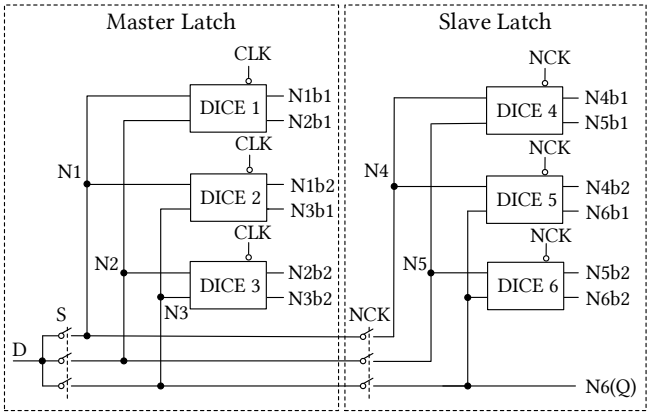

Figure 2: Schematic of the proposed SCDRL-FF.

2 Proposed SCDRL-FF

2.1 Schematic and Working Principles

Fig. 2 shows the schematic of the proposed SCDRL-FF that comprises a master latch and a slave latch. The master latch of the proposed SCDRL-FF is composed of three interlocked and clock-gating based DICEs (DICE1 to DICE3). These clock-gating based DICEs have three common nodes (N1 to N3), and three TGs marked with CLK can bridge these common nodes and the input (D) of the SCDRL-FF cell. Note that a TG marked with CLK denotes that the gate-terminal of the NMOS transistor in the TG is connected to CLK and the gate-terminal of the PMOS transistor in the TG is connected to NCK, respectively. Simultaneously, three TGs marked with NCK

from the slave latch are respectively connected to the common nodes (N1 to N3) to receive values from the master latch. Similarly, the slave latch also contains three interlocked and clock-gating based DICEs (DICE4 to DICE6) that are respectively connected to the common nodes (N4 to N6). The common node N6 is reused as the output (Q) of the SCDRL-FF cell. It can be seen that the connections of the clock-gating based DICEs in the slave latch are similar to those of the clock-gating based DICEs in the master latch, but the clock signals are opposite. In particular, the twelve redundant reverse nodes (N1b1 to N6b2) of all clock-gating based DICEs in the master/slave latch have no additional connections.

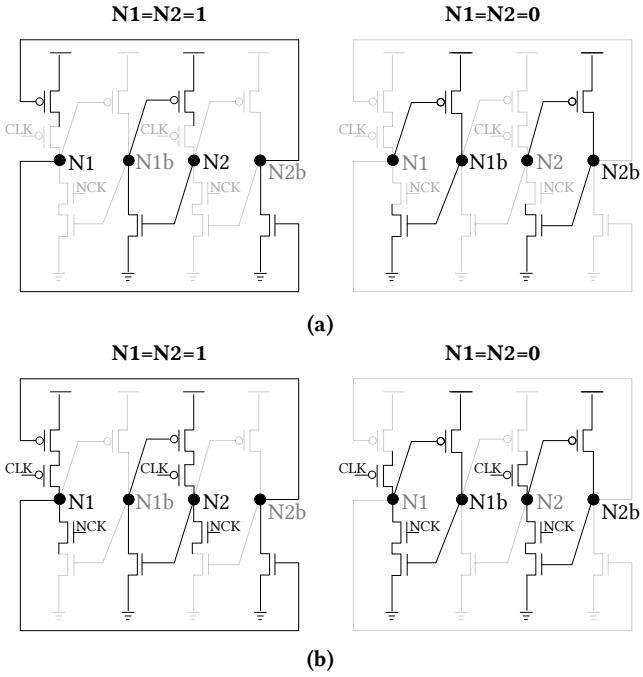

Figure 3: The clock-gating based DICE1 in the master latch. (a) DICE1 working in transparent mode (all nodes can be pre-charged), and (b) DICE1 working in hold mode.

The normal operation of the proposed SCDRL-FF is as follows:

(1) Initially, when CLK = 1, the TGs in the master latch are ON and the TGs in the slave latch are OFF. At this time, the clock-gating based DICEs in the master latch work in transparent mode. Fig. 3 (a) shows the clock-gating based DICE1 in the master latch working in transparent mode. It can be seen that the values of all nodes can be pre-charged correctly.

(2) Next, when CLK = 0, states of all TGs are switched compared to Step (1). At this time, the clock-gating based DICEs (DICE1 to DICE3) in the master latch enter the hold mode to store the pre-charged values and the DICEs in the slave latch enter the transparent mode; thus, the common nodes (N1 to N3) of the master latch can transmit values to the common nodes (N4 to N6) of the slave latch through TGs in the slave latch. Fig. 3 (b) shows the clock-gating based DICE1 in the master latch working in hold mode. It can be seen that the clock-gating based DICE working in hold mode is equivalent to the normal DICE. Therefore, the values stored in the DICEs in the master latch can propagate to the slave latch outputting through the output (Q).

(3) Subsequently, CLK returns to 1, and TGs return to the states in Step (1). Therefore, the slave latch is independent of the master latch once again. At this time, the master latch returns to the transparent mode and receives the new value of the input (D). Meanwhile, the clock-gating based DICEs in the slave latch return to the hold mode to store the value received from the master latch in Step (2), and the values stored in the DICEs in the slave latch can output through the output (Q).

(4) Finally, the CLK returns to 0 once again to accomplish the operations in Step (2). Therefore, the above steps demonstrate the correct sequential operations of the proposed FF.

Fig. 4 shows the simulation results of the normal operation of the proposed SCDRL-FF. All simulations in this paper used the Synopsys HSPICE tool with 22nm CMOS technology. The supply voltage was set to 0.8V and the working temperature was set to 25 ℃. The following operations can be seen from Fig. 4.

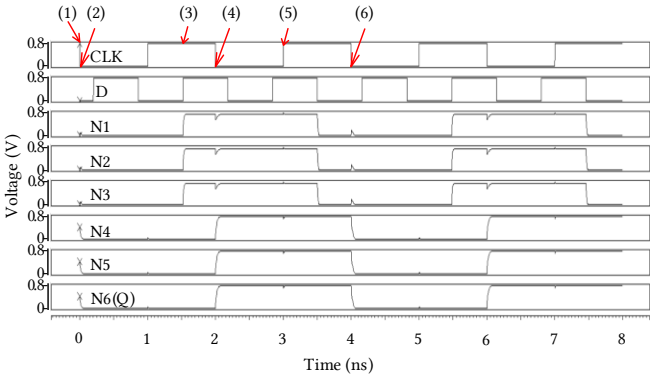

Figure 4: Simulation results for normal operations of the proposed SCDRL-FF.

(1) Initially, when CLK = 1, the SCDRL-FF can be initialized and thus all nodes in the master latch are pre-charged according to the value of D.

(2) When CLK switches to 0, the master latch stores the pre-charged D value in Step (1), and the slave latch receives this value.

(3) When CLK switches to 1, the master latch receives the new value of the input (D). At this time, the common nodes of the master latch change along with the D-value because the master latch works in transparent mode (the final D-value in this step is 1). The common nodes of the slave latch do not change along with the D-value because the slave latch works in hold mode and the previous D-value in Step (2) is stored in the slave latch.

(4) When CLK switches to 0, the master latch stores the final D-value in Step (3) and outputs this D-value to the slave latch that works in transparent mode.

(5) Then, when CLK switches to 1, the FF can finish the operations as in Step (3).

(6) Finally, when CLK switches to 0, the FF can finish the operations as in Step (4).

Therefore, the proposed SCDRL-FF can output the D-value stored in the slave latch only at the falling edge of the CLK signal. The simulation results clearly show that the normal operations of the proposed SCDRL-FF are correct.

2.2 Recoverability Principles

The recoverable principles for SNUs and DNUs of the proposed SCDRL-FF are discussed as follows. As mentioned above, a DICE is fully recoverable from any SNU. Therefore, the interlocked DICEs in the master latch and the slave latch are fully recoverable from any SNU when they work in hold mode. Note that, the constructions of the master latch and the slave latch are equivalent so that only one latch needs to be considered when discussing the recoverability from DNUs. We mainly discuss the recoverability from DNUs of the slave latch when it works in hold mode. There are five possible cases discussed as follows.

Case 1: A DNU affects two common nodes (e.g., node-pair <N4, N5>). In this case, DICE4 suffers from a DNU and it cannot self-recover from the DNU in the worst case. However, DICE5 and DICE6 only suffer from an SNU, respectively. Therefore, DICE5 and DICE6 can recover from the SNU so that all nodes can return to the correct states. Therefore, the latch/FF can recover from this kind of DNUs and Q is still correct.

Case 2: A DNU affects two non-common nodes in two clock-gating based DICEs (e.g., node-pair <N4b1, N4b2>). This type of DNUs is equivalent to the case that two SNUs respectively affect two clock-gating based DICEs that can recover from any SNU. Therefore, the latch/FF can recover from this kind of DNUs and Q is still correct.

Case 3: A DNU affects two nodes in a clock-gating based DICE (e.g., node-pair <N4b1, N5b1>). In this case, DICE4 suffers from a DNU and it cannot self-recover from the DNU in the worst case. However, DICE5 and DICE6 are not impacted so that N4 and N5 are always correct. Thus, the transient error (DNU) in DICE4 can be removed by correct N4 and N5. Therefore, the latch/FF can recover from this kind of DNUs and Q is still correct. Note that this case is similar to Case 1.

Case 4: A DNU affects a common node and a non-common node in a clock-gating based DICE (e.g., node-pair <N4, N4b1>). In this case, DICE4 suffers from a DNU and it cannot self-recover from the DNU in the worst case. However, DICE5 only suffers from an SNU and DICE6 has all correct node states. Thus, SNU-recoverable DICE5 and DICE6 can still feed correct values to DICE4. Then, the transient error (DNU) in DICE4 can be removed by correct N4 from DICE5 and N5 from DICE6. Therefore, the latch/FF can recover from this kind of DNUs and Q is still correct.

Case 5: A DNU affects a common node of two clock-gating based DICEs and a non-common node in another clock-gating based DICE (e.g., node-pair <N4b1, N6>). This case is equivalent to the case that each DICE suffers from an SNU so that each DICE can self-recover. Therefore, the latch/FF can recover from this kind of DNUs and Q is still correct.

Fig. 5 shows the simulation results of all representative DNU injections for the above-mentioned cases (Case 1 to Case 5) for the slave latch of the proposed SCDRL-FF. In all the above simulations, we used a controllable double exponential current source model to perform all the DNU injections [20]. The worst-case injected charge was up to 45fC. The time constants of the rise and fall of the current pulse were set to 0.1 ps and 3.0 ps, respectively. It can be seen from Fig. 5 that, during 2ns and 3ns, when Q=1, a DNU was respectively injected to node-pairs <N4, N5>, <N4b1, N4b2>, <N4b1, N5b1>, <N4, N4b1> and <N4b1, N6>. Moreover, during 4ns and 5ns, when Q=0, the reversed DNUs were respectively injected into these node-pairs. It can be seen from Fig. 5 that the node-pairs with injected charge can recover from all these DNUs. In summary, simulation results validate the DNU recoverability of the proposed SCDRL-FF and thus the proposed SCDRL-FF can also recover from SNUs.

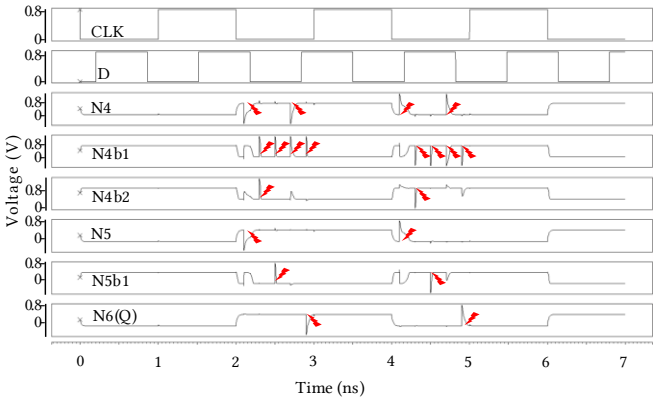

Figure 5: Simulation results of all indicative DNU injections for the slave latch of the proposed SCDRL-FF.

3 Comparison Results

To make a fair and comprehensive comparison with typical state-of-the-art FFs, such as the *traditional unhardened FF* (TUFF) [12], the triple-modular-redundancy (TMR)-based TMR-FF [13], the HPST-FF [14], the DRRH-FF [13], the Quatro-FF [15], the DNUR-FF [16], the DICE-FF [17] and the DURI-FF [18], the same simulation conditions described above were used (the same transistor sizes, supply voltage and working temperature).

TABLE 1: Reliability comparison results among the FFs.

Flip-Flops	SNU Tolerant	SNU Recoverable	DNU Tolerant	DNU Recoverable
TUFF [12]	×	×	×	×
TMR-FF [13]	√	×	×	×
HPST-FF [14]	√	×	×	×
DRRH-FF [13]	√	×	×	×
Quatro-FF [15]	√	×	×	×
DNUR-FF [16]	√	×	×	×
DICE-FF [17]	√	√	×	×
DURI-FF [18]	√	√	√	√
SCDRL-FF (Proposed)	√	√	√	√

Reliability comparison results are shown in Table 1. It can be seen that the TUFF cannot provide node-upset tolerance in the presence of an SNU or a DNU. This means that the output of the TUFF can change due to at least an SNU. The TMR-FF, HPST-FF, DRRH-FF, Quatro-FF and DNUR-FF can tolerate SNUs. They use multiple redundancy technologies to provide SNU tolerance but cannot provide SNU recoverability. In other words, the impact of SNUs still exists in these FF circuits. The DICE-FF is SNU-tolerant

and SNU-recoverable but there is still at least one counterexample that it cannot tolerate a DNU. The DURI-FF and the proposed SCDRL-FF are recoverable from any SNU and DNU. Therefore, the DURI-FF and the proposed SCDRL-FF can provide a higher level of robustness but the DURI-FF consumes a large delay and high power that will be discussed in the following.

TABLE 2: The overhead comparison results among the FFs, in terms of delay, power, area and DPAP.

Flip-Flops	Delay (ps)	Power (μW)	10^2×Area (μm^2)	DPAP
TUFF [12]	17.23	0.84	2.97	0.43
TMR-FF [13]	45.41	2.47	9.80	10.99
HPST-FF [14]	23.00	1.16	8.02	2.14
DRRH-FF [13]	43.01	1.26	5.94	3.22
Quatro-FF [15]	38.99	3.68	6.14	8.81
DNUR-FF [16]	42.39	2.19	11.29	10.48
DICE-FF [17]	17.19	1.30	5.64	1.26
DURI-FF [18]	20.17	4.59	11.58	10.72
SCDRL-FF (Proposed)	10.68	2.42	12.47	3.22

Table 2 shows the overhead comparisons among these FFs, in terms of delay, power dissipation, silicon area and *delay-power-area product* (DPAP). In Table 2, "Delay" means CLK to Q transmission delay, i.e., the average of rising and falling delays from CLK to Q. "Power" means the average of dynamic and static power dissipation. "Area" means the area of silicon measured by the method in [18]. "DPAP" means the delay-power-area product calculated by multiplying the delay, power, and area to comprehensively evaluate the overhead of these FFs. Obviously, a lower DPAP represents a lower comprehensive overhead of an FF design.

Qualitative delay overhead comparison results are shown in Table 2. It can be seen from Table 2 that the proposed SCDRL-FF has the lowest transmission delay overhead from CLK to Q. This is mainly because the other designs usually set the node in the last level of the slave latch as the output port, thus there are more transistors from TGs to the output for them. Since the SNU/DNU recoverability of the proposed FF is implemented by the interlocked clock-gating base DICEs, no extra devices between TGs and the output are needed. Thus, the common nodes of the clock-gating based DICEs in the master latch of the proposed SCDRL-FF directly feed the common nodes in the slave latch, and a common node in the slave latch can be used as the output port to reduce delay. Simultaneously, when the master latch transmits the D-value to the slave latch, the transparent mode of the clock-gating based DICEs in the master latch can ensure the scenario that the slave latch cannot affect the master latch due to the clock-gating.

Qualitative power overhead comparison results are also shown in Table 2. It can be seen that the proposed SCDRL-FF consumes lower power when compared to the same-type DURI-FF. This is mainly because the proposed SCDRL-FF employs clock-gating technology for all DICEs. In transparent mode, the clock-gating based DICEs cannot generate any feedback loops or current completion, resulting in lower power dissipation. Meanwhile, due to the effective constructions of the master latch (and the slave latch being similar), one of the latches is in transparent mode and another latch is in hold mode at any time. Therefore, dynamic and static power dissipation of the FF is low on average. Note that, the Quatro-FF and the DURI-FF have higher power dissipation. This is mainly because they use more transistors or there is much current competition in their designs, thus they consume more power.

The area overhead comparison results are also shown in Table 2. It can be seen from Table 2 that the proposed SCDRL-FF has to consume a large area overhead to provide high reliability with low delay as well as low power. If we do not use the clock-gating for all DICEs, the area overhead can be effectively reduced but the power will increase. Therefore, the low power and high reliability features are mainly achieved at the cost of extra silicon area that is reasonable.

The DPAP comparison results are also shown in Table 2. It can be seen from Table 2 that the TUFF has the smallest DPAP mainly because its power and area are the smallest. When the provided reliability of FFs is similar, the comparison of DPAP is more convincing. Note that Table 1 shows that the TUFF cannot tolerate SNUs or DNUs and the TMR-FF, HPST-FF, DRRH-FF, Quatro-FF, DNUR-FF and DICE-FF cannot tolerate DNUs. On the contrary, the DURI-FF and the proposed SCDRL-FF are recoverable from SNUs and DNUs. The delay and power overhead of the proposed SCDRL-FF is lower than those of the DURI-FF and the area of them is similar. Therefore, the DPAP of the proposed SCDRL-FF compared with the DURI-FF is lower.

Among the compared hardened FFs, the DURI-FF and the proposed SCDRL-FF have the highest level of robustness because they can recover from any SNU and DNU but the SCDRL-FF has a small delay, low power and small DPAP. It can be calculated that the delay overhead of the proposed SCDRL-FF compared with the other hardened FFs can reduce 65.46% on average. Note that, the proposed SCDRL-FF is also compared with the DURI-FF in terms of delay, and the percentage of the reduced delay overhead is 47.05%. Meanwhile, the power dissipation of the proposed SCDRL-FF is close to the average power dissipation that is 2.19μW of the other FFs. Compared with the DURI-FF, the power dissipation of the proposed SCDRL-FF reduces 47.28%. In addition, due to the use of the extra transistors, the area overhead of the proposed SCDRL-FF is higher than the other FFs. In summary, the proposed SCDRL-FF compared with the typical state-of-the-art FFs not only provide high reliability but also reduce delay and power dissipation at the cost of silicon area.

4 Conclusions

This paper has proposed a novel DNU recoverable FF design, namely SCDRL-FF, that provides high reliability with low delay. The master latch of the proposed SCDRL-FF can directly transmit values to the output through only a transmission gate when the slave latch switches into transparent mode. The clock gating in the master/slave latches can reduce current competition in the FF to efficiently reduce power consumption. The low delay makes the SCDRL-FF effectively applicable to high-performance applications and the DNU recoverable feature makes the FF also applicable to

aerospace applications. Simulation results demonstrate the DNU recoverability and low delay of the proposed SCDRL-FF.

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