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***Abstract*—With technology scaling down, the vulnerability of circuits to radiation and the increase of static power have become severe concerns. Spintronic devices such as magnetic tunnel junction (MTJ) have been developed to cope with many concerns, among which reliability concerns [1]. Spintronic devices have attractive properties, such as non-volatility and compatibility with conventional CMOS fabrication process. Based on an advanced triple-path dual-interlocked-storage-cell (TPDICE) and MTJs, this paper proposes a radiation-hardened non-volatile magnetic latch, namely M-TPDICE, that can completely tolerate single-node upsets (SNUs) and double-node upsets (DNUs). Simulations of the proposed latch with the HSPICE tool with a 45 nm CMOS technology model have demonstrated the effectiveness of the proposed latch.**

***Index Terms*—**Magnetic tunnel junction, soft error, robust computing, spin transfer torque.

I. Introduction

CMOS technology scaling can improve integration and performance for integrated circuits and systems. However, with the shrinking of transistor feature sizes, CMOS devices have become more and more vulnerable to soft errors that can severely cause data corruptions, execution failures, or even system crashes in the worst case. Soft errors are transient errors caused by the strike of radiative particles, such as protons and neutrons. When a particle collides with an OFF-state transistor of an integrated circuit, it can flip the value of a node and induce an SNU. Due to charge-sharing [2], DNUs can be caused when a high energy particle simultaneously impacts two OFF-state transistors. However, non-volatile (NV) magnetic memories using spintronic technologies, such as spin-transfer torque (STT) and spin orbit torque (SOT), are promising alternatives to overcome the limitations of conventional CMOS-based circuits. NV magnetic memories have various advantageous features, such as high endurance, scalability, high density, low access latency, and soft error immunity [3]. In such spintronic technologies, MTJ cells are used as storing devices, which store logic values as resistive states.

As the fundamental device of spintronic circuits, MTJs play a significant role in the radiation hardening and the non-volatility of these circuits [4]. As shown in Fig. 1, an MTJ is comprised of two ferromagnetic layers. The top layer is called the free layer (FL), which is typically made of the CoFeB material [5]. The MgO dielectric layer in the middle is called the tunnel barrier (TB), which is ultrathin [5]. The bottom ferromagnetic layer is referred to as the pinned layer (PL). With the fixed magnetization in PL as a reference, the magnetization in FL is either parallel (P state) or anti-parallel (AP state) to that of PL. Note that, the resistance of an MTJ in the AP state is higher than that in the P state.

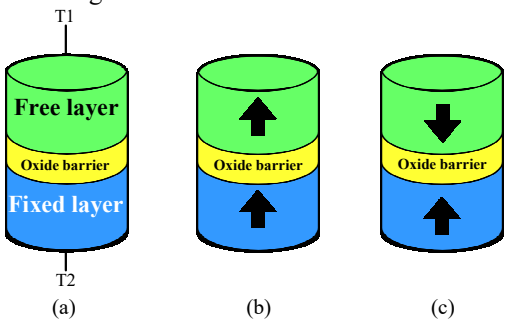

Fig. 1. MTJ device and its states. (a) MTJ device structure. (b) P state. (c) AP state.

In this paper, based on the aforementioned features of the MTJ, a radiation-hardened NV magnetic latch, namely M-TPDICE, is proposed. The proposed latch offers complete SNU and DNU hardening, high performance, and non-volatility. The non-volatility is achieved by MTJs which facilitate zero static power without missing information in the power-off state.

The rest of the paper is organized as follows. Section II introduces backgrounds on spintronic, MTJ-based circuits and some previous works. Section III presents a radiation-hardened NV magnetic latch, namely M-TPDICE. Simulation results will be presented and discussed in Section IV to verify the functionality of the proposed latch. Finally, Section IV concludes the paper.

II. Backgrounds

A. Spintronic

Field-induced magnetization switching (FIMS), thermally assisted switching (TAS), STT, spin hall assisted STT (SHA-STT), and voltage-controlled magnetic anisotropy (VCMA) are typical approaches to write data into MTJs [4, 6-9]. FIMS and TAS have high power consumption and instability [4, 6]. SHA-STT needs extra current-flow, which increases routing complexity [8]. VCMA needs high voltage, which can decrease MTJ lifetime [9]. STT has been widely adopted because of lower current and data disturbance than the other ones [10].

The tunneling magneto-resistance (TMR) effect and STT can provide read and write mechanisms for MTJ devices. The resistance of MTJ devices depends on the thickness of TB and

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the relative direction of magnetization in FL and PL. The resistance can be relatively low when MTJ devices is in the P state, as shown in Fig. 1(b). When MTJ devices is in AP state, as shown in Fig. 1(c), the resistance can be relatively high. This phenomenon is well known as the TMR effect [11]. The TMR ratio, which can be defined by TMR = (R_{AP} - R_P) / R_P, where R_{AP} and R_P are the resistance values of AP and P states, is the portrayal of that phenomenon.

MTJ devices use the STT effect to write values. In order to switch the states of MTJ devices between AP and P, a spin-polarized current is needed to pass through the MTJ. When the current passes through the MTJ and is larger than the critical switching current (CSC), the magnetization in the FL will switch to the correct state, which depends on the direction of the current. In [12], CSC is a key electrical parameter, defined as the current to switch the states of MTJ devices within a period of time and at zero temperature.

B. Previous Works

Several existing techniques for NV latch designs are shown in Fig. 2. As shown in Fig. 2(a), reference [13] proposed a magnetic random-access memory (MRAM) latch, which mainly comprises four modified C-elements (MCEs) to tolerate SNUs. Each MCE comprises six transistors, e.g., the left-top six transistors in the latch. Note that original C-elements are shown in [14]. By storing two copies of the stored values, the latch can improve its robustness and implement the NV feature.

As shown in Fig. 2(b), the design proposed in [15] is mainly composed of two inverters, two parallel CEs (in the dotted rectangle), some signal-controlled transistors and a pair of complementary MTJs. The CEs provide the soft-error tolerance and the MTJs provide the NV feature. However, the internal nodes of the design are direct inputs of the MTJ cells in the backup operation, resulting in large delay. To mitigate the drawbacks of the design in [15], the design proposed in [16] does not use peripheral circuits and additional control signals. However, this design cannot provide any DNU hardening.

To reduce the number of CMOS transistors, as shown in Fig. 2(d), the design in [18] does not use inverters as the design in [16]. However, the design suffers from high power consumption and large D-Q delay. Moreover, the design cannot provide any DNU tolerance. By using seven 3-input CEs, the design in [19] can provide the DNU tolerance. However, it uses

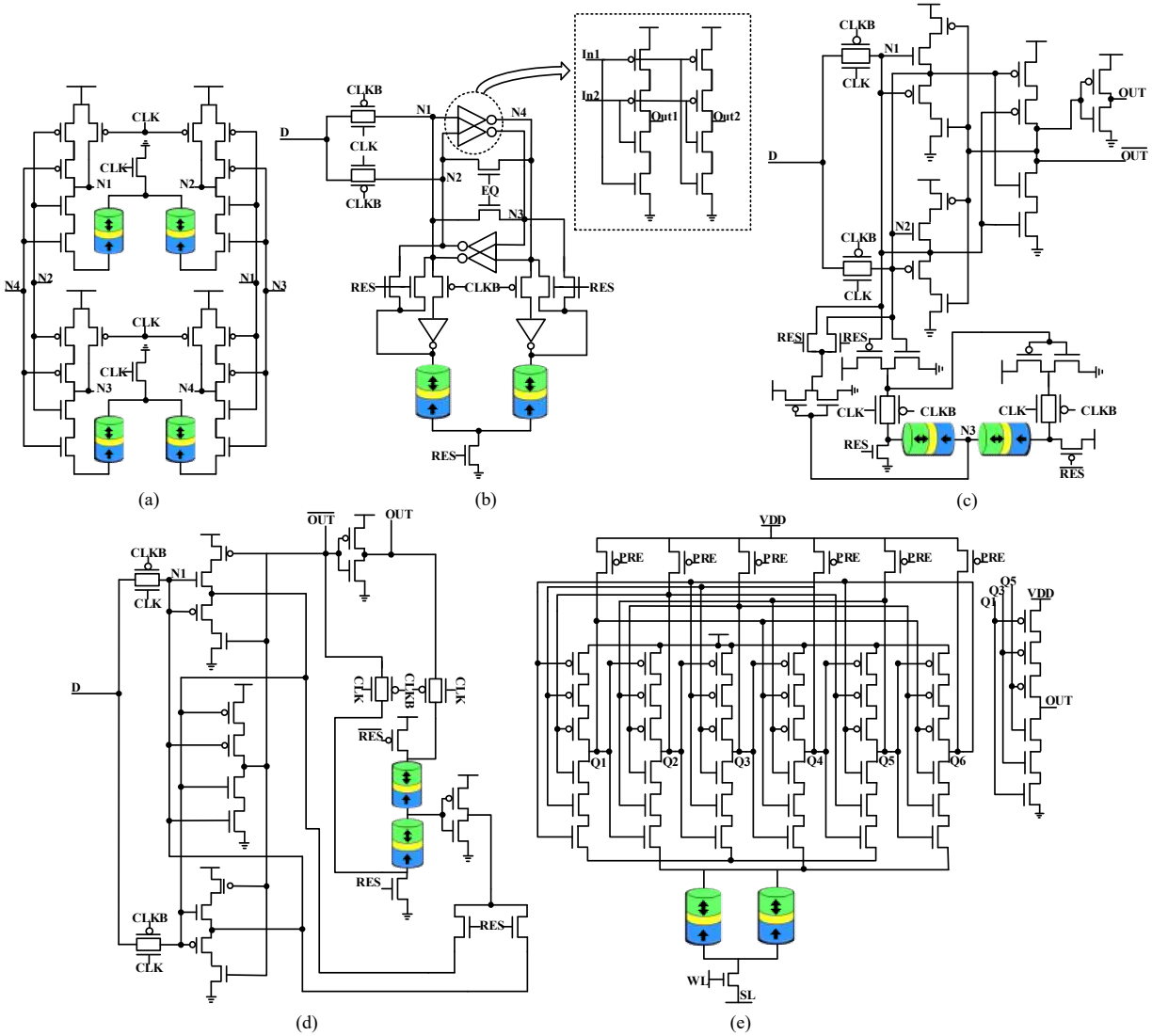

Fig. 2. Previous NV magnetic latches. (a) Design in [13], (b) design in [15], (c) design in [16], (d) design in [18] and (e) design in [19].

many transistors and cannot provide the backup operation. Note that values cannot be written into MTJs for designs in [13, 19]. To provide the backup operation for them, we can modify the design in [13] by adding transmission gates (TGs) so that N1 and N3 can be initialized by D and N1-N4 can be connected to the FL of MTJs through TGs. We can also add TGs in [19] so that N1, N3 and N5 can be initialized by D and N1-N6 can be connected to the FL of MTJs through TGs.

III. Design of the Proposed NV Latch

Figure 3 shows the proposed radiation-hardened NV magnetic latch. The latch mainly comprises TGs, an improved TPDICE (the original version of TPDICE is in [22]), a pair of MTJ cells, and a clock-gating (CG) based 3-input CE (see the left-bottom device in Fig. 3 and its transistor-level structure is just the first column of transistors in Fig. 2(e)). The output Q of the CG-based CE, which is fed by N2, N4 and N6, is the output of the proposed latch. In this latch, D is the input, N1 to N6 are the internal nodes, CLK is the system clock, CLKB is the negative system clock, and PRE and RES are signals used for the restore operations, respectively. The advantages of the proposed latch include radiation hardening and non-volatility, which will be discussed in the following.

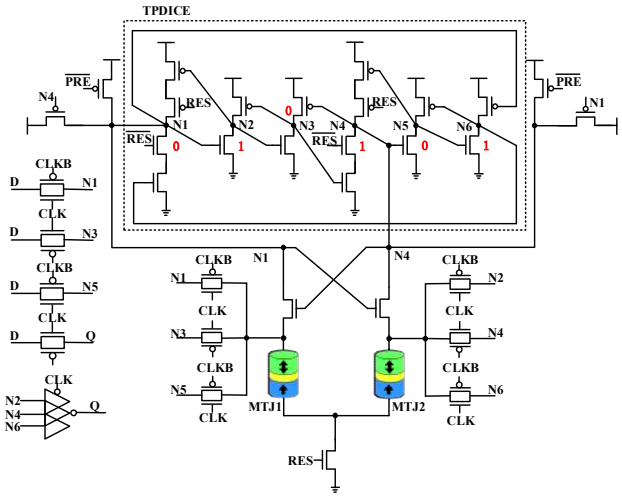

Fig. 3. Schematic of the proposed radiation-hardened NV latch.

A. Radiation Hardening

The error-free operations in transparent mode and hold mode as well as the fault tolerance against SNUs and DNUs of the proposed latch are described in the following. Note that the transisters controlled by RES and $\overline{\text{RES}}$ are ON to construct feedback loops so as to provide radiation hardening capability.

(1) Error-free Operations

When CLK = 1 and CLKB = 0, the latch works in transparent mode. In this mode, all transistors in TGs are ON and N1, N3, N5, and Q can be initialized by D through the TGs (TG1 to TG4). Moreover, the resistance of MTJ1 and MTJ2 can be initialized by N1-N6. Therefore, the latch can properly work in transparent mode.

When CLK = 0 and CLKB = 1, the latch works in hold mode. In this mode, all transistors in TGs are OFF, and Q can only be driven by N2, N4 and N6. Since the internal nodes of the TPDICE feed each other, the feedback loops in the TPDICE can be properly constructed to hold stored values. Therefore, the proposed latch can properly store values and can output the stored values through Q.

(2) Fault Tolerance

It should be noted that Q and N1-N6 are sensitive to node-upsets in the proposed latch. The state shown in Fig. 3, i.e., N1 = N3 = N5 = Q = 0, and N2 = N4 = N6 = 1, is selected as an example for fault-tolerance discussion. First, the SNU tolerance of the proposed latch is discussed.

When any internal node in the TPDICE is affected by an SNU, the node can recover to its correct state. For example, when N1 is affected by an SNU, N1 temporarily flips to "1". At this time, the error cannot propagate to N6 because the PMOS transistor above N6 becomes OFF. Meanwhile, N1 = 1 can temporarily turn on the NMOS transistor below N2, causing N2 to output a weak "1". N3-N6 are not directly affected by the flip of N1, allowing them to keep their correct values. N3 is still correct and the PMOS transistor above N2 is still ON so that N2 has a strong value "0". Clearly, the strong "1" of N2 can neutralize the weak "0" so that the value of N2 is still "1". Because N2 and N6 are correct, N1 can return to its correct value (N2 = 1 so that the PMOS transistor above N1 is OFF; N6 = 1 so that the NMOS transistor below N1 is ON). Therefore, N1 can recover when it is affected by an SNU. In a similar way, N2-N6 can also recover when any of them is affected by an SNU.

On the other hand, when Q is affected by an SNU, the values of the internal nodes in TPDICE are still correct. This means that the inputs of the CE are correct so that Q can return to its correct value. Therefore, the nodes in the proposed latch can self-recover from SNUs. In other words, the latch is completely SNU-hardened.

In the following, the DNU tolerance of the proposed latch is discussed. Due to the symmetry of the latch structure, only three possible cases (i.e., Case 1 to Case 3) are needed to be discussed as follows.

Case 1: The output Q and one node in the TPDICE are affected by a DNU and the key node-pairs are <N1, Q> and <N2, Q>. When <N1, Q> is affected by a DNU, the temporary flip of N1 can be immediately removed since the internal nodes of TPDICE can self-recover from any SNU (as explained above). Meanwhile, the output Q can still return to its correct value since all inputs (N2, N4 and N6) of the CG-based CE still have their correct values. Therefore, <N1, Q> can self-recover from the DNU. Similarly, <N2, Q> can also self-recover from the DNU. Therefore, the latch is completely DNU-hardened for Case 1.

Case 2: The output Q is not affected by a DNU and only one input of the CG-based CE is affected by a DNU. <N1, N2> and <N2, N5> are representative node-pairs. When <N1, N2> is affected by a DNU, N1 flips to "1" and N2 flips to "0" so that the PMOS transistor above N1 and the NMOS transistor below N2 are temporarily ON. Thus, N1 can output a weak "1" and N2 can output a weak "0". At this time, the PMOS transistor

above N6 and the NMOS transistor below N3 are OFF so that the error cannot propagate to N3 and N6. Thus, N3-N6 are not directly affected by N1 and N2 so that they can still remain their correct values. This means that, the NMOS transistors below N1 and the PMOS transistor above N2 are ON so that N1 can output a strong "0" and N2 can output a strong "1". Clearly, the strong "0" of N1 can neutralize the weak "1" so that the value of N1 is still "0"; the strong "1" of N2 can neutralize the weak "0" so that the value of N2 is still "1". Therefore, the node-pair <N1, N2> can recover when it is affected by a DNU.

When <N2, N5> is affected by a DNU, N2 flips to "0" and N5 flips to "1". At this time, the NMOS transistor below N3 and the PMOS transistor above N4 are OFF so that the error cannot propagate to N3 and N4. Meanwhile, the PMOS transistor above N1 and the NMOS transistor below N6 are ON so that N1 can output a weak "1" and N6 can output a weak "0". N1, N6 and N3-N4 are not directly affected by N2 and N5. This means that, N1 has its correct value "1" and N6 has its correct value "0". Thus, the NMOS transistor below N1 and the PMOS transistor above N6 are ON so that N1 has a strong "0" and N6 has a strong "1". Clearly, the strong "0" can neutralize the weak "1" so that the value of N1 is still "0"; the strong "1" can also neutralize the weak "0" so that the value of N6 is still "1". Therefore, N1, N3, N4 and N6 still have their correct values. Because N1 and N3 are correct, N2 can return to its correct value (N1 = 0 so that the NMOS transistor below N2 is OFF; N3 = 0 so that the PMOS transistor above N1 is ON). Because N4 and N6 are correct, N5 can return to its correct value as well. Therefore, the node-pair <N2, N5> can tolerate the DNU. In other words, the latch is completely DNU-hardened for Case 2.

Case 3: Any two inputs of the CG-based CE are affected by a DNU. Due to the symmetric structure of the latch, the key node-pair is only <N2, N4>. When <N2, N4> is affected by a DNU, N2 and N4 flip to "0". At this time, the PMOS transistor above N3 is ON and the NMOS transistor below N3 is OFF so that N3 flips to "1". Meanwhile, the PMOS transistors above N1 are ON and the NMOS transistors below N5 is OFF. N5 still has its previous correct value "0" since the PMOS transistor above N5 is OFF. The value of N4 is uncertain (the voltage of the node is higher than GND but lower than VDD) since the PMOS transistors above N4 and the NMOS transistors below N4 are ON. The value of N1 is uncertain since the PMOS transistor above N1 and the NMOS transistor below N1 are ON. However, N6 can still have its correct value "1" since the NMOS transistor below N6 is OFF. The output (i.e., node Q) of the CG-based CE can remain its correct value since the inputs of the CE cannot simultaneously be flipped. As a result, <N2, N4> can tolerate the DNU. Therefore, the proposed latch is completely DNU-hardened for Case 3. In summary, the proposed latch is completely SNU/DNU hardened.

B. MTJ-based Non-volatility

For the proposed latch, the basic operations of the non-volatility include two states (backup and restore). Note that, when the latch works in backup operation, RES = 0, $\overline{\text{RES}}$ = 1 and $\overline{\text{PRE}}$ = 1; when it works in restore operation, RES = 1, $\overline{\text{RES}}$ = 0 and $\overline{\text{PRE}}$ = 0.

(1) Backup Operation

When the proposed latch design works in transparent mode (CLK = 1), the D value is directly transferred to the output through the TG. Meanwhile, the copy of the D value is also stored in the MTJs by the current flow and the backup can be completed. For example, when N1 = N3 = N5 = 0 and N2 = N4 = N6 = 1, the state of MTJ1 is P and the state of MTJ2 is AP because the current-flow is from the FL of MTJ2 to the FL of MTJ1. Note that, we use three nodes (e.g., N1, N3 and N5 converged to the node above MTJ1) instead of one node to cause a higher current so that the state of MTJs can be effectively switched [12].

(2) Restore Operation

The powered-off VDD turns all the transistors into OFF. After the VDD power-on, the circuit enters into the restore operation. When $\overline{\text{PRE}}$ = 0, the nodes N1 and N4 can be charged by PMOS transistors (i.e., N1 = N4 = 1). At the same time, RES = 1 and $\overline{\text{RES}}$ = 0, indicating that the nodes N1 and N4 will not be changed by the other nodes in the TPDICE, and thus the PL of MTJ1 and MTJ2 connect to the ground. Since the MTJ in the P state has lower resistance than that in the AP state, the node connected to the MTJ in the P state is discharged faster than the node connected to the MTJ in the AP state. Therefore, the logic value of N1 and N4 will be different.

For example, when MTJ1 is in the P state and MTJ2 is in the AP state, the resistance of MTJ1 is much lower than that of MTJ2. When the latch works in the restore operation (N1-N6 have no values), $\overline{\text{PRE}}$ = 0 so that N1 = N4 = 1. At this time, because the transistors directly controlled by RES and $\overline{\text{RES}}$ are OFF, N1 and N4 cannot be impacted by other nodes in the TPDICE. Meanwhile, the NMOS transistors connected to MTJs are ON since N1 = N4 = 1 and RES = 1. N1 discharges faster than N4 because the resistance of MTJ1 is much lower than that of MTJ2 (MTJ1 is in the P state and MTJ2 is in the AP state). Thus, N1 = 0 and N4 = 1. Meanwhile, the PMOS transistor above N6 and the NMOS transistor below N5 are ON so that N5 = 0 and N6 = 1. Moreover, the PMOS transistor above N3 is OFF so that the value of N3 will become "0" in a short time. The NMOS transistor below N2 is OFF and the PMOS transistor above N2 is ON when the value of N3 becomes "0". Thus, the value of N2 becomes "1". Therefore, the values of N1, N3 and N5 are "0" and the values of N2, N4 and N6 are "1". Thus, the output (i.e., node Q) of the CG-based CE becomes "0" since the inputs of the CE (i.e., N2, N4 and N6) have the same value "1". Therefore, the states of output Q and N1-N6 reload the original states, meaning that the restore operation is finished.

IV. Simulation Results

The proposed latch was implemented in a 45nm CMOS technology and the MTJ model proposed in [21] was used. The 1.0V supply voltage and the room temperature were assumed.

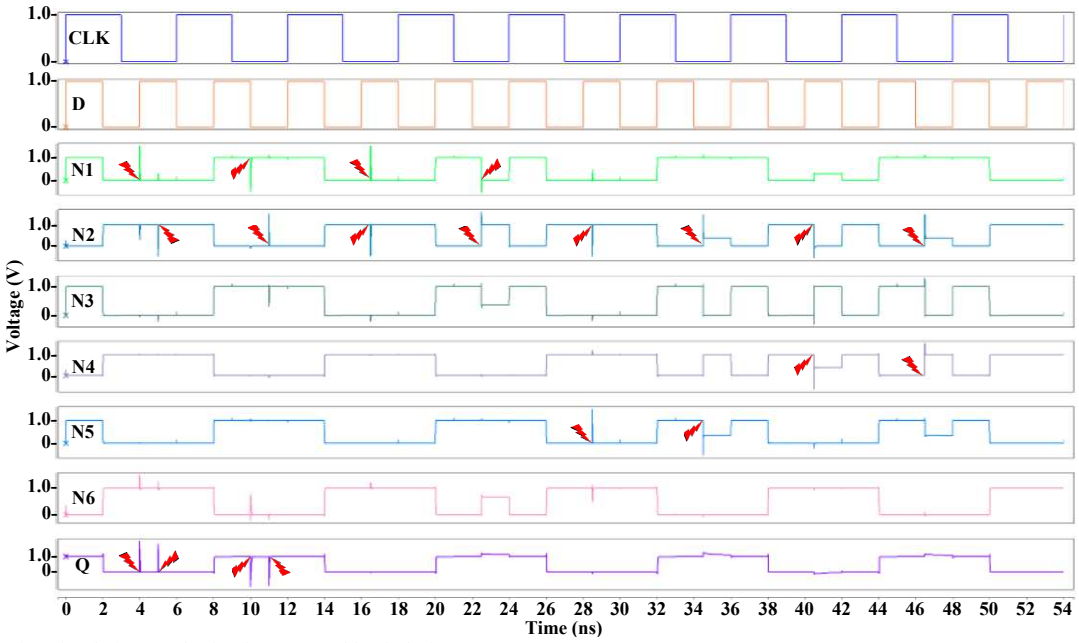

Fig. 4. DNU-injection simulation results for the proposed latch design.

As in [1, 17], pertinent simulations using Synopsys HSPICE were conducted.

A. DNU Hardening

Figure 4 shows the simulation results of DNU injections in the proposed latch. It can be seen that, at 4ns, a DNU was injected to <N1, Q>; at 5ns, a DNU was injected to <N2, Q>; however, the injected DNUs only resulted in narrow pulses and the node-pairs returned to the correct states quickly. At 17ns, a DNU was injected to <N1, N2>; at 29ns, a DNU was injected to <N2, N5>; at 41ns, a DNU was injected to <N2, N4>; however, the injected DNUs had no impact on Q. In other words, the injected DNUs cannot flip Q. Therefore, the simulations demonstrate the DNU tolerance of the proposed latch.

B. Normal and Restore Operations

Figure 5 shows the simulation results for normal and restore operations of the proposed latch. The latch worked in normal operation when VDD = 1, PRE = 0 and RES = 0. It can be seen that, at 39ns (before CLK fell to 0), the latch was in transparent mode; Q was initialized by D (Q = D = 0) and the copy of D value was stored into MTJs (MTJ1 was in the P state and MTJ2 was in the AP state) to complete the backup. It can also be seen that, at 41ns (after CLK went back to 0), the latch was in hold mode; the value of Q still remains at the value initialized by D in previous transparent mode.

Moreover, it can be seen that, at 120ns, the latch was powered-off (VDD = 0) and the output was 0. However, the output did not have its correct value before VDD was powered-on at 200ns. After applying the restore signals, correct data can be transferred from the MTJs to the TPDICE and the values of all nodes in the latch became correct again. Therefore, the simulations demonstrate the correct operations of the proposed latch.

C. Comparison Results

Table I shows the reliability and overhead comparison results among the radiation-hardened NV magnetic latches. It can be seen from Table I that only the proposed latch and the latch in [19] are completely SNU and DNU tolerant. Hence, the proposed latch is more reliable than the latches that can only provide SNU tolerance. Note that, "Backup Ability" means the ability to store the copy of the D value into MTJs, and "Restore Ability" means the ability to transfer the values stored in MTJs to the latch.

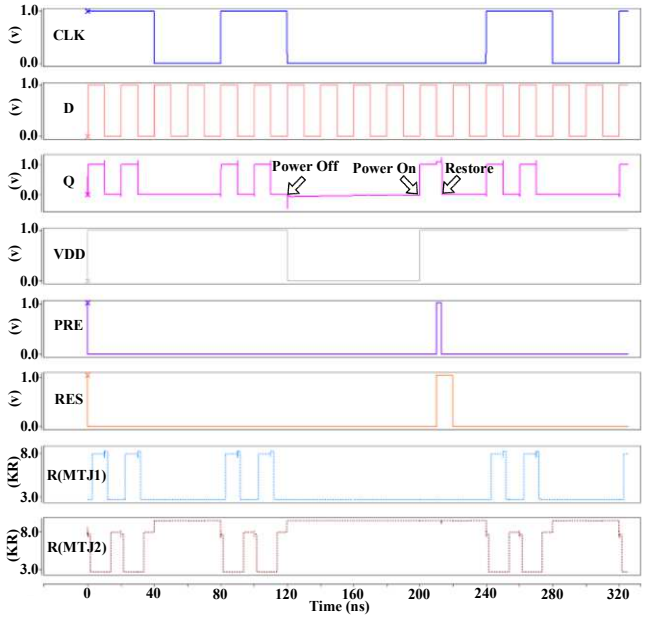

Fig. 5. Simulation results of the proposed latch during nomal and restore operations. Note that, at 39ns, the copy of D value was stored into MTJs (MTJ1 was in P state and MTJ2 was in AP state) to complete the backup.

Now we discuss the overhead comparison results among the latches. In Table I, "D-Q Delay" means the average of the transmission delays (rise and fall) from D to Q, "CMOS Area" means the silicon area measured as in [20], "Power" means the

TABLE I
RELIABILITY AND OVERHEAD COMPARISON RESULTS AMONG THE RADIATION-HARDENED NV MAGNETIC LATCHES

Designs	SNU Tolerance	DNU Tolerance	Backup Ability	Restore Ability	D-Q Delay (ps)	10^{-4}×CMOS Area (nm^2)	Power (μW)	MTJ Counts
Design in [15]	√	×	√	√	55.03	10.13	18.72	2
Design in [16]	√	×	√	√	35.35	9.52	11.15	2
Design in [18]	√	×	√	√	44.65	8.30	11.10	2
Modi-design in [13]	√	×	×	√	50.827	6.89	14.46	4
Modi-design in [19]	√	√	×	√	101.742	15.39	17.15	2
M-TPDICE (Proposed)	√	√	√	√	2.02	14.99	14.53	2

average of the power dissipation (dynamic, static and backup), and "MTJ Counts" means the number of used MTJs in each design. It can be seen from Table I that, the modified-design in [19] consumes the largest D-Q delay (mainly due to more devices from D to Q) and consumes the largest CMOS area (mainly due to its more used transistors); the modified-design in [13] has four MTJs to store the values; the design in [15] consumes the largest power; however, the proposed latch consumes the smallest D-Q delay because there are fewer devices from D to Q. In other words, compared with the existing hardened latches, the proposed latch only requires moderate overhead so as to perform radiation-hardening and provide NV features.

V. CONCLUSION

This paper has proposed a novel DNU-completely-hardened NV magnetic latch design based on an extended TPDICE and MTJs for robust computing in radiation environments. Owing to the SNU recovery and redundant nodes of the extended TPDICE, and error-interception of the CG-based 3-input CE, the latch is completely DNU-hardened. Moreover, the latch can also provide non-volatility because of the use of MTJs. Simulation results demonstrate the complete DNU hardening, non-volatility and moderate overhead of the proposed latch.

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