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Effects of High-Energy Protons on a Self-Refresh DRAM

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Abstract

This work targets the study of the effects of high-energy protons on a commercial self-refresh DRAM. The memory devices under investigation were exposed to high-energy protons varying in a range from 70 MeV up to 230 MeV at the Proton Irradiation Facility in the Paul Scherrer Institute. The radiation-induced faults were identified as Single-Bit Upsets, stuck bits, and block errors. These results are in line with the outcome of our previous test campaigns, targeting thermal and atmospheric-like neutrons. The event cross sections for each fault type and energy are presented and discussed.

Index Terms

high-energy protons, radiation effects, self-refresh DRAM, SEEs.

I. Introduction

Space systems are continuously exposed to space radiation, which contains particles such as protons, electrons, and heavy ions. The main radiation sources in the space environment are galactic cosmic rays, energetic particles trapped in the Van Allen belts, and solar particle events. These radioactive particles cause damaging effects on semiconductors, leading to device error and failures [1].

Dynamic random-access memories (DRAMs) are used in electronic systems. They consist of capacitive cells that must be recharged frequently to keep their energy level. When exposed to radiation, the leakage current of DRAM cells increases, reducing their retention capability. The affected cells may appear as stuck bits, generally induced by radiation [2]–[4]. In [5], [6] the authors have shown that the single-particle displacement damage effect, induced by single high-energy neutrons and protons, is the leading cause of stuck bits. In [7] the authors state that recent DRAM technologies may be more susceptible to stuck bit behavior due to significantly decreased retention times.

In previous works [8], [9], we presented the effects of thermal and atmospheric-like neutron irradiation on a self-refresh DRAM, also known as Pseudo-Static RAM (PSRAM). In both works, we identified the occurrence of Single-Bit Upsets (SBUs), stuck bits, and block errors (SEFIs – Single-Event Functional Interrupts) in the memory. Besides that, we analyzed the damaged cells' retention time, which shows a difference in the efficiency between the self-refresh mechanism and an actual read operation. A correlation of the fault mechanism that generates both SBUs and stuck bits under neutron irradiation was also proposed, in line with the results under electron irradiation in [10].

This work extended the studies analyzing the effects under high-energy protons to compare the fault mechanisms with the results obtained for neutron particles. Furthermore, we presented and discussed the event cross sections for each fault type and energy.

The rest of the paper is structured as follows: Section II presents the Device Under Test (DUT), the test facility, the experimental setup, and the applied test mode; Section III presents and analyses the results from the high-energy proton irradiation; Section IV concludes the work.

II. Experiment

A. Device Under Test

The DUT is a DRAM memory manufactured by Infineon Technologies, the S27KS0642GABHI020 [11]. The device is designed with a 38 nm high-speed CMOS technology, using a Double Data Rate (DDR) interface to reach a data throughput up to 400 MBps with a maximum operation clock of 200 MHz. The DUT is commercially known as

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HyperRAM™ and its interface as HyperBus™. Due to a self-refresh mechanism that performs refresh operations on the cells without the controller intervention, this type of memory is also known as pSRAM (pseudo-SRAM). The device has a capacity of 64 Mib using a logical structure of 8192 rows, with each row containing 512 words (16 bits) addresses.

B. Test Facility

This experiment was performed in the Proton Irradiation Facility (PIF), part of the Paul Scherrer Institute (PSI) in Switzerland. The facility was constructed for testing spacecraft components, and it is capable of generating proton energies relevant to harsh space environments. During the test campaign, the instruments were configured to generate protons with energies ranging from 70 MeV to 230 MeV, targeting different fluxes from $3 \cdot 10^7$ to $8 \cdot 10^7$ p/cm^2/s. The primary proton energy used was 230 MeV with a flux of $8 \cdot 10^7$ p/cm^2/s, and to reach lower energies, metal plates were placed in the beam path to reduce the energy of the protons. The experiment started with 230 MeV, decreased to the lowest energy of 70 MeV, and finalized with 150 MeV. The beam homogeneity was checked for each energy setting, and the reported proton fluence variation on the DUTs is estimated to be less than 10%. The DUT was evaluated at room temperature.

C. Test Setup

In order to test the DUT, a controller board based on the Zynq-7000 SoC from Xilinx was used to implement the HyperBus™ interface and enable the execution of test algorithms. A daughterboard was used to connect the DUT to the controller. The controller was composed of a configurable System-on-Chip (SoC) architecture, which provides: a Cortex™-A9 processor, used for test execution; several peripherals for communication and development; and the SoC's programmable logic, in which an IP (Intellectual Property) provided by Infineon managed the communication between the processor and the DUT.

An external current monitor was utilized during the experiment to identify Single Event Latch-up (SEL) events. The results generated with the experimental tests were logged for posterior analysis, including faulty logical addresses, bit error data, and operation status. The controller board was positioned out of the effective beam area to improve the dependability of the test setup.

Fig. 1 summarizes the complete test setup used for the experiment, and Fig. 2 shows the control board and the daughter board with the mounted DUT.

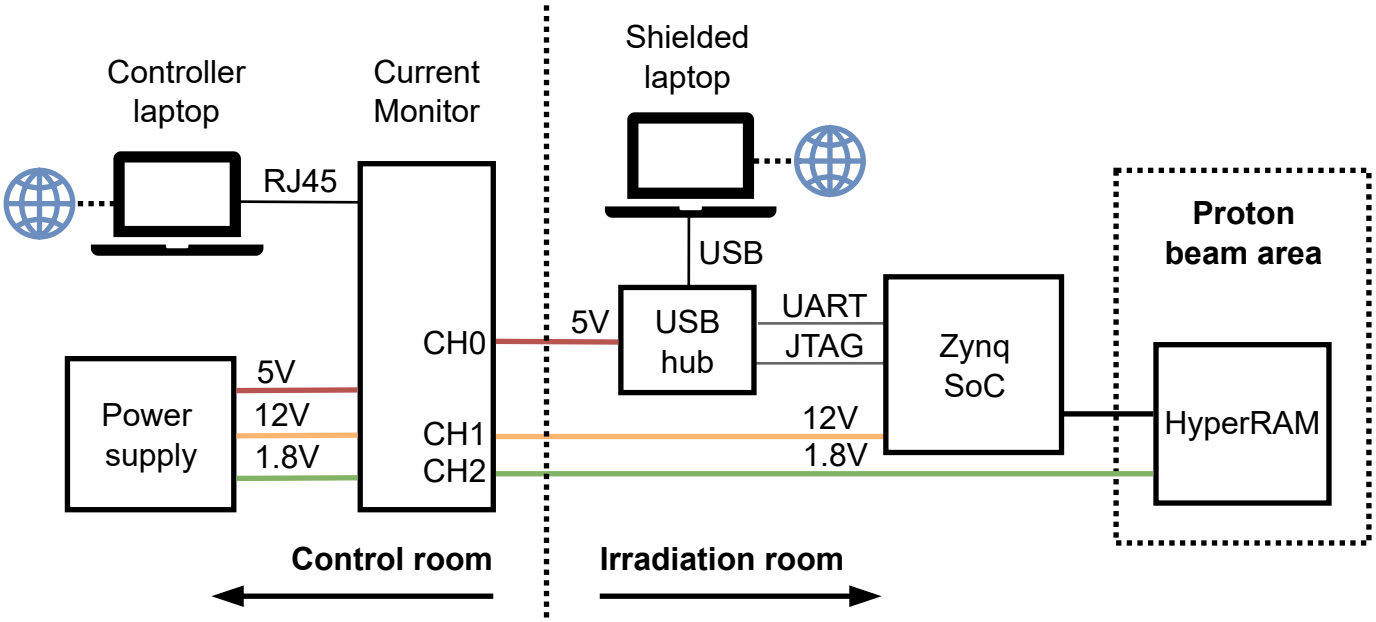

Fig. 1. Tools and setup used during the test campaign.

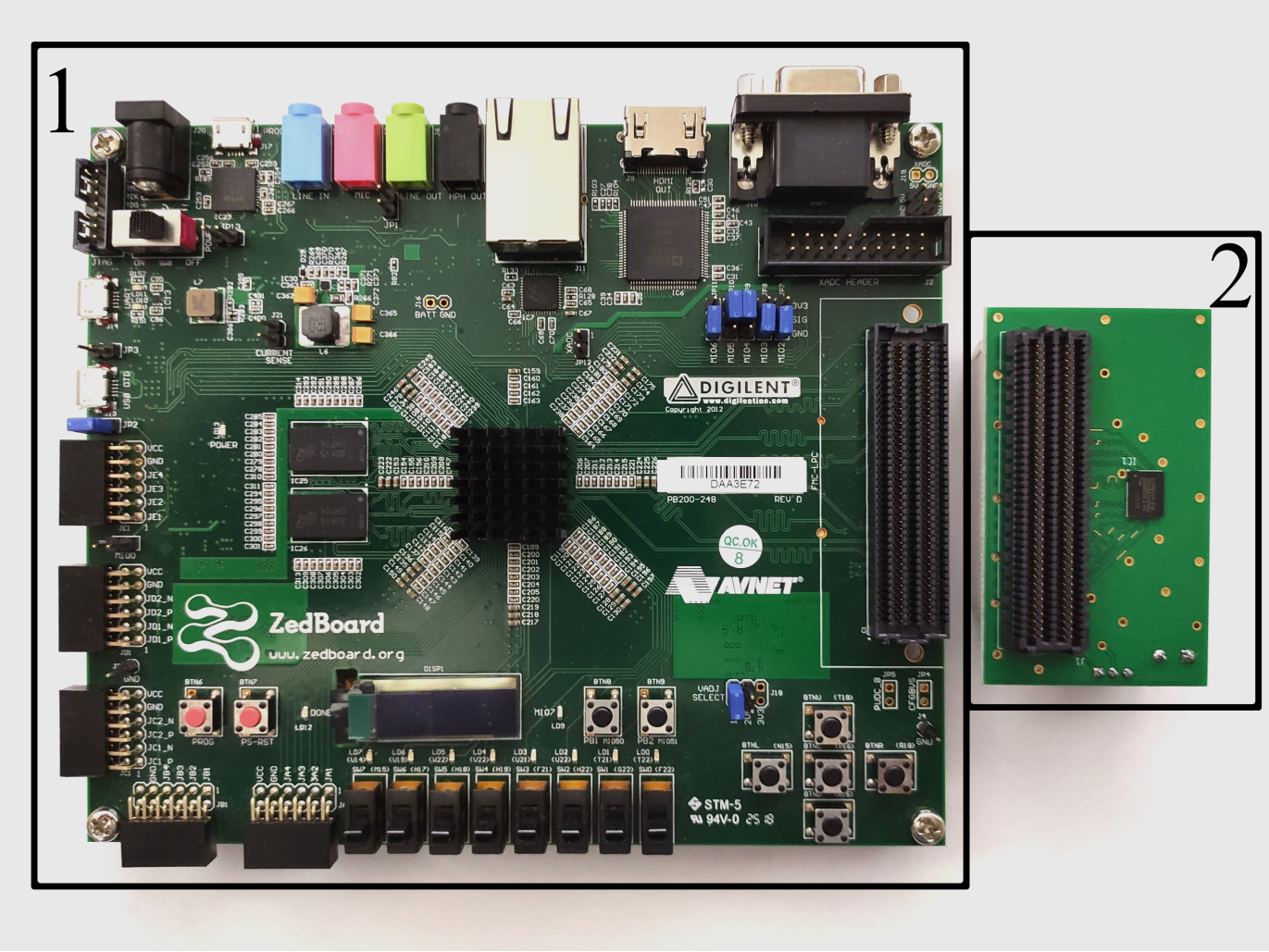

Fig. 2. Top-down photograph of the controller board (square 1) and the daughter board (square 2) [8].

D. Test Mode

This experiment employed dynamic testing of the memory, in which write and read operations were executed under irradiation, generating radiation-induced upset events during active utilization of the DUT. This approach leads to a more realistic evaluation of the faults identified since the DUT operation behavior is similar to an actual application use case. In this experiment, the dynamic test used was the March C- algorithm, which consists of a sequence of reads and writes, described in (1), where the arrow indicates the addressing order ('↑' up or '↓' down), 'w' (write), and 'r' (read) indicates the operation, and the following Boolean number indicates the data background. Also, between test runs, functional testing was performed to provide further assessments of the DUT and the controller itself.

$$\begin{aligned} &\uparrow (w0); \\ &\{\uparrow (r0, w1); \uparrow (r1, w0); \downarrow (r0, w1); \downarrow (r1, w0); \uparrow (r0)\} \end{aligned} \tag{1}$$

III. Results

In order to analyze the error data in this work, we used two approaches: logical bitmaps to provide an overview of the errors and their patterns, and cross section plots for measuring the occurrence of the events. The found proton-induced events have the same classification as ones from previous works focusing on neutron effects: SBUs, stuck bits, and SEFIs (block errors) [8], [9]. Fig. 3 presents an example of a logical bitmap, which illustrates each type of error. The red bounding boxes show the errors within that area, increasing their size to improve the visualization. In 1, SBUs and stuck bits are represented. In 2 and 3, horizontal and vertical block errors are shown, respectively.

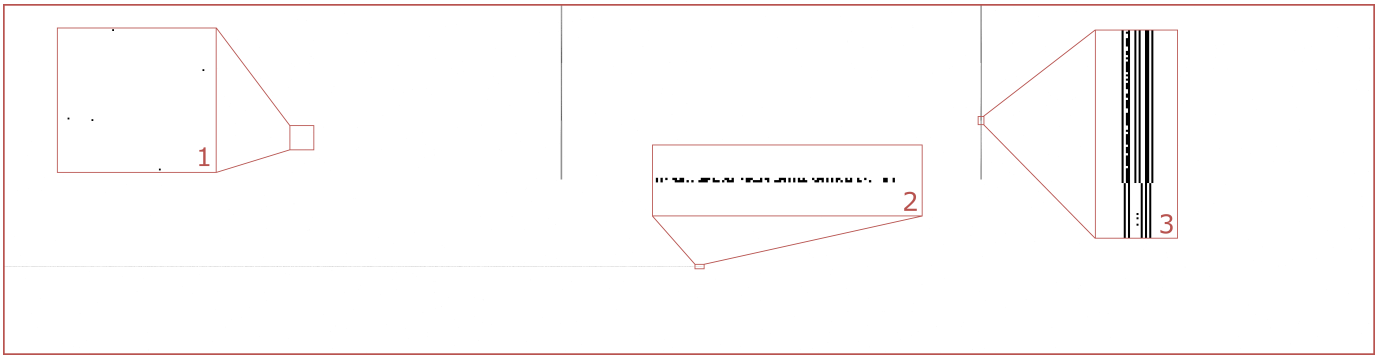

Fig. 3. Example of error types in the logical memory bitmap represented by 16384 columns per 4096 rows. The bits are represented as pixels, and each pixel with an error appears in black. Zoom-ins are added to increase the visibility of the block event and the SBU and/or stuck bit. The zoom-in box (1) presents SBUs and/or stuck bits randomly spread in the memory array, (2) a block event in a horizontal shape, and (3) a block event in a vertical shape.

It is important to note that in previous studies [8], [10] it is proposed that SBUs and stuck bits have the same fault mechanism: the degradation of retention time. Despite that, the cross sections of these errors are presented separately since the fault model to represent both are different. SBUs were classified as bits appearing as a '0' to '1' or '1' to '0' transition that occurred only once during the test campaign, which means that after a write operation in the bit cell, the same was not recurrently (at least one more time) recognized as faulty. Stuck bits also appeared as a transition from both logic values. However, in this case, the bit was recurrently (at least twice, and after write operations) recognized as a faulty bit.

Fig. 4 and Fig. 5 present, respectively, the SBUs and stuck bits cross sections. The values are presented for each proton energy. The cross section is calculated as:

$$\sigma_{(bit)} = \frac{N}{F \times M} \tag{2}$$

where N is the number of events (SBUs or stuck bits), F is the cumulative run fluence, and M is the memory size in bits. In the results, the errors bars represent a 95% confidence interval with a 10% beam fluence uncertainty.

For both cases, SBUs and stuck bits, the number of events increased with the energy. However, it is important to note that the error bars, in some cases, overlap. It can be seen, e.g., in Fig. 4, where the calculated cross section and its error bar for 230 MeV are included in the same range of the calculated values for 150 MeV. Furthermore, for all energies, the cross section for stuck bits is higher in comparison with the ones for SBUs. In dynamic mode, where the cells are constantly accessed with write and read operations, a similar behavior was found on the same memory under thermal and atmospheric-like neutron spectra [9].

Besides the SBUs and stuck bits, block errors were observed at 230 MeV, but not for the lower energies. Since the number of block errors events at 230 MeV was very low (giving the high error bars), the probability of having the same type of events in the lower energies should not be discarded.

For evaluating the cross section for this kind of event, since this fault is related to the control logic of the device, we may define the cross section as:

$$\sigma_{\text{device}} = \frac{N}{F} \tag{3}$$

where the memory size is removed from the equation, and the cross section is device-based. Fig. 6 presents the block error cross section for each proton energy.

As stated above, since there was no occurrence of block errors for 70 MeV and 150 MeV, in Fig. 6 there are no points for both energies, and we are reporting only the error bars.

Finally, as described in subsection II-C, the DUT current was monitored during the whole test campaign, and no SEL was identified.

IV. Conclusion

In this work, the effects of high-energy protons on a self-refresh DRAM were investigated and reported. The experiment results were analyzed using cross sections and logical bitmaps, which enabled the visualization and evaluation of the detected fault events. Despite the possible different physical phenomena related to protons and

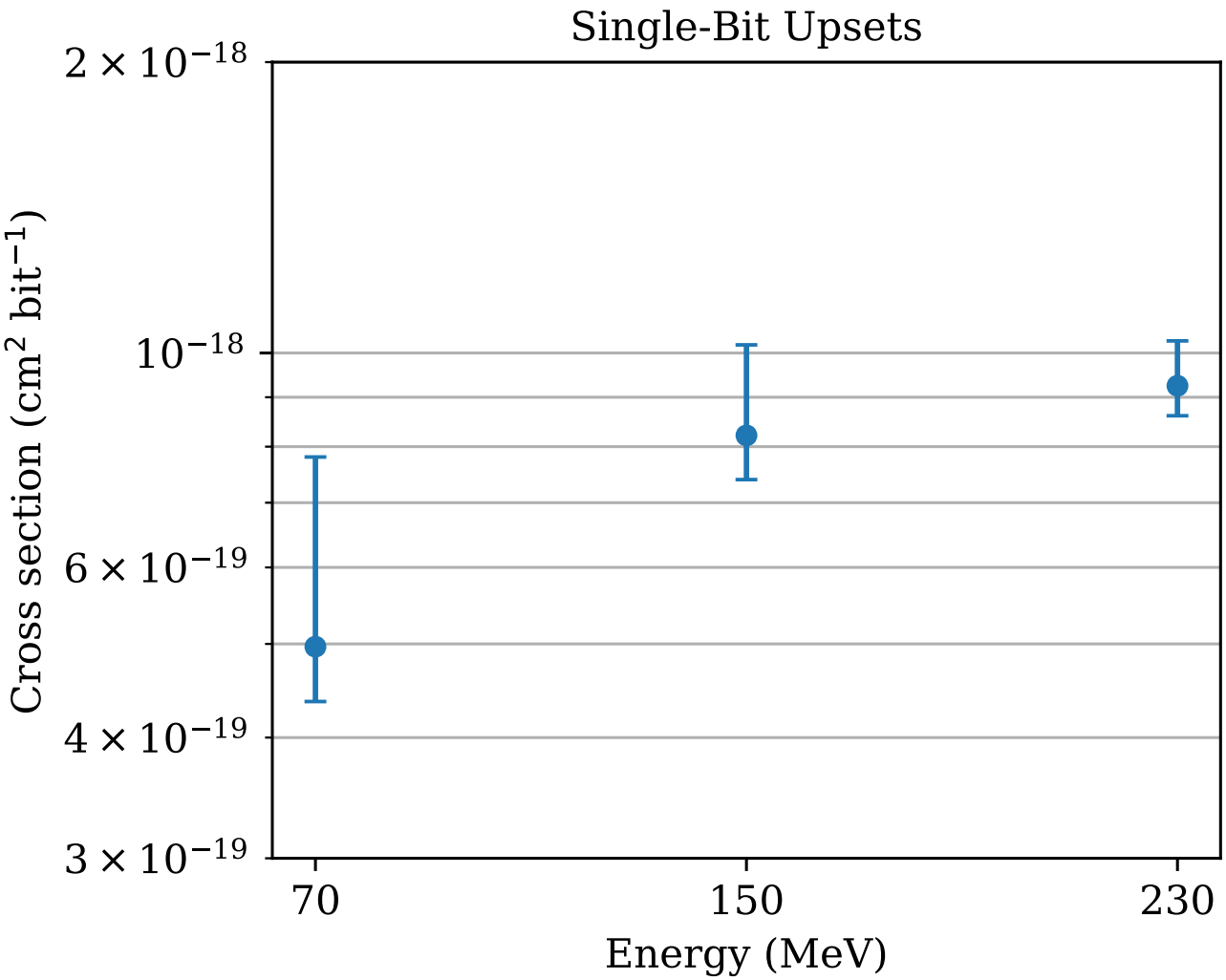

Fig. 4. Estimated SBUs bit cross section for each energy value. The error bars represent a 95% confidence interval with a 10% beam fluence uncertainty.

neutrons events generation, the fault mechanisms identified in this work were similar to those encountered in the previous works with neutrons: SBUs, stuck bits, and block errors (SEFIs).

The results have shown a higher occurrence of stuck bits in comparison with the SBUs, where the cross section value increased according to the energy. The block errors were observed as long horizontal and vertical lines, where several memory cells in different addresses are affected due to a single event, presenting a significant impact on critical applications.

For future work, we intend to investigate the retention time of the tested samples to achieve a deeper understanding of the memory cells degradation and to obtain a better correlation with previous studies.

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References

[1] C. Claeys and E. Simoen, *Radiation effects in advanced semiconductor materials and devices*. Springer Science & Business Media, 2002, vol. 57, DOI: 10.1007/978-3-662-04974-7.

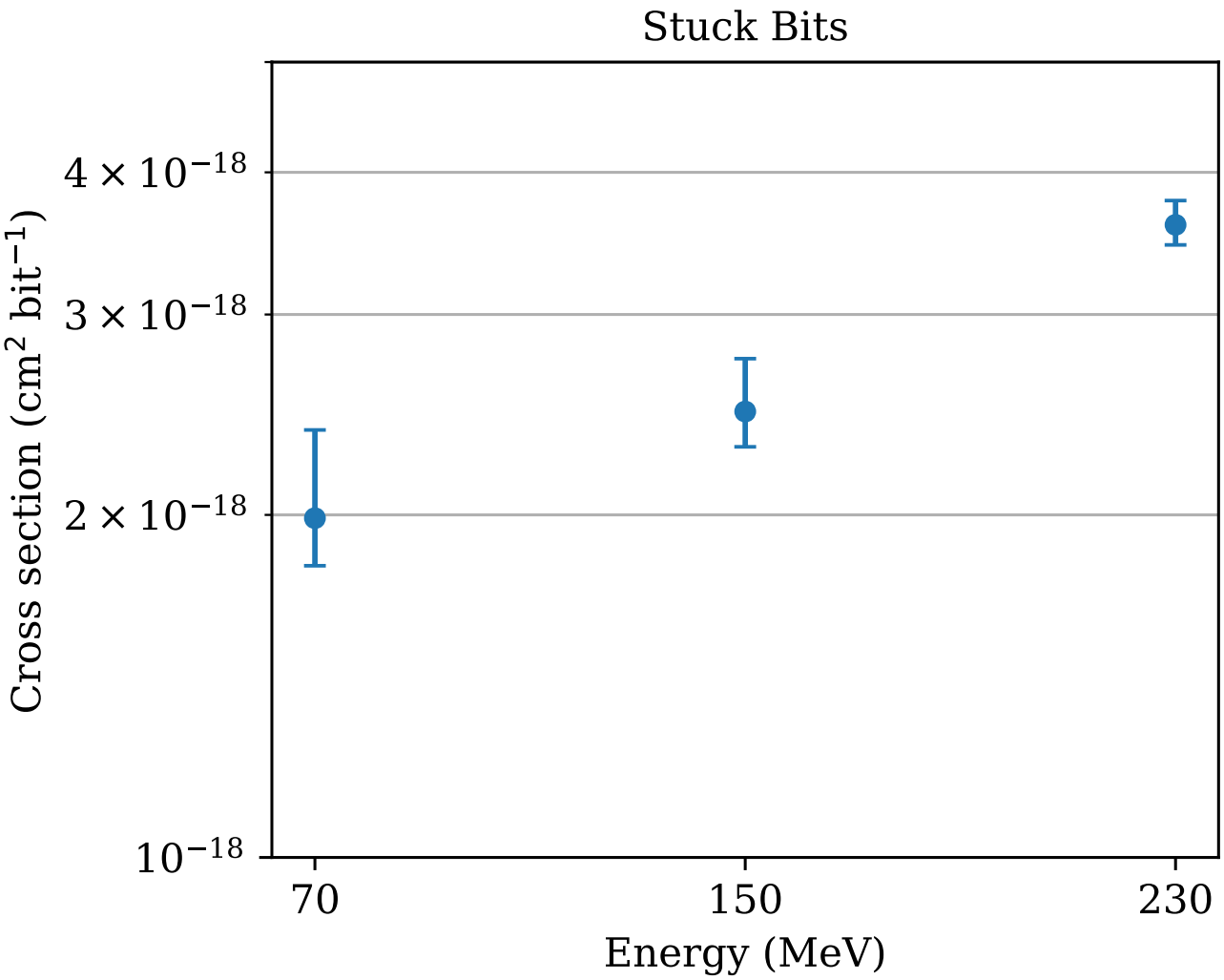

Fig. 5. Estimated stuck bits bit cross section for each energy value. The error bars represent a 95% confidence interval with a 10% beam fluence uncertainty.

[2] L. D. Edmonds and L. Z. Scheick, "Physical mechanisms of ion-induced stuck bits in the hyundai 16m¡formula formulatype="inline"¿¡tex notation="tex"¿ × ¡/tex¿ ¡/formula¿4 sdram," *IEEE Transactions on Nuclear Science*, vol. 55, no. 6, pp. 3265–3271, 2008, DOI: 10.1109/TNS.2008.2006902.

[3] K. Lee, C.-H. Yun, H. Seo, T. Kang, Y. Lee, and K. Cho, "An evaluation of x-ray irradiation induced dynamic refresh characterization in dram," in *2019 IEEE International Reliability Physics Symposium (IRPS)*, 2019, pp. 1–3, DOI: 10.1109/IRPS.2019.8720574.

[4] C. Lim, H. S. Jeong, G. Bak, S. Baeg, S.-J. Wen, and R. Wong, "Stuck bits study in ddr3 sdrams using 45-mev proton beam," *IEEE Transactions on Nuclear Science*, vol. 62, no. 2, pp. 520–526, 2015, DOI: 10.1109/TNS.2015.2392851.

[5] A. M. Chugg, A. J. Burnell, P. H. Duncan, S. Parker, and J. J. Ward, "The random telegraph signal behavior of intermittently stuck bits in sdrams," *IEEE Transactions on Nuclear Science*, vol. 56, no. 6, pp. 3057–3064, 2009, DOI: TNS.2009.2032184.

[6] A. M. Chugg, J. McIntosh, A. J. Burnell, P. H. Duncan, and J. Ward, "Probing the nature of intermittently stuck bits in dynamic ram cells," *IEEE Transactions on Nuclear Science*, vol. 57, no. 6, pp. 3190–3198, 2010, DOI: 10.1109/TNS.2010.2084103.

[7] L. Scheick, S. Guertin, and D. Nguyen, "Investigation of the mechanism of stuck bits in high capacity sdrams," in *2008 IEEE Radiation Effects Data Workshop*, 2008, pp. 47–52, DOI: 10.1109/REDW.2008.15.

[8] L. M. Luza, D. Söderström, H. Puchner, R. G. Alía, M. Letiche, A. Bosio, and L. Dilillo, "Effects of thermal neutron irradiation on a self-refresh dram," in *2020 15th Design Technology of Integrated Systems in Nanoscale Era (DTIS)*, 2020, pp. 1–6, DOI: 10.1109/DTIS48698.2020.9080918.

[9] L. Matana Luza, D. Söderström, H. Puchner, R. G. Alía, M. Letiche, C. Cazzaniga, A. Bosio, and L. Dilillo, "Neutron-induced effects on a self-refresh dram," *Microelectronics Reliability*, vol. 128, p. 114406, 2022, DOI: 10.1016/j.microrel.2021.114406.

[10] D. Söderström, L. M. Luza, H. Kettunen, A. Javanainen, W. Farabolini, A. Gilardi, A. Coronetti, C. Poivey, and L. Dilillo, "Electron-induced upsets and stuck bits in sdrams in the jovian environment," *IEEE Transactions on Nuclear Science*, vol. 68, no. 5, pp. 716–723, 2021, DOI: 10.1109/TNS.2021.3068186.

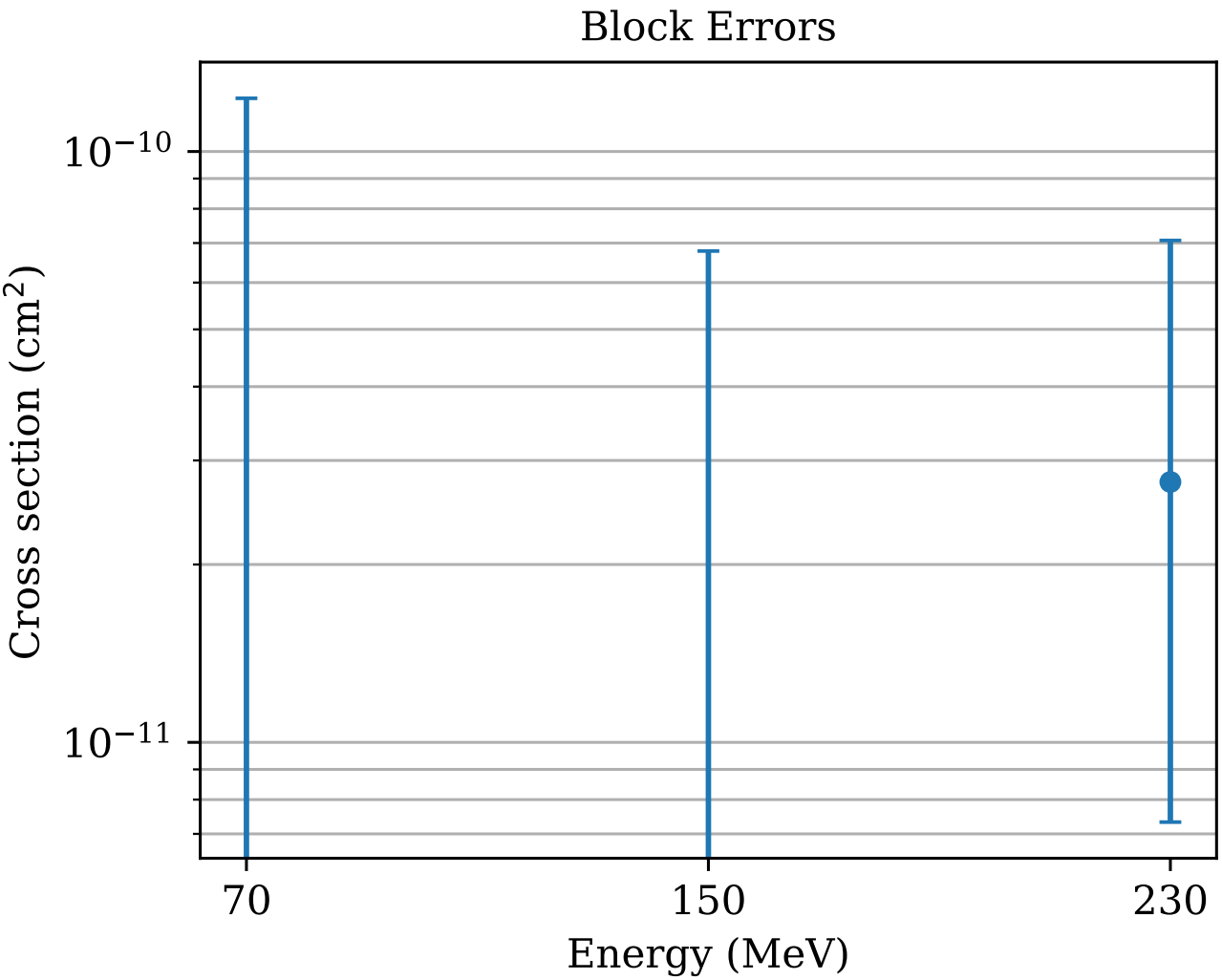

Fig. 6. Estimated block errors bit cross section for each energy value. The error bars represent a 95% confidence interval with a 10% beam fluence uncertainty.

[11] Infineon, *S27KL0642/S27KS0642 - 64-Mb HYPERRAM™ self-refresh DRAM (PSRAM), HYPERBUS™ interface, 1.8 V/3.0 V, Rev. H*, Infineon Technologies AG, Jan. 2022, accessed on: February 10, 2022. [Online]. Available: https://www.infineon.com/dgdl/Infineon-S27KL0642_S27KS0642_3.0_V_1.8_V_64_Mb_(8_MB)_HyperRAM_Self-Refresh_DRAM-DataSheet-v08_00-EN.pdf?fileId=8ac78c8c7d0d8da4017d0ee8a1c47164